UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
PROGRAMA DE PÓS-GRADUAÇÃO EM MICROELETRÔNICA

PAULO FRANCISCO BUTZEN

Aging Aware Design Techniques and CMOS Gate Degradation Estimative

Thesis presented in partial fulfillment of the requirements for the degree of Doctor in Microelectronics

Prof. Dr. Renato Perez Ribas
Advisor

Prof. Dr. André Inácio Reis
Co-advisor

Porto Alegre, October 2012.

CIP – CATALOGAÇÃO NA PUBLICAÇÃO

Butzen, Paulo Francisco

Aging Aware Design Techniques and CMOS Gate Degradation Estimative [manuscrito] / Paulo Francisco Butzen. – 2012.

79 f.:il.

Orientador: Renato Perez Ribas; Co-orientador: André Inácio Reis.

Tese (doutorado) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Microeletrônica. Porto Alegre, BR – RS, 2012.

1.Projeto de circuitos integrados digitais. 2.Portas Lógicas 3.Efeitos de Envelhecimento. I. Ribas, Renato Perez. II. Reis, André Inácio. III. Título.

UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
Reitor: Prof. Carlos Alexandre Netto
Vice-Reitor: Prof. Rui Vicente Oppermann
Pró-Reitor de Pós-Graduação: Prof. Aldo Bolten Lucion
Diretor do Instituto de Informática: Prof. Luis da Cunha Lamb
Coordenador do PGMICRO: Prof. Ricardo Reis
Bibliotecária-Chefe do Instituto de Informática: Beatriz Regina Bastos Haro

ACKNOWLEDGMENT

Firstly I would like to thank God for the wonderful life that I have and for keeping up my courage and enthusiasm every day.

I would like to express my gratitude to my family, especially to thank my mom, Gloria, and my dad, Otavio, and my sister, Paula, for their patience, encouragement and love. They were always supporting me and encouraging me with their best wishes.

I acknowledge my fiancée, Raquel, for her love, care, partnership, and support. She was always there cheering me up and stood by me through the good times and bad.

I would like to thank CNPq for financial support. And also thank all my colleagues from LOGICS Research Lab. They were always willing to help and give their best suggestions.

Finally, I would like to express my gratitude to my advisors, Renato Perez Ribas and André Inácio Reis, for their guidance, patience and example. They were always close and ready to guide me when the things seemed dark and the project seemed endless.

TABLE OF CONTENTS

LIST OF ABBREVIATIONS

ASIC	Application-Specific Integrated Circuits
CLA	Carry Look Ahead
CMOS	Complementary Metal Oxide Semiconductor
FPGA	Field-Programmable Gate-Arrays
HCI	Hot Carrier Injection
HDB	Hard Breakdown
IC	Integrated Circuit
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTCMOS	Multi Threshold Complementary Metal Oxide Semiconductor
NBTI	Negative Bias Temperature Instability
NMOS	N-type Metal Oxide Semiconductor
PBD	Progressive Breakdown
PLD	Programmable Logic Devices
PMOS	P-type Metal Oxide Semiconductor
PTM	Predictive Technology Model
RTL	Register Transfer Level
SBD	Soft Breakdown
SEE	Single Event Effects
SET	Single Event Transient
SEU	Single Event Upset
TDDB	Time Dependent Dielectric Breakdown
TDI	Total Dose Ionization
TSP	Transistor Stress Probability
TSwP	Transistor Switching Probability
VLSI	Very Large Scale Integration

LIST OF FIGURES

LIST OF TABLES

ABSTRACT

The increased presence of integrated circuit (IC) in the people's life has occurred for main two reasons. The first is the aggressive scaling of integrated device dimensions. This miniaturization enabled the construction of smaller, faster and lower power consumption devices. The other factor is the use of a cell based methodology in IC design. This methodology is able to provide efficient circuits in a short time. With the devices scaling, new factors that were usually ignored in micrometer technologies have become relevant in nanometer designs. Among them, it can be mentioned the static consumption, process parameters variability, manufacturability and aging effects. Some of these factors, such as static consumption and variability, are already taken into account by the standard cell design methodology. On the other hand, the degradation caused by aging effects has increased at each new technology node, as well as the importance in relation to the circuit reliability throughout its entire lifetime has also increased. This thesis explores such aging effects in the design of digital IC. The main contributions can be highlighted as the definition of a cost of aging that can be exploited by logic synthesis algorithms to produce a more reliable circuit. This cost can be also used by the analysis tools in order to obtain an estimative of the degradation that specific circuit experiences throughout their lifetime. In addition, a proposal to reorder the transistor structural arrangement of logic gates is presented in order to treat the effects of aging on initial steps in the design flow. Finally, a simplified analysis of the characteristics to be exploited at circuit level is performed exploring details of the design of complex logic gates. The aging cost results have given a good and fast prediction of logic gates degradation. The transistor arrangement restructuring approach is a good alternative to design more reliable circuits. Furthermore, the use of complex arrangements is also an excellent alternative which exploits the intrinsic robustness of series transistors association. Moreover, the discussed approaches can be easily used together with existing techniques in the literature to achieve better results.

Keywords: digital integrated circuit design, logic gates, CMOS technology, aging effects, modeling, reliability.

Técnicas de Projeto Considerando Envelhecimento e Estimativa da Degradação em Portas Lógicas CMOS

RESUMO

O advento da utilização de circuitos integrados pela sociedade se deu por dois motivos. O primeiro consiste na miniaturização das dimensões dos dispositivos integrados. Essa miniaturização permitiu a construção de dispositivos menores, mais rápidos e que consomem menos frequência. O outro fator é a utilização da metodologia baseada em biblioteca de células. Esta metodologia permite o projeto de um circuito eficiente em um curto espaço de tempo. Com a redução dos dispositivos, novos fatores que eram desconsiderados no fluxo automático passaram a ter importância. Dentre eles podemos citar o consumo estático, a variabilidade, a manufaturabilidade e o envelhecimento. Alguns desses fatores, como o consumo estático e a variabilidade, já estão integrados à metodologia baseada em biblioteca de células. Os efeitos de envelhecimento tem sua degradação aumentada a cada novo processo tecnológico, assim como tem aumentado também a sua importância em relação à confiabilidade do circuito ao longo da sua vida útil. Este trabalho irá explorar estes efeitos de envelhecimento no projeto de circuitos integrados digitais. Dentre as principais contribuições pode-se destacar a definição de um custo de envelhecimento na definição de portas lógicas, que pode ser explorado pelos algoritmos de síntese lógica para obterem um circuito mais confiável. Este custo também pode ser utilizado pelas ferramentas de análise a fim de obter uma estimativa da degradação que o circuito proposto irá sofrer ao longo da sua vida útil. Além disso, é apresentada uma proposta de reordenamento estrutural do arranjo de transistores em portas lógicas, a fim de tratar os efeitos de envelhecimento nos níveis mais iniciais do fluxo. Por fim, uma análise simplificada de características a serem exploradas ao nível de circuito é discutida utilizando o auxílio do projeto de portas lógicas complexas. Os resultados apresentam uma boa e rápida estimativa da degradação das portas lógicas. A reestruturação do arranjo dos transistores tem se apresentado como uma boa alternativa ao projeto de circuitos mais confiáveis. Além disso, a utilização de arranjos mais complexos também é uma excelente alternativa que explora a robustez intrínseca da associação de transistores em série. Além disso, as alternativas propostas podem ser utilizadas em conjunto com técnicas já existentes na literatura.

Palavras-Chave: projeto de circuitos integrados digitais, portas lógicas, tecnologia CMOS, efeitos de envelhecimento, modelagem, confiabilidade.

1 INTRODUCTION

The presence of digital integrated circuits (IC) in people's lifestyle has increased significantly during the last decades. These components can be found from computers and mobiles to embedded systems in cars and house appliances. This success is mainly due to the progress achieved by the semiconductor industry.

The semiconductor industry has been guided by the "Moore's Law". In 1965, Gordon E. Moore predicted that the numbers of transistors that could be integrated in a single die would double every 24 months (MOORE, 1965). Such behavior has been roughly confirmed until now, as illustrated in Figure 1.1 (INTEL, 2010). This increment in transistor count is resulted from the scaling down of device dimensions. In general, the scaling process improves the amount of device in the same area, increases the transistor speed and reduces the individual parasitic capacitances. However, a drawback of this scaling is the advent of several effects that were usually neglected in micrometer technologies due to their insignificant magnitude. Static currents, performance variability and device reliability are some examples of those new issues that have to be considered in nanometer IC design (RABAEY, 2003).

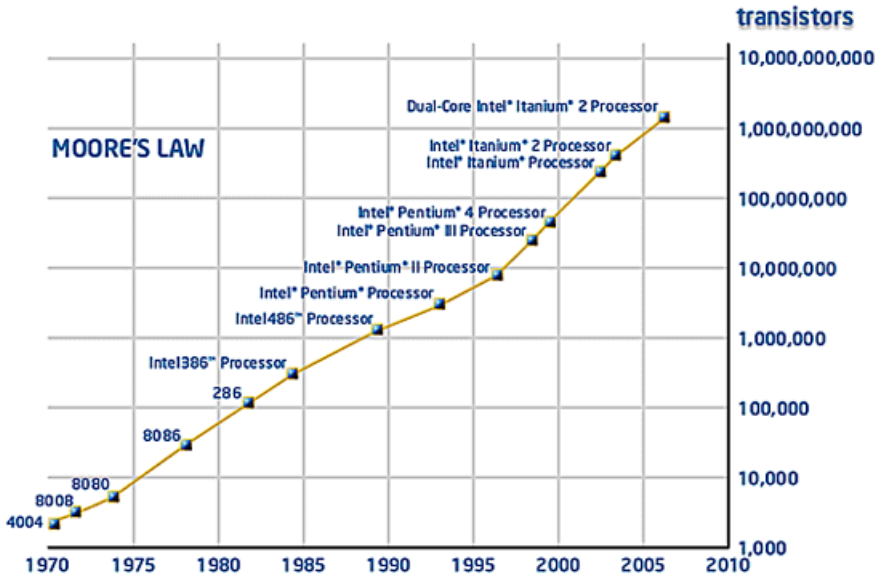


Figure 1.1 – Evolution in the amount of transistors in Intel processors (INTEL, 2010).

On the other hand, different design solutions can be explored to implement electronic systems. The choice of the most efficient solution involves the evaluation of the costs, capabilities and limitation of each design style based on the circuit requirements. Basically, digital circuits can be designed from three different approaches. A microprocessor can perform the computation from a functional circuit

specification, through an algorithm description (software programing). Programmable logic devices (PLDs), in turn, are usually used to implement the circuit from a register transfer level (RTL) description, which specifies the components and connections required to achieve the circuit behavior. The last approach consists in designing the entire layout of an integrated circuit. An automated flow, known as standard cell design methodology, that reuses pre-designed and pre-characterized gates, is a common strategy for fast development of the physical design of a chip (WESTE, 2004).

This thesis investigates the reliability aspect of IC designed in nanometer technologies. The consequences of emerging aging effects during the entire system lifetime are investigated. The focus is centered in the design solutions that can be applied in standard cell methodology to generate more reliable circuits. CMOS logic gates and circuit level design solutions are explored.

The rest of the text is organized as follow. The basic concepts of VLSI design solutions and a brief review of the challenges related to the technology scaling process are presented in Chapter 2. The physics mechanisms behind three aging effects and respective analytical models are discussed in Chapter 3. In Chapter 4 are discussed several solutions proposed to deal with the aging degradation. A lack of design solutions to deal with this aging degradation in the standard cell flow motivates the proposals presented in the last section of that chapter. The definition of a logic gate aging cost is presented in Chapter 5, whereas design solutions at circuit level are explored in Chapter 6. Conclusions and final remarks are presented in Chapter 7.

2 PRELIMINARIES

This chapter presents the basic concepts associated to solutions explored in this thesis. The different digital system design methodologies are initially discussed. The standard cell methodology receives special attention since the most of the proposed approaches are directly applied in this scope. The new design challenges introduced by the technology scaling are presented in following. The discussion presents a brief overview of the physics and some design techniques for each design topic.

2.1 Digital System Design Methodologies

Due to the wide variety of potential applications and the current complexity of the circuits, the choice of the correct design solution is crucial to the success of an electronic product. This choice involves mainly the evaluation of economic cost, circuit performance and time-to-market. The main difference between the existing solutions is the integrated components associated (WESTE, 2004).

A digital system can be developed by programming a microprocessor or microcontroller. In this approach, a generic microprocessor is programmed by software for a desired application. Hardware integration that explores this type of solution has associated with it reduced design cost and development time. Since the solution involves programing in high level language, the approach presents good flexibility. However, such solution tends to have the worst performance in terms of speed and power consumption when compared to other existing methodologies. Also, the unit cost of a microprocessor can be considered elevated. This solution is ideal when the project requires short time-to-market and flexible product constrains.

Another approach is the use of programmable logic devices (PLDs). In this case, the programming is done at the hardware level system. When compared to microprocessors, this solution presents a better performance in terms of speed and power consumption at the cost of non-recurring engineering (NRE) cost and development time. A variety of PLDs are available. Each one has their own architecture and technology of configuration, impacting the performance, cost and programmability characteristics. FPGAs and CPLDs are the most powerful programmable devices. They are usually designed in modern manufacturing processes and uses static RAM and flash memories to configure routing and logic functions. Such solution is usually adopted when microprocessors does not achieve speed and power consumption requirements.

In addition to the two previous approaches, there is a third solution related to the development of application specific integrated circuits (ASICs). It is commonly used in applications that have strict time and power consumption constraints. Moreover, due to the cost associated with the customized manufacturing process, the development of

ASICs is more associated to products of high market demanding. There are two main methodologies that used in IC design: the full-custom and the standard cells.

In full-custom methodology, all geometric forms of layout that represent the devices and interconnection in the circuit are designed individually (customized). From this degree of freedom is possible to obtain almost optimal circuit in terms of area, speed and power consumption. The main drawback is the exhaustive handmade tasks, increasing significantly the final design cost. Typically, such approach is used to improve the circuit area, performance and/or power consumption in respect to the standard cells design.

A cell-based methodology, also known as standard cell methodology, is widely used in ASIC design. This approach in based on standard cell library that contains several pre-designed and pre-characterized gates as the basic block to be automatically reused in the IC design. The circuit designed using the standard cell methodology does not have the NRE costs as elevated as the circuit designed using the full-custom approach. There are two main reasons for this reduced cost. The first one is the fact that the basic block is a pre-designed logic gate instead of geometric forms of full-custom methodology. The second one is the existence of a complete automated flow that explores the cells available in a target library.

Table 2.1 summarizes the main characteristics of each solution discussed previously. The remainder of this section presents the standard cell design flow and explores the potential points of optimization.

Table 2.1 – Comparison of CMOS digital circuit design solutions.

Design Solution		Unit Cost	Complexity/Cost of Implementation	Time to Market	Speed	Power Consumption	Flexibility
Microprocessor		Medium	Low	Low	Low	High	High
PLD		Medium	Medium	Low	Medium	Medium	Medium
IC Design	Cell-Based	Low	High	High	High	Low	Low
	Full-Custom	Low	High	High	Very High	Low	Low

2.1.1 Standard Cell Design Flow

The standard cell design flow is widely used to design integrated circuits. The main factors contributing to this great spread are:

- Automated design flow which provides a quickly development time when compared to full-custom methodology;
- The use of a cell library which consists of a set of logic gates already designed and previously characterized;
- Possibility to generate a circuit with nearly optimal results with respect to performance, area and power.

This methodology can be divided into two main stages, as illustrated in Figure 2.1. The logic synthesis generates a structural description composed by logic gates and registers from a circuit specification created from the product requirements. This step

explores the selection of logic gates from a pre-designed library to represents the best result considering the design constraints. The physical synthesis generates the circuit layout from the structural description provided by the logic synthesis. It is responsible for the circuit organization, the placement of logic gates and the signals routing. In both stages are carried out tests to check if the circuit meets the specifications generated early. If product requirements are not met, a rework is required. Considering this methodology, the circuit quality depends on three factors: the logic synthesis tool, the physical synthesis tool (place and route), and the cell library (SCOTT, 1994).

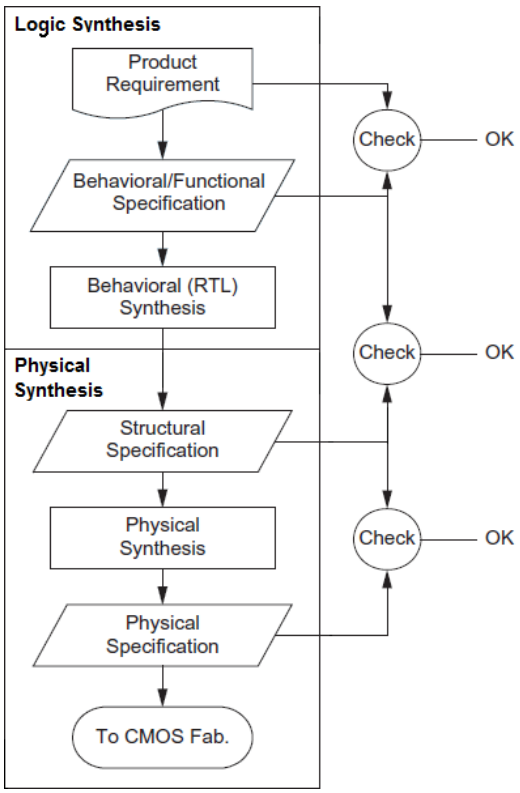


Figure 2.1 – Standard cell design flow (WESTE, 2004).

The logic synthesis process may be subdivided, as illustrated in Figure 2.2. To initial circuit specification are applied technology independent optimizations. Since these optimizations are independent of technology, they occur at the logical level and exploit primarily the concepts of factorization, reduction/rewriting graphs, trees or BDDs, and functional composition/decomposition. Next, the technology mapping step uses the logic gates of a cell library to find the best logic gates combination which meet the constraints of the circuit. In the set of logic gates defined by the technology mapping, new optimizations can be applied, now considering the target technology, in order to generate an optimized network of logic gates. During the complete flow, several verification steps are performed to guarantee the logic correctness of generated circuit and the desired performance. The resulted circuit from this phase is a set of logic gates and their interconnections that are used as starting point in physical synthesis.

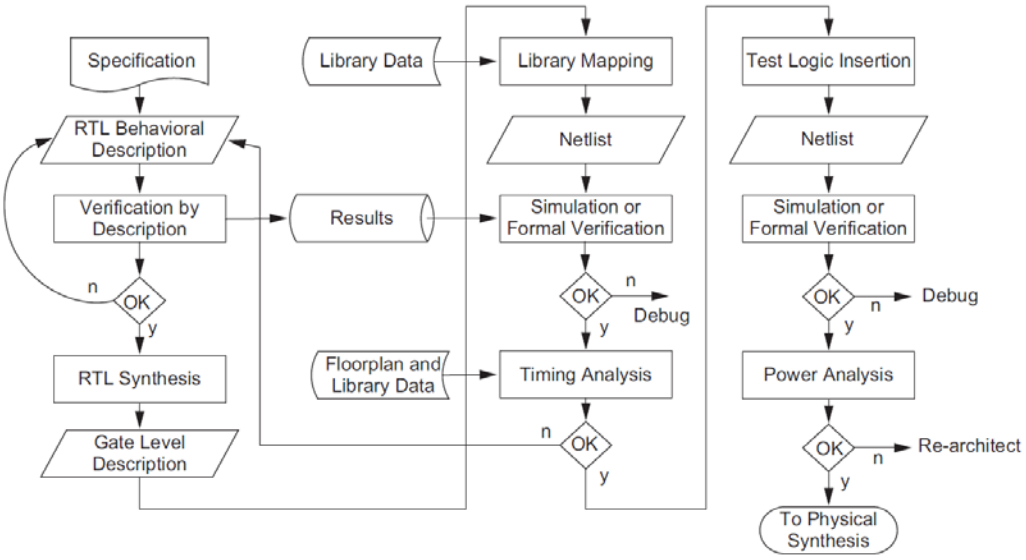


Figure 2.2 – Logic synthesis flow (WESTE, 2004).

The physical synthesis stage may be subdivided as illustrated in Figure . Usually, the first step is named floorplanning and it is responsible to define the position of the high level blocks in the total circuit area. The I/O pads position, power supply and clock network is also defined in such step. The next step is responsible for positioning the gates of each high level block in the circuit area. The signal routing is performed in the following. From this stage, the layout of the circuit is complete. However, to be considered ready, the circuit needs to have their characteristics verified. As in logic synthesis, there are several verification steps that confirm if the designed circuit meets the constraints. On the contrary, any of the above steps can be executed again trying to achieve a better result.

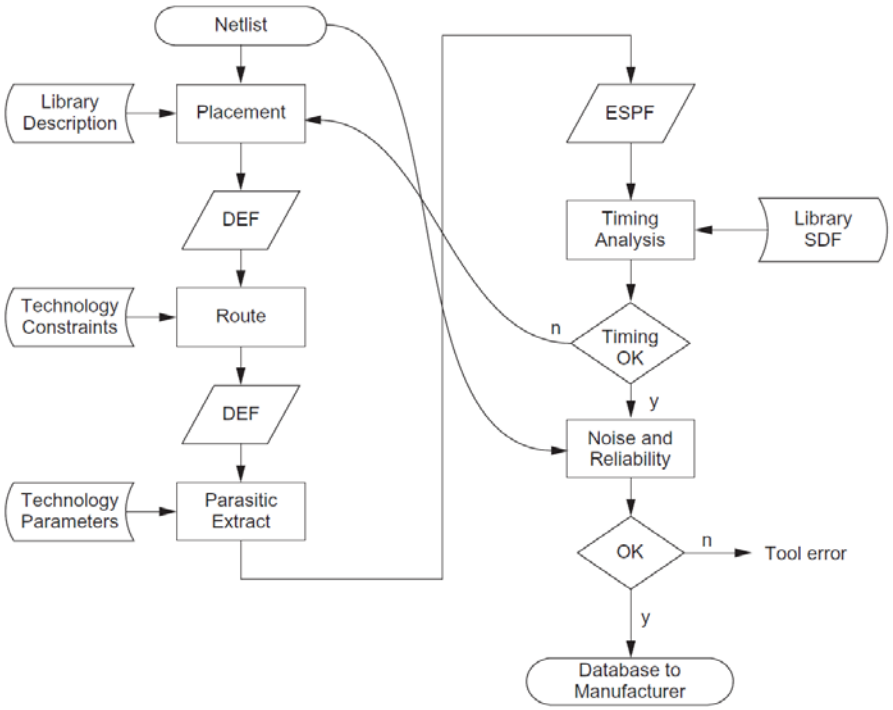
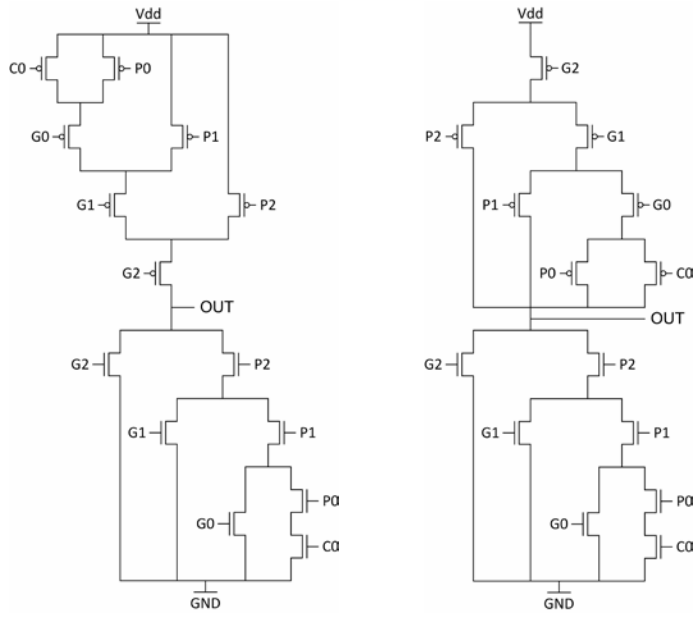


Figure 2.3 – Physical synthesis flow(WESTE, 2004).

As the basic unit used in standard cell methodology is the logic gate, the quality of integrated circuits that are designed using this solution is directly related to the quality of the target standard cell library (SCOTT, 1994). Some aspects that have influence in the quality of a library involves the amount of logic gates, their layout and cell sizing, the sizing variety (drive strength), and the amount of logic function presented in the library. In the literature, there are authors claiming that the best library is the one with few cells (RICCI, 2007), while others support libraries with as many cells as possible (GUAM, 1996), with no consensus on this. Ideally, it is easier to obtain a gate that implement the correct logic function with the appropriate size to achieve the optimal solution for a specific portion of the circuit with a library that contain a higher the number of designed logic functions with several sizing options. However, as more cells are added to the library, more runtime is necessary to technology mapping algorithm and also more time is needed to design, verify and characterize the library.

Disregarding the amount of logic gates, their layout and sizing, another point that can increase the quality of a library is the diversity of transistor arrangement that implement some logic function. Figure 2.4 illustrates two versions of the function "$OUT = !(G_2 + P_2 \cdot (G_1 + P_1 \cdot (G_0 + P_0 \cdot C_0)))$". This function represents the 'generate signal' in a carry lookahead adder (CLA), and will be referred as 'CLA unit' in the rest of the text. Each of these versions has different speed and power consumption characteristics and this difference can be explored by the technology mapping if both versions are presented in the cell library.



(a) **(b)**

Figure 2.4 – Two versions of a CLA unit (OUT = !(G2+P2 · (G1+P1 · (G0+P0 · C0)))).

A variant of the cell-based methodology is the one that explores the automatic cell generation, commonly known as library-free (BERKELLAR, 1998; ABOUZEID, 1992; CORREIA, 2004; MARQUES, 2007). In this variant, it is assumed that the gates can have their layout automatically generated by a tool as they are used by the technology mapping algorithm. In this case, the library contains only the cells that the technology mapping algorithm uses to design the circuit. The main advantage of this approach is that the system is not restricted to a pre-defined amount of logic gates available. With

the possibility to automatically generate any logic gate, the technology mapping algorithm can exploit the diversity of options available to design optimized gates. Such diversity includes both different logic styles and different versions for the same style. Ideally, with the possibility of using any gate at any portion of the circuit, this variant would tend to produce better results when compared to the standard cell design flow presented previously.

One of the major obstacles for the use of library-free concept is the fact that the logic gates in this variant were not previously characterized. Without the characterization values, the technology mapping algorithms that exploit this approach usually use metrics that do not reflect the actual behavior of the logic gate (CORREIA, 2004; MARQUES, 2007). The development of more accurate metrics enables the technology mapping algorithms to reach closer results to the real circuit behavior.

Those metrics are not restricted to timing and power information. The existence of metrics to nanometer effects could also support the design of more robust circuits. The aging effect can be used as example. In traditional approaches, they are treated at post-technology mapping stages of the design flow. One reason for that is the inexistence of data that can be used by the technology mapping algorithm. When properly computed, a metric for the aging effects could be associated with the cost of the logic gate, allowing its analysis in an initial stage of the project. This early treatment can avoid possible re-processes, lowering the total circuit design cost.

2.2 Technology Scaling

The transistor dimension scaling is the main artifice used by the semiconductor industry to increase the performance of the integrated circuits. As mentioned previously, the nanometer devices have more current capability and smaller capacitances than the bigger ones. These two factors contribute to design faster circuits at each advance in technology node. Smaller capacitances also contribute to lower power consumption per operation. Moreover, smaller dimensions also allow the integration of more devices in same silicon area, reducing so the circuit cost and allowing the design of more complex circuit in the die.

The higher transistor density in nanometer circuits produces thermal issues due the higher power consumption per area (HUANG, 2004). The reduction of power supply (V_{dd}) is necessary to deal with power and thermal constrains in the circuit. An inconvenient of such reduced power supply is the lower circuit noise margin and smaller robustness against radiation particles (DRESSENDORFER, 1989). Another consequence of this V_{dd} reduction is the threshold voltage (V_{th}) reduction too. The V_{th} reduction is necessary to keep a good transistor current capacity. This reduced V_{th} increases significantly the transistor subthreshold current, that is one of the main contributors to the static power increasing in nanometer designs (NARENDRA, 2006). Other contributors, such as gate tunneling current and band-to-band tunneling current, have their magnitude increased due to the increment in electric fields presented in transistor structures (ROY, 2003). Although the supply voltage has been reduced, the reduction in transistor dimensions is proportionally higher than the supply voltage scaling, increasing so the electric fields. This increment in electric fields causes also degradation in transistor characteristics during the circuit lifetime. The mechanisms that cause this degradation are called aging effects, that can be also considered as a temporal variation in transistors characteristics (STATHIS, 2003). Moreover, another aspect that

increases as the transistor dimension scaling is the process variation. Since the absolute value of transistor dimensions or doping profile is smaller, any variation in drawing shapes or in dopant profile has higher impact in the transistor parameters. The scenario has become even worse due to the fact that the light wavelength used in lithography process is several times larger than the smallest drawing dimension considered in the technology node (BORAK, 2003). All of those issues have become important design aspects to the performance, area and power consumption of nanoscale IC designs (ORSHANSKY, 2008). Some details related to such undesired effects are discussed in the following.

2.2.1 Static Currents

In past technologies, the magnitude of static currents was low and usually neglected. However, as the devices have been being scaled to achieve higher density, performance, and lower dynamic power consumption, the static power in the nanometer regime is becoming a significant portion of total power dissipation in CMOS circuits, as depicted in Figure 2.5. These currents are responsible for power consumption when the circuit is in idle mode. The fact that several integrated circuits are embedded in portable applications and the basic requirement for this type of equipment is the reduced power consumption, the importance of treating properly static power consumption is quite obvious.

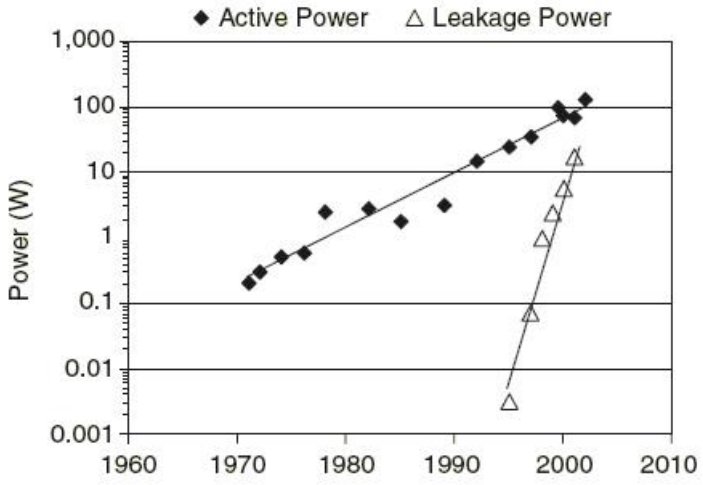


Figure 2.5 – Active (dynamic) and static power consumption in Intel processors (MOORE, 2003).

The reduction of the supply voltage is necessary to maintain, or even decrease, the dynamic power consumption (ROY, 2003; MUKHOPADHYAY, 2006; BUTZEN, 2010; CHENG, 2006; AGARWAL, 2006; ALKABANI, 2008). In order to keep the current capacity of the devices and avoid the aggravation of short channel effects, the transistor threshold voltage and the transistor gate oxide thickness (t_{ox}) have followed the V_{dd} reduction. Due to the same reason, the dopants density has been increased. The changes in these three transistor parameters have resulted in a significant increasing in static currents for every new technology node. Figure shows the two major static currents present in nanometer MOS transistor. Besides subthreshold and gate tunneling currents, there are minor components as the current through the reverse biased pn-junctions (BTBT), the punchthrough current and the gate induced drain leakage (GIDL) (ROY, 2003).

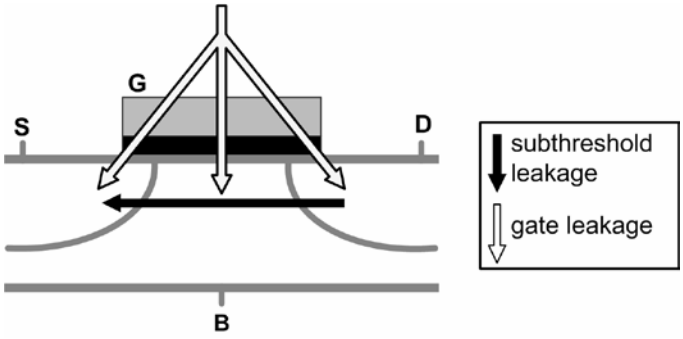


Figure 2.6 – Major static currents in MOS transistor.

Several models and reduction techniques have been proposed and used by industry to address this undesired consumption. Regarding to the reduction techniques, at manufacturing level, the introduction of high-κ dielectric in transistor oxide gate allows a significant reduction in the gate tunneling current (KITTI, 2009). Furthermore, new technologies have transistors with different threshold voltages. This fact is related to the exponential dependence of subthreshold current to V_{th} (KAO, 2000; WEI 1999). Additionally to the techniques that use the dual threshold transistors, the forward and reverse body biasing is also explored (NARENDRA, 2003). The use of sleep transistors to turn off parts of the circuit that are not executing a computation is also explored to reduce the static power. This technique associated to dual threshold transistors is called multi-threshold CMOS (MTCMOS) (MUTOH, 1995). Figure 2.7 illustrates the basic concepts of this approach.

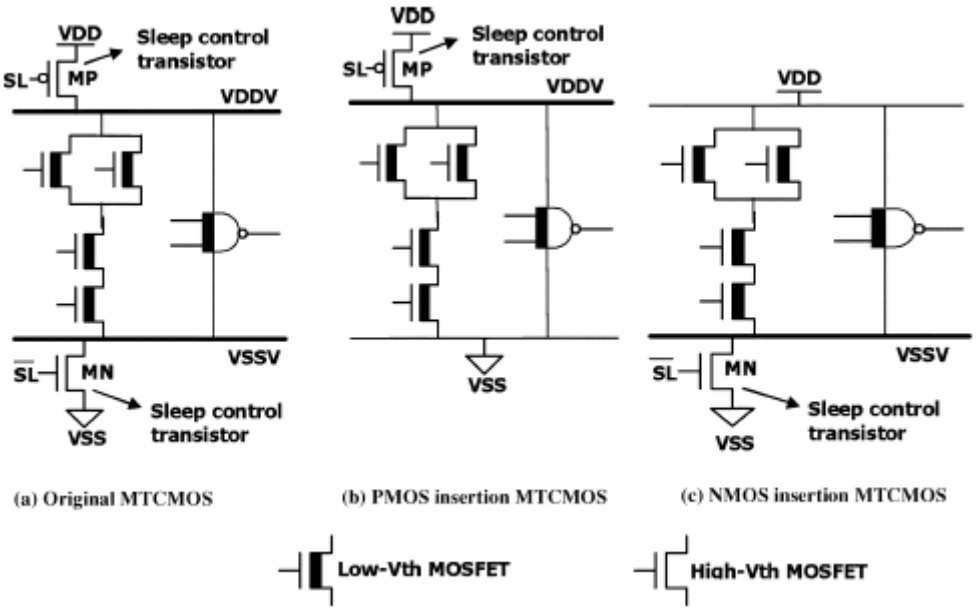


Figure 2.7 – Circuits exploring MTCMOS technique (MUTOH, 1995).

2.2.2 Manufacturing Variability

As the minimum dimensions are reduced, greater is the uncertainty regarding to the effective shape and the effective quantity of atoms which form the devices. Thus, the device characteristics are more sensitive to any slight variations in shape and in amount of atoms that compose it. These variations can be classified as random variations and systematic variations. The random variations are mainly related to the fabrication

process. Random dopant fluctuations (RDF) and line edge roughness (LER) are examples of random variations. The principal way to mitigate this kind of variation is centered in process calibration. There is no solution at design level to deal directly with such variations. Most works evaluate the effect and the impact in device behavior. The systematic variations are mainly related to the lithography process.

Lithography is a key process in the fabrication of integrated circuits. The light wavelength used in this process is directly linked to resolution of the layout. Figure 2.8 illustrates the wavelength used in the technological nodes from 1 µm to 45 nm. According to Figure 2.8, it seems clear that in the processes below 180 nm the resolution of the layout patterns is penalized due to the light wavelength larger than the minimum allowed drawing shape size.

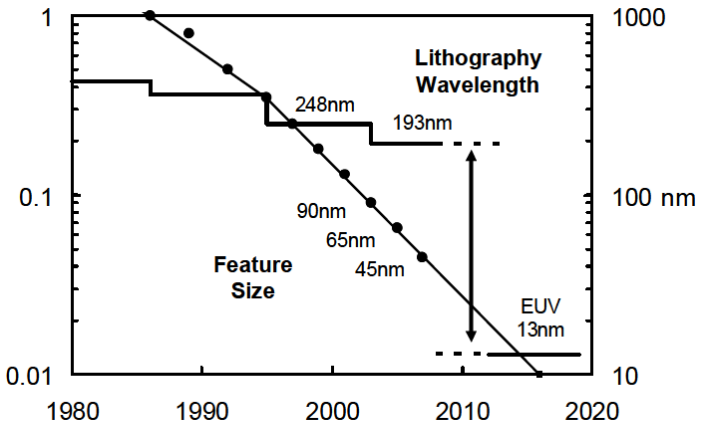


Figure 2.8 – Wavelength versus technology node (SIVAKUMAR, 2006).

Moreover, the affected transistor characteristics can achieve different magnitudes (BORAK, 2003). Figure 2.9 shows the variations in frequency and static power consumption of identical microprocessors produced over the same wafer. While the frequency variation does not reach 40%, the variation in static power consumption is about 20 times. Moreover, environmental variations, such as in temperature and in power supply voltage contribute to add more uncertainty about the circuit behavior. There are several works that explore techniques to minimize the effect of variability in nanoscale ICs (BHUSHAN, 2006; SYLVESTER, 2008; PANG, 2009; AITKEN, 2009).

Several techniques in manufacturing and design levels are used to allow circuits at dimensions smaller than the used wavelength. At process level, two strategies have to be mentioned. The first one is the exploitation of optical concepts to allow the use of a wavelength larger than the printed shape. The second one is the strategy named immersion lithography that improves the process resolution (MACK, 2006, FRENCH 2007). At design level, the techniques are centered in layout optimization. Restrictive design rules (RDR) are being used to mitigate the systematic variations (JHAVERI, 2010). As the own name suggests, this set of design rules is more restrictive than the traditional one. Example of restrictions is the rules that allow layers in only one direction with equally spacing between them. Figure 2.10 illustrates the layout of a logic gate designed considering traditional approach and considering restrictive design rules.

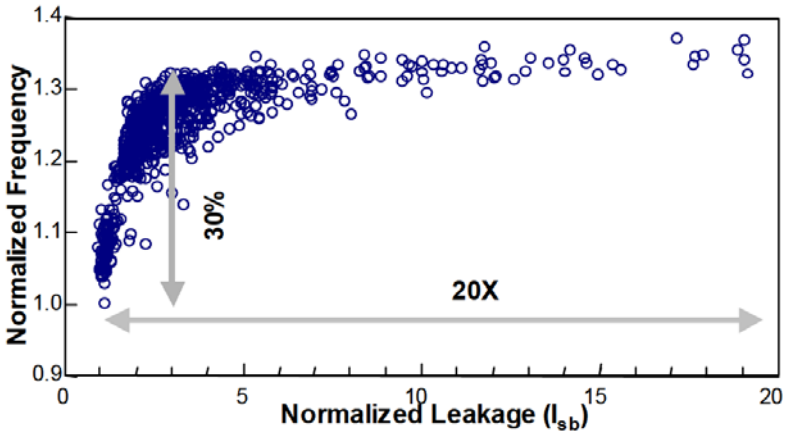
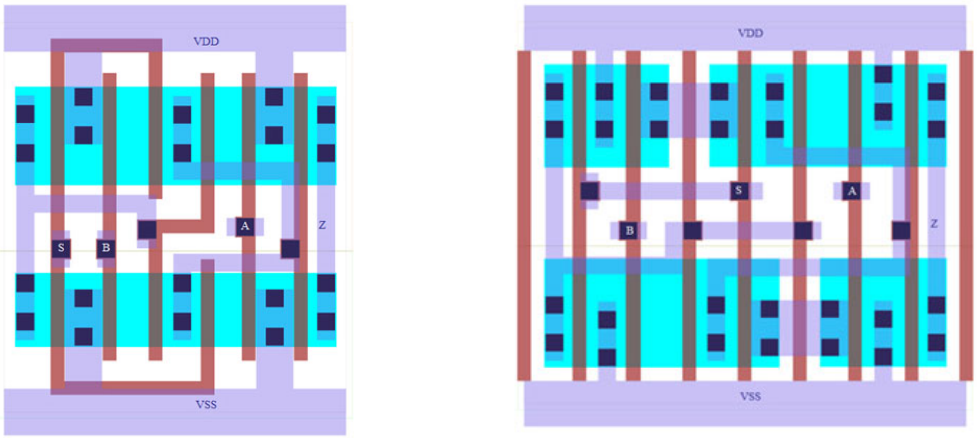


Figure 2.9 – Frequency and static power variations of microprocessors in a wafer (BORAK, 2003).



(a) **(b)**

Figure 2.10 – CMOS gate layout considering conventional (a) and restrictive (b) design rules (PALLISGAARD, 2012).

There are also several techniques that exploit post-layout processing. These techniques explore the drawing-printed shapes relationship to improve the final layout resolution. Such techniques are named resolution enhancement techniques (RET) (WONG, 2001). For instance, the technique called optical proximity correction (OPC) applies some distortions in original layout with the objective to achieve the expected final form. Figure 2.11 illustrates the objective and solutions presented by this technique for a simple layout. Other techniques, such as phase-shift mask and double patterning, are also used in the context of RET (JHAVERI, 2010). In addition to the approaches discussed above, the evaluation of variability robustness in different transistor arrangements can also be explored as a solution to mitigate variability (SILVA, 2009). This approach can provide important data to help the standard cell design flow, especially the mapping algorithm, in generating circuits with lower variability.

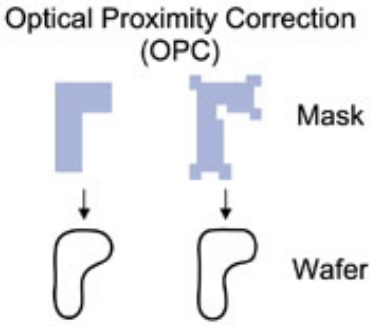


Figure 2.11 – Original and post-processed OPC layout and printed shapes (MACK, 2006).

2.2.3 Radiation

Radiation effects are related to the incidence of ions and particles in the integrated circuits (DRESSENDORFER, 1989). The main transient effect caused by these particles is a momentary voltage and current value change in transistors terminals. The perturbation magnitude and duration is proportional to the energy of the incident particle and the amount of charges stored in transistor structured. According to the incident region or the perturbation propagation, a bit flip can occurs, resulting in a wrong system computation.

Each new technology generation present a scaling in transistor dimensions. This dimension scaling is directly related to the reduction in the number of atoms that make up device structure. The reduction of the supply voltage reflects in small circuit noise margins. These two factors are responsible to nanometer circuits being more vulnerable to the effects of energy particles that reach it. In other words, voltage fluctuations that were caused only by high-energy particles in micrometer processes, in nanometric circuits they are caused by particles of average power, increasing significantly the occurrence of failures due to radiation (JOHNSTON, 2000).

Figure 2.12 illustrates the incidence of an energy particle in MOS transistor. When a particle strikes an IC, it produces a large population of electron-hole pairs. Since electrons present a higher mobility than holes, electrons are collected towards higher potentials present on the IC bulk, which generates a fast current transient. If the stricken IC area is the reverse-biased depletion region of a transistor, and if this transient is large enough, the perturbation may result in the loss of the stored information (i.e., a bit flip).

The effects caused by radiation can be divided into cumulative effects, called total ionizing dose (TID), and transient effects, known as single events effects (SEEs) (LABEL, 2000). TID consists in accumulation of charges over time in nsulating layers, provoking leakage current increase and transistor transistor threshold voltage shifts. This effect causes degradation in transistor parameters. This degradation is permanent, but it usually takes a long time to cause a functional failure in the circuit. It is also being mitigated with the scaling due to the small dimensions of transistor structures (LABEL, 2000). SEEs, in turn, are also classified according to the location affected by the radiation particle.

Single event effects are generally characterized by a voltage variation at a transistor node caused by a particle impact in that device terminal. As mentioned before, the perturbation magnitude and duration are proportional to the particle energy value. In extreme cases, these events may have enough energy to cause a permanent failure (i.e.,

hard SEEs), or even cause the device destruction (i.e., destructive SEEs) (LABEL, 2000).

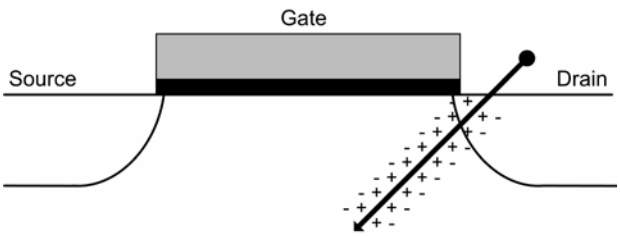


Figure 2.12 – Incidence of an energized particle in MOS transistor.

The radiation effects that cause transient faults (i.e., soft SEEs) are classified according to the affected location. When the node reached by a particle is a storage element and the particle has enough energy to provoke a bit flip in that element, the effect is known as single event upset (SEU). The other case is when the particle hits the combinational logic blocks. In this case, the effect is called single event transient (SET). The voltage perturbation from a SET is usually logically or electrically masked. An indirect SEU occurs when the voltage perturbation from a SET is propagated to a storage element. The computation error is characterized when occurs a bit flip in the storage unit (MASSENGILL, 2000).

As the vulnerability of circuits against radiation effects increases in new technology processes, the use of techniques that produce radiation robust circuits become more important. There are techniques at all levels of abstraction, from the algorithmic level to the process level. At process level, the use of silicon-on-insulator (SOI) can be pointed out. At physical level, several layout solutions are proposed (COLINGE, 2001). At gate level, it can be highlighted works that explore the logical and electrical masking, as well as the robustness of the network of transistors compared to the propagation of the effect of radiation (NICOLAIDIS, 1999).

From architectural to algorithmic level, the redundancy is explored. Techniques as triple modular redundancy (TMR), time redundancy (TR), parity, error detection and correction (EDAC), can be explored (NICOLAIDIS, 1999; PETERSON, 1980). The concept is the use of redundancy to be able to detect the correct computation by comparing experimental results.

Figure 2.13 illustrates the TMR, where there are three instantiations of the same circuit and a voter that computes the correct result. All these techniques introduce significant area overhead and performance penalty.

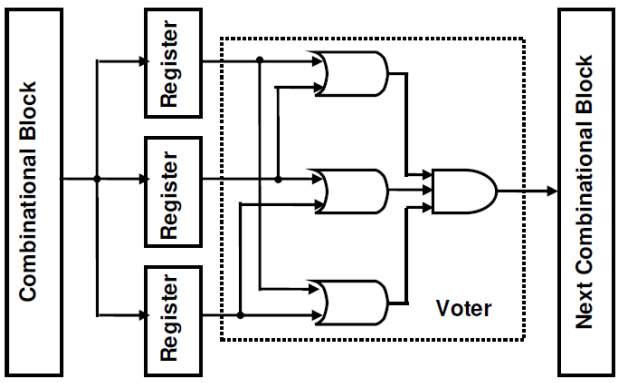


Figure 2.13 – TMR architecture (BASTOS, 2006).

2.2.4 Aging Effects

The transistor scaling is responsible for a significant improvement in circuit performance in each new technology generation. The reduced dimensions increase the electric fields across the device structures. These higher electric fields are the main responsible for the increased device characteristics degradation over time. Effects such as time dependent dielectric breakdown (TDDB), negative bias temperature instability (NBTI) and hot carrier injection (HCI) have become important parameters to be taken into account in circuits designed in nanometer technologies. Considering that the transistor dimensions continue scaling, and consequently the electric fields in transistor structure continue increasing, the importance of treating such wearout mechanisms in the new technology nodes is increasing since they may cause important losses in timing performance, increasing also power consumption and ultimately, functional errors in the system computation (WANG, 2007; VATTIKONDA, 2006; CHEN, 2003; TAKEDA, 1995; TONG, 2009; NIGAM, 2009).

The metal-oxide-semiconductor structure that characterizes the MOS devices can be considered the most vital transistor structure (STATHIS, 2003). Ideally, the gate oxide should be a ‘perfect’ insulator. However, some defects are presented in the crystal structure since the oxide growth in the manufacturing process. The transistor is characterized with these defects and the effect of their existence is computed in this characterization. During the transistor operation, some new defects are created in the MOS structure, degrading the device characteristics. As the oxide is getting thinner, the electric field across it is getting more intense. The same occurs with the gate length scaling and the increment of the electric field across the channel. These higher electric fields increase the defect generation tax and increase the importance of treating these wearout mechanisms.

The defects created by the wearout mechanisms in the oxide structure results in penalties on timing and power performance of the circuit. The degradation caused by each aging effect involves in general more than one physical mechanism. However, each effect has its degradation behavior well defined. Also, the affected transistor characteristic is well known. TDDB and NBTI are static degradation effects, while HCI acts when the transistor is switching. TDDB effect creates traps at gate oxide when a high electric field is presented across the oxide. This traps creation compromise the isolation oxide characteristic, increasing the gate tunneling current. At extreme cases, a conductive path through the oxide can be created and the transistor operation is compromised (TONG, 2009). Figure 2.14 illustrates the defects and the conductive path created by TDDB in a gate transistor oxide. Moreover, NBTI generates traps in the interface between the gate oxide and the substrate. This effect occurs in PMOS transistor at the presence of a high electric field. It happens when the transistors are negative biased. This interface traps degrade the transistor threshold voltage, impacting the transistor maximum current capability and the circuit speed. When the electric field is not presented, some threshold voltage recovery is verified (WANG, 2007). Figure 2.15 illustrates the dynamic behavior of NBTI effect. On the other hand, as discussed before, HCI acts when the transistor is switching. Some carriers that are flowing in the channel gain enough energy and are injected into the gate oxide near to the drain terminal. Figure 2.16 illustrates this carrier injection. This degradation is also reflected in transistor threshold voltage and, consequently, in the circuit timing characteristics (TAKEDA, 1995).

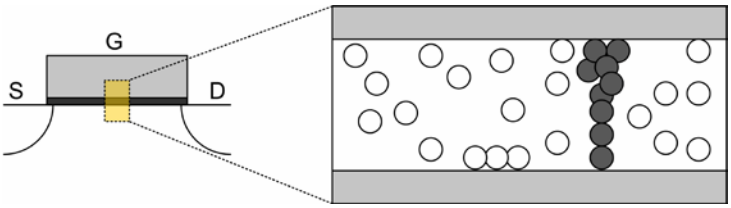


Figure 2.14 – Traps and conductive path in the gate oxide due to TDDB effect.

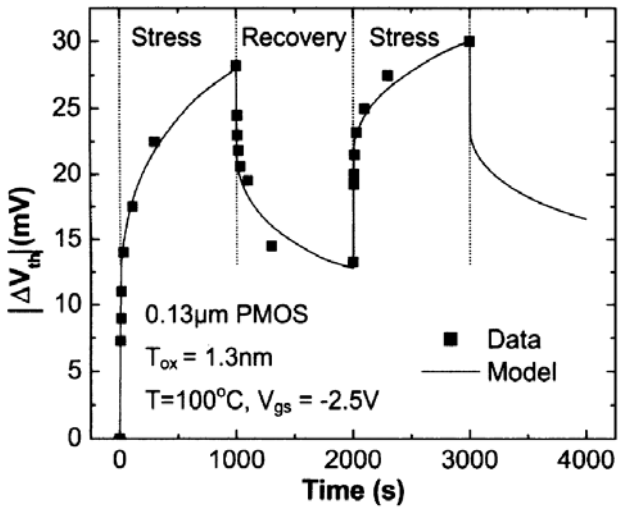


Figure 2.15 – Stress and recovery behavior of NBTI (VATTIKONDA, 2006).

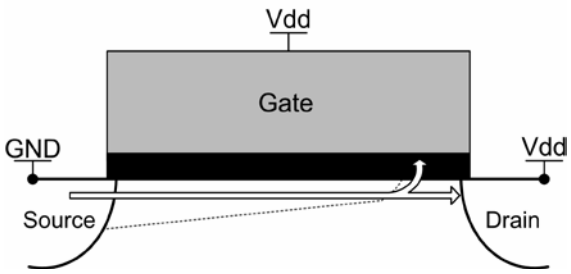


Figure 2.16 – Carriers injection into the oxide due to HCI.

The techniques that deal with the mitigation of aging effects degradation explore the interaction between both, manufacturing and design solutions. As TDDB effect has a clear transistor bias degradation, design techniques look for the transistor with higher transistor bias degradation probabilities in order to replace them by transistor with ticker gate oxide, being this kind of device available at the fabrication process. This solution can cause timing penalty whether the transistors belong to the critical paths (STATHIS, 2003). The HCI effect is related to the channel current flow. Due to the output capacitance, the transistors connected to the output node experience high HCI degradation at every switching activity. Based on that, transistors with higher switching activity are placed far from output logic gate nodes (TAKEDA, 1995). Since NBTI has stress and recovery phases, some input vector control techniques try to maximize the recovery time to mitigate the transistor threshold voltage degradation (VATTIKONDA, 2006).

The aging effects are in the center of this work. More details related to the principal characteristics of each effect and some related works presented in the literature are discussed in the following chapters.

3 AGING EFFECTS

The shrinking in critical transistor dimensions to nanometer ranges and the increasing substrate doping densities result in a significant increase of electric fields through the channel region and across the gate oxide of MOS transistors. These high electric fields act in several ways changing the transistor characteristics during its lifetime. The physical mechanisms of three aging effects and respective analytical models are discussed in the following sections.

3.1 Hot Carrier Injection

The hot carrier injection (HCI) phenomenon is been a reliability issue in MOS circuits since the 1970s. It can be considered as one of the aging effects more studied and treated in the literature. In summary, due to the lateral electric field, carriers that are travelling in the channel gain enough energy to break the energy barriers being injected into the gate oxide, breaking so an interface state. This process results in a shift in threshold voltage, in the transconductance degradation, and in decreasing of the transistor drain current drive capability. Physical details and models are briefly reviewed bellow.

3.1.1 HCI Physical Mechanism

The classic theory behind the HCI effect involves the high lateral electric field in MOS transistor when the device is biased under saturation conditions. This high lateral electric field produces energetic carriers near to the transistor drain region. These carriers are called hot carriers because they have higher energy than the thermal energy of surrounding lattice. Part of this carriers produce substrate current that can lead to a latch up in CMOS structures (MATSUNAGA, 1980). However, the most important aspect for long-term reliability is those carriers that acquire sufficient energy to overcome the energetic barrier and get injected into the gate oxide, breaking an interface state (CHENG, 1985). The higher mobility of electrons makes the HCI degradation impact worse in NMOS transistors than in PMOS transistors (ROY, 2005). The carrier generation in NMOS transistor due to HCI and the intensity of the lateral electric field across the transistor channel are illustrated in Figure 3.1.

The damages caused by the carriers that are injected into the gate oxide may result in a permanently change in device characteristics, such as the drain current capability, threshold voltage and transcondutance. This oxide damage induces gradual degradation over the time and can lead to long-term circuit performance degradation and malfunctioning. As technology scaling, the supply voltage (V_{dd}) has to be also scaled down. From the reduction in supply voltage, the HCI impact in device parameters was expected to decrease, becoming an insignificant effect. However, this behavior has not

been verified through experimental results for nanoscale technologies. In fact, the HCI degradation has not vanished for MOS operating at lower supply voltages, but remains significant and is also projected to get worse in future technology generations (KUFLUOGLU, 2007).

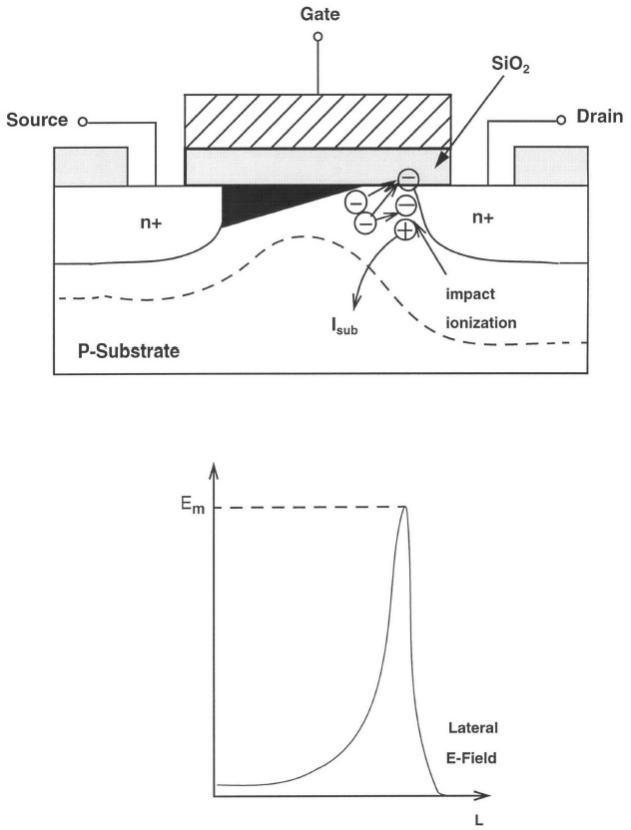


Figure 3.1 – Illustration of hot-carrier generation in NMOS transistor, and the lateral electric field in the channel (JIANG, 1998).

New theories have been introduced to explain the physical mechanisms involved in hot carrier degradation in scaling devices at low supply voltage (RAUCH. 2005). Three distinct regimes have been suggested to describe the physics involved in the transistor degradation. They representation of the lifetime degradation is proposed as function of the transistor drain current. The relations described below consider that for a fixed drain voltage (V_d), the drain current is increased with gate voltage (V_g), whereas the energy is lowered (GUERIN, 2007).

The first regime considers a low drain current (low V_g, high energy). In this situation, the lifetime shows to be linearly dependent to the drain current. The generated hot carriers are attracted to the interface due to the electric field with sufficient energy to break interface state.

The second degradation mode considers a medium drain current (medium V_g and energy). In this current stage, the lifetime degradation has a quadratic behavior. In this regime, the carriers are induced by impact ionization. Most of them have not enough energy to break interface bonds. However, some carriers achieve higher energy level through carrier-to-carrier interactions. In this case, these high energy carriers are able to break the bonds.

The third (and last) regime considers high drain current (high V_g and low energy). This degradation mode presents a cubic but dispersive behavior. The transition between quadratic to cubic behavior is explained by the transition from a bulk-dominated current at medium V_g to a surface-dominated current at high V_g. The carriers in this mode do not get enough energy to break a bond by a single excitation. At this regime, the carrier density close to the interface strongly increases. Considering that several carriers are required to lower the energy needed to generate an interface state, the high carrier density favors the low energy interaction between carriers and bonds.

From this last perspective, the impact of traditional channel hot carriers (CHC) and also the impact of phenomenon presented in nanometer technologies, such as cold carriers (CCC) and non-conductive hot carriers (NCHC), are considered.

3.1.2 HCI Long Term Analytical Model

As mentioned previously, the HCI effect was exhaustively explored for micrometric technologies from the 1980s to the 1990s. During this time, several analytical models have been presented in the literature (TAKEDA, 1983; TAM, 1984; HU, 1985; GROESENEKEN, 1995).

One of the most accepted model, and largely used by the industry and academic community, explores the classic relation between HCI degradation and the lateral electric field presented in transistor channel. The lucky electron model (LEM) explores the field driven approach (TAM, 1984; HU, 1985). In this scope, the damage caused by HCI is related to the interface state generation (N_{it}). This interface states are directly linked to threshold voltage degradation. The model relates the HCI degradation to the electric field at the drain (E_m), to the drain to source current (I_{ds}), and to the stress time (t) in a simple power law relationship, as presented in the following (GROESENEKEN, 1995):

$$\Delta N_{it} = C_1 \left[\frac{I_{ds}}{W} \cdot \exp\left(-\frac{\Phi_{it,e}}{q \cdot \lambda_e \cdot E_m} \right) \cdot t \right]^n \tag{3.1}$$

where W is the channel width, $\Phi_{it,e}$ is the critical energy for electrons create an interface state, λ_e is the hot-electron mean free path, C_1 is a technology dependent constant, and n is widely accepted to be 0.5.

However, the LEM does not consider the importance of low energy carriers in nanometer technologies. The new energy driven theory, summarized in previous section, has been introduced to explain the carrier degradation mechanisms for nanometric devices operating at low supply voltages. The energy-driven model explores the carriers behavior at various energy levels, ranging from high-energy hot carriers to low-energy cold carriers. The model provides the device lifetime (τ) as presented in the following (BRAVAIX, 2009):

$$\frac{1}{\tau} = C_1 \cdot \left(\frac{I_{ds}}{W} \right)^{a_1} \cdot \left(\frac{I_{bs}}{I_{ds}} \right)^{m} + C_2 \cdot \left(\frac{I_{ds}}{W} \right)^{a_2} \cdot \left(\frac{I_{bs}}{I_{ds}} \right)^{m} + C_3 \cdot V_{ds}^{a3/2} \cdot \left(\frac{Ids}{W} \right)^{a_3} \cdot \exp\left(\frac{-E_{emi}}{K_B \cdot T} \right) \tag{3.2}$$

where C_1, C_2, C_3 are three technology parameters determined by their dominant mode, i.e., high, medium and low energy modes, respectively. E_{emi} is the activation energy. The parameters m, a_1, a_2, a_3 are extracted from experimental data. More details can be obtained in (BRAVAIX, 2009).

The terms in Equation (3.2) correspond to the high, medium and low energy modes, described in previous section, and present excellent fit with experimental results. However, for a design point-of-view, the previous model is not practical. Although hot carrier injection is a cumulative effect in nature, the previous approaches turn too complex the analysis of dynamic degradation involved in circuit normal operation conditions. A long term cumulative model is required to obtain practical estimative of the transistor degradation over a long period of time. A simple empirical model that captures the long term V_{th} transistor degradation is expressed by (TAKEDA, 1983):

$$\Delta V_{th} = A \cdot t^{n} \tag{3.3}$$

where, A is a technology dependent constant related to the number of carriers generated by impact ionization, t is time, and n reflect the most severe hot carrier mechanism. This model is still valid, and it is also being used to capture transistor aging-induced variability (MAGNONE, 2011).

During digital circuit operation, the transistor is not under degradation all the time. In fact, the transistor suffers HCI degradation only when its input is switching (HUARD, 2007). Also, the more severe degradation occurs in transistors with maximum drain-to-source voltage (GUERIN, 2008). Hence, a derived close form expression for V_{th} degradation due to HCI can be given by:

$$\Delta V_{th} = A \cdot \left(TSwP \cdot t\right)^{n} \tag{3.4}$$

Similar to the approach proposed in (TAKEDA, 1983), the proposed solution considers a specific technology node and a given set of environmental conditions, that are important to obtain the technology dependent constants A and n. To capture the switching activity, the degradation is expressed as a function of the transistor switching probability (*TSwP*).

3.2 Negative Bias Temperature Instability

Negative bias temperature instability (NBTI) is a degradation phenomenon occurring mainly in PMOS transistor, investigated since the late 1960s. Even though the exact degradation causes are not well understood yet, it is now commonly admitted that under a constant negative gate voltage bias and elevated temperature a built up of interface traps and positive charges occur either at the oxide-substrate interface and in the oxide layer (HUARD, 2006; GRASSER, 2011). PMOS transistors are mostly affected, since these devices are negatively biased when they are conducting. NBTI effect increases the PMOS transistor threshold voltage (V_{th}) over time, reducing the device drive current and circuit speed (PAUL, 2006).

3.2.1 NBTI Physical Mechanism

There is a constant effort during last decade to advance in the comprehension of NBTI degradation. Several experiments with different characterization methodologies and stress conditions have been used to try to identify the physical mechanisms lying behind the NBTI degradation. It can be considered a consensus that NBTI degradation results from the superposition of many individual processes. Although there is no single physical mechanism that is comprehensive enough to explain all the behaviors related to the NBTI phenomenon, two solutions are the most accepted. Those solutions are

proposed considering experimental data extracted from characterization circuits (DENAIS, 2004; SHEN, 2006; KARL, 2008; KEANE, 2010).

An initial approach to deal with NBTI behavior was proposed in 1977, and consists in a hydrogen-diffusion controlled interface state creation mechanism (JEPPSON, 1977). This reaction diffusion theory has been the bulk of the literature for several years. From this theory, it is arguably believed that the increase of V_{th} due NBTI is caused by broken Si-H or Si-H_2 bonds. These broken bonds are induced by the electric field generated by the positive holes from the PMOS transistor channel and the voltage applied to the transistor gate. H atoms diffuse away to the oxide, creating positive interface traps, which cause the increasing in V_{th}. Each new experimental measurement reveals new details related to NBTI degradation behavior, and the reaction-diffusion theory has been reviewed and adapted (STATIS, 2005; ALAM, 2007).

However, some experiments over new technologies have suggested that the hydrogen diffusion was dispersive (KACZER, 2005; GRASSER, 2008). From this perspective, the interface traps creation is not the sole source of NBTI degradation but a second mechanism also contribute to the V_{th} increment. This second approach is based on the hole trapping/detrapping theory. This mechanism involved in V_{th} increment can be described by tunneling of channel carriers into oxide defects induced by the electric field through the gate oxide when the PMOS transistor is negative biased. The oxide defects can either pre-exist in the transistor structure or be created by electrical stress. Transistors with high-κ dielectric have higher density of pre-existing defects. From this point-of-view, hole trapping/detrapping is becoming the dominant contributor to NBTI degradation (KACZER, 2010).

Another important characteristic involved in NBTI effect is its dynamic behavior. There are two phases of NBTI for a PMOS transistor behavior depending on its bias condition. The first phase is usually referred as “stress”. In this phase occurs the device degradation. It occurs when the transistor is negative biasing, the gate voltage V_g = ‘0’ and drain-to-source voltage V_{gs} = ‘-V_{dd}’. An elevated electric field is experience through the gate oxide with this bias condition. From reaction diffusion mechanism, positive interface traps are accumulating over the stress time with H diffusing towards the gate. The hole trapping are associated to the carrier tunneling injection and trapping in gate oxide. The second phase is usually referred as “recovery”. The PMOS bias condition on this phase are V_g = ‘V_{dd}’, and V_{gs} = ‘0’. The electric field is no more present through the gate oxide, and no new interface traps are generated or carriers are tunneling. Instead, the carriers trapped in the oxide are emitted back to the substrate and the H diffuses back and recomposes the broken Si-H or Si-H_2 interface bonds. Figure 2.5 illustrates the NBTI dynamic behavior.

The NBTI dynamic behavior allows the decomposition of NBTI degradation in two different components. The first component is defined as permanent or universal degradation, and the other one is a non-universal or recoverable degradation (HUARD, 2006; ISLAM, 2011). The permanent degradation is associated to the interface defect generation, while the hole trapping is associated to the non-universal component. This approach is consistently explained using the reaction-diffusion theory as the universal slow mechanism and the hole trapping as the non-universal fast mechanism. From this approach, the hole trapping is at the origin of the strong recovery effect and the reaction diffusion reflect the long term degradation.

Those efforts in understanding the theory behind NBTI effect and developing models to estimate the degradation have to be supported by practical measurements in order to be effective. Those techniques usually use specialized equipment to access individual devices or explore the concept of on-chip monitors that are capable to measure some parameter which reflects the degradation (DENAIS, 2004; SHEN, 2006; KARL, 2008; KEANE, 2010). Since NBTI degradation is perceptible in long period of time (usually years), the degradation is usually accelerated by raising the power supply (V_{dd}) (KIM, 2008). To correlate the accelerate measurements to real behavior is another challenge involved in this process. The sensors have also to be able to measure the static and dynamic behaviors. Furthermore, the measurements should explore a range of stress voltages, temperatures and time. The characterization methodologies are in constant investigation, and they are the most responsible to the advance in NBTI comprehension (HUARD, 2006).

3.2.2 NBTI Long Term Analytical Model

NBTI degradation models are based on the physical mechanism theory previously discussed and on the experimental data findings. From a historical perspective, the dynamic behavior of NBTI degradation is the main challenge related to NBTI models. It is inherently complicated since NBTI exhibits the unique property of both stress and recovery behavior during circuit dynamic operation. The dynamic models based on the reaction diffusion theory explore the number of interface traps to obtain the V_{th} degradation (ALLAM, 2005; VATTIKONDA, 2006; ALAM, 2007). The models that explore hole trapping/detrapping theory use the holes trapped into oxide defects to estimate the V_{th} change (GRASSER, 2011). The following equation has been proposed in (ISLAM, 2011), and it is one of the models that explore both theories to obtain the V_{th} degradation (ΔV_{th}), as expressed by:

$$\Delta V_{th} = \Delta V_{IT} + \Delta V_{HT} + \Delta V_{OT} \tag{3.5}$$

where ΔV_{IT}, ΔV_{HT}, and ΔV_{OT} refer to the contributions to ΔV_{th} from interface traps, pre-existing oxide defects, and electrical generated oxide defects, respectively. ΔV_{IT}, ΔV_{HT}, and ΔV_{OT} basis can be obtained in (ISLAM, 2011).

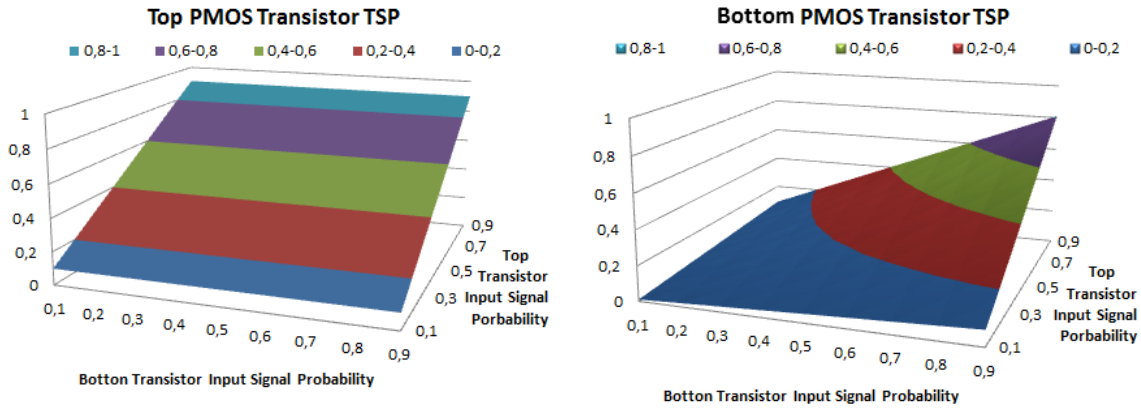
The NBTI dynamic degradation models estimate accurately the V_{th} degradation from cycle to cycle. However, under regular operating conditions, the V_{th} degradation due to NBTI is perceptible in a long term, e.g. over a few years. Considering long term prediction, that is the focus of this work, it is unpractical to run cycle to cycle simulation for the estimation of transistor degradation. Hence, a derived close form expression for V_{th} degradation that considers a specific technology node and a given set of environmental conditions could be expressed by:

$$\Delta V_{th\_NBTI} = A.(TSP.t)^n \tag{3.6}$$

where A is a technology dependent constant, t is time, and n is the NBTI time exponential constant. *TSP* is defined as the probability of PMOS transistor in negative biasing. It is a function of the input signal probability and the position of the transistor in the arrangement (BUTZEN, 2010). A procedure to obtain the *TSP* from any transistor netlist is presented in Chapter 5.

The used model is derived by the one proposed in (WANG, 2007). The main difference is in the *TSP* term. (WANG, 2007) uses the input signal probability instead of TSP. The motivation to use TSP instead only input signal probability is to explore the

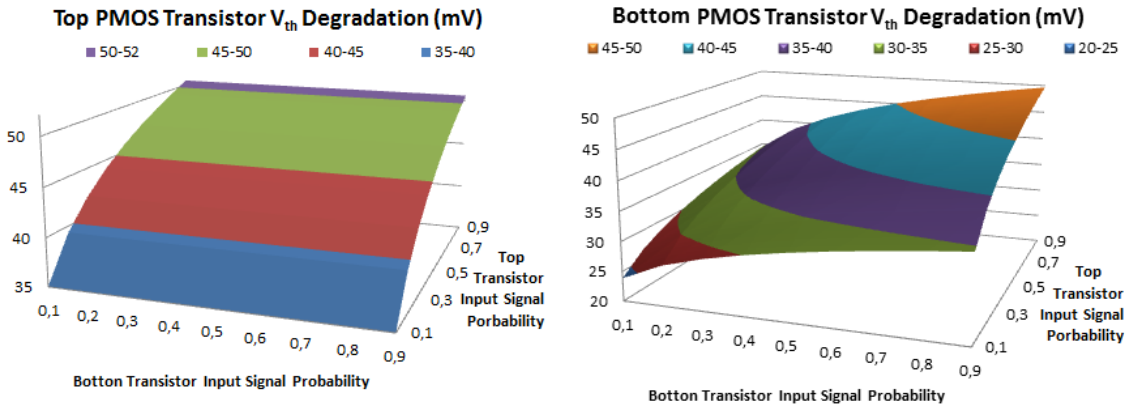
influence of the transistor position in the arrangement. The plots depicted in Figure 3.2 illustrate the *TSP* of the top and bottom transistor that are present in the pull-up stack of a NOR gate, according to input signal probabilities. The top transistor in the stack, i.e. the one connected to the power supply, has its degradation condition controlled only by its input signal. The bottom transistor has to consider the combination of both input signal probabilities (KUMAR, 2007).



(a) **(b)**

Figure 3.2 – Transistor stress probability (TSP) for two stacked PMOS transistor of a NOR gate: (a) top transistor (connected to power supply); (b) bottom transistor (connected to output node).

Figure 3.3 presents the V_{th} degradation results for the two stacked PMOS transistors of a NOR gate. The data illustrated in the plots consider a maximum V_{th} degradation of 50 mV, the probabilities presented in Figure 3.2 and the technology dependent parameters applying the values used in (WANG, 2007): $A = 3.9 \times 10^{-3}$ and $n = 1/6$. From the plots is possible to verify the model fidelity from the experimental data reported in the literature (DENAIS, 2004; SHEN, 2006; KARL, 2008; KEANE, 2010). The importance of considering TSP instead of only input signal probabilities are also evident. If only input signal were considered, the plots might have the same behavior. However, the difference between both plots achieves 47% in the worst case.



(a) **(b)**

Figure 3.3 – Vth degradation of two stacked PMOS transistor of NOR gate according to long-term model presented in Equation (3.6) and the TSP values illustrated in Figure 3.2.

3.3 Time Dependent Dielectric Breakdown

Another reliability issue in nanoscaled devices is the time dielectric dependent breakdown (TDDB). This mechanism degrades the isolation properties of gate dielectric, increasing the tunneling current across the transistor gate terminal. TDDB is an increasing concern in digital circuit design as gate dielectric thickness is scaling down and the supply voltage does not follow that aggressive scaling. The result is an increasing in the electric field through the gate oxide for every new technology node, causing a large TDDB degradation. The following sections review the physical concepts behind TDDB and present a long term analytical model that will be used in this work.

3.3.1 TDDB Physical Mechanism

Although the TDDB effect has been studied for decades, many of the physical details behind TDDB are still under debate. However, there is a general consensus that the large electric field across the transistor gate oxide is the direct cause of TDDB.

A simple physical explanation is that in the presence of a large electric field across the gate oxide, defects are eventually formed into the oxide structure. These defects are usually created by charges that pass through the oxide. Ideally, no charge should pass through the oxide. However, thin oxide and large electric fields make this usual. The large electric fields through the oxide lead to several quantum tunneling effects. Fowler-Nordeim tunneling can be considered as the main physical mechanism that causes the time dependent dielectric breakdown.

In Fowler-Nordheim tunneling phenomenon, electrons in the conduction band of a conductor can acquire enough energy to jump the oxide barrier, penetrating into the oxide conduction band. This is a rare occurrence at low electric fields, but, as the electric field increases, the rate of this injection increases rapidly. The Fowler-Nordheim tunneling presents exponential dependence to voltage. As the gate thickness scaling, new effects such as direct tunneling pass to contribute to TDDB degradation. In this process, the electrons penetrate through the gate directly to the channel. In this process, tunneling increases exponentially with the decrease of oxide thickness (TAROG, 2010).

The breakdown behavior of each new CMOS process should be thoroughly captured during the process characterization phase in order to obtain a detailed understanding of technology reliability. In this sense, the theory involved in any aging effect is strongly based on experimental data extracted from dedicated characterization circuits (KEANE, 2011). The characterization methods used to measure the useful lifetime of thin dielectrics usually performs the characterization in arrays of overstressed devices for a short period of time. The time to fail for device is captured and the data is analyzed considering the correlation to typical operation conditions. These characterization methodologies usually explore several TDDB dependencies. The most common are gate voltage and oxide thickness, temperature, device area, and dielectric materials (KEANE, 2011).

These characterization procedures have been important to identify peculiarities of TDDB in thin oxides. The generated defects compromise the oxide isolation characteristic and lead to an increment in tunneling currents through the oxide. This tunneling current, associated to the large electric field, further degrade the oxide, leading to the formation of more oxide defects that culminate with the oxide breakdown. The gate tunneling current behavior in the presence of TDDB effect is

illustrated in Figure 3.4. It is well illustrated that in thin oxides the transistor suffers a gradual degradation during its lifetime before achieving a condition known as hard breakdown (HBD). The first gate tunneling current change is defined as soft breakdown (SBD). The gradual degradation between the SBD and the HDB is defined as progressive breakdown (PBD) (MONSIEUR, 2002, LINDER, 2002).

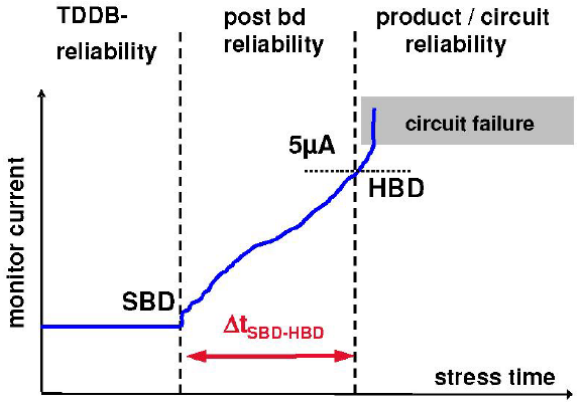


Figure 3.4 – Transient change of gate current showing SBD, PBD and HBD (KERBER, 2007).

During the progressive breakdown, the device is still functional but the system power dissipation and delay characteristic are compromised. Studies have revealed that the rate of trap formation increases as the permittivity of the dielectric increases (NIGAM, 2009). With the introduction of high-κ gate dielectrics, the probability of having a SBD, and consequently the PDB, during the device lifetime has increased substantially (CHOUDHURY, 2010).

3.3.2 TDDB Long Term Analytical Model

Gate oxide breakdown, TDDB defect-generation mechanism and device wearout dynamics have been investigated during the last decades. Conceptually, the TDDB phenomenon can be divided in two stages. In the first stage, the oxide is slowly damaged under electrical stress. In this stage, the tunneling current is increasing gradually as a result of oxide defects generation. SBD and PBD are represented in this stage. When the tunneling current reaches a critical value, a rapid runway stage begins. In this stage occurs acceleration in the damage process, leading to the formation of a permanent conductive path through the oxide. The result of this stage is the hard oxide breakdown (HBD). The time necessary to the device reach the runway stage determines the oxide lifetime, which is directly related to the device mean time to failure (MTTF).

There are several different models proposed in the literature to estimate the MTTF of TDDB aging effect. Currently, three models, thermochemical model (*E*), voltage-driven model and anode-hole-injection model (*1/E*), have received wide applications and are used by reliability research and engineers (LI, 2008). These models explore mainly the electric field strength in the oxide, temperature, transistor dimensions, and some technology parameters.

MTTF is important to estimate the device lifetime. For an operation point-of-view, it is also important to know the TDDB behavior before the HDB, e.g. the behavior of the first stage mentioned at the beginning of this section. Another negative point related to previous cited models is that they are not intuitive to designers. The main characteristic

affected by TDDB is the gate tunneling current. An empirical model that explores I – V characteristic of TDDB have been proposed in (MIRANDA, 1999). The proposed model is represented by:

$$I_g = KV^p \tag{3.7}$$

where V is the voltage across the gate oxide, and K and p are fitting technology parameters based on technology characterization results. Since this power law model reflects the gate tunneling current, it is incorporated in several electrical simulations as a voltage dependent current source or a voltage dependent resistance placed between the gate and drain/source transistors terminals, as illustrated in Figure 3.5.

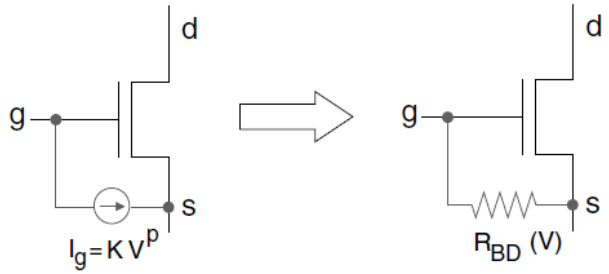


Figure 3.5 – Power law TDDB equivalent circuit model (CHOUDHURY, 2010).

This power law model presented previously is widely applied in the related literature. However, the TDDB time dependence is not considered as a parameter. Although the TDDB effect does not have an recovery stage in normal operation conditions, the temporal dependence is important since in a digital circuit the transistors of a logic gate have the same stress condition, i.e., the same V value in Equation (3.7), but such transistors are not in that stress condition during all the time. Experimental data have indicated that the gate tunneling current due to TDDB effect grows exponentially with stress time (LINDER, 2004). A time dependent oxide defect current model for TDDB effect is described as following (LI, 2008):

$$I_g = I_0 \exp\left[\kappa_1 \cdot \exp\left(\beta_1 \cdot V_g - \theta_1 \cdot t_{ox}\right) \cdot t\right] \tag{3.8}$$

where I_0 is the gate tunneling current in a fresh transistor, κ_1 is determined by the relation between the fresh and breakdown gate tunneling current, β_1 is a Weibull slope parameter, V_g is the voltage across the gate oxide, θ_1 is a constant parameter equal to 7.67, t_{ox} is the oxide thickness, and t is time.

In digital circuits, two voltage levels are verified. The electric field associated to TDDB degradation is only present when the PMOS transistor is negative biased and the NMOS transistor is positive biased. Considering the PMOS as example, this degradation condition is the same as the one in NBTI effect. As discussed previously, the degradation condition is function of the gate signal probability and the transistor arrangement. The transistor stress probability (TSP) parameter used in NBTI model can be also applied to TDDB model. For NMOS transistor, the TSP is the complementary bias condition.

Since the TDDB degradation condition in digital circuits has always the same voltage across the gate oxide, the model represented in Equation (3.8) can be simplified. Another peculiarity of TDDB effect is the inexistence of a recovery stage in normal

operation conditions. This characteristic allow in insertion of TSP as an effective degradation time concept. The simplified model used in this work is the following:

$$I_g = I_0 \cdot C \cdot \exp(D \cdot TSP \cdot t) \tag{3.9}$$

where I_0 is the gate tunneling current in a fresh transistor, C and D are technology dependent constants, t is time, and TSP is the transistor stress probability.

Figure 3.6 shows a comparative analysis between the model presented in (LI, 2008) and the proposed simplified model. The curves are exactly the same since the constants C and D of the proposed model have been calibrated based on constants presented in (LI, 2008) and the TSP is considered '1', observing that it is not presented in (LI, 2008).

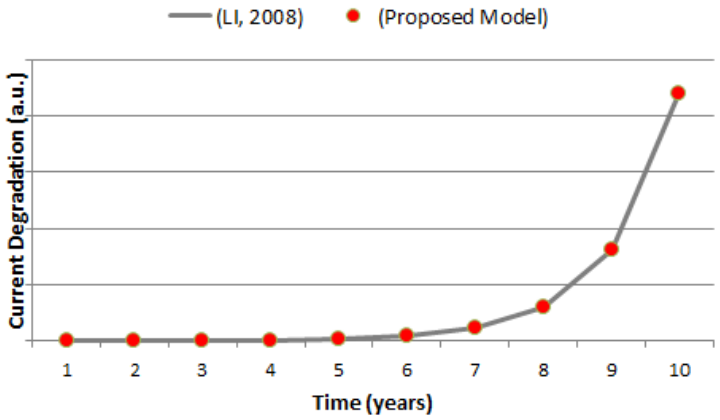


Figure 3.6 – Comparative analysis between models described by Equation (3.8) and Equation (3.9).

3.4 Interaction Between Mechanisms

Each of the previous aging mechanisms mentioned has its own particularities. HCI can be defined as a dynamic mechanism that affects the NMOS threshold voltage. NBTI can be considered as a static effect that affects the PMOS threshold voltage. TDDB is also a static mechanism, but affects the gate tunneling current in both PMOS and NMOS transistors. Their effects might be combined to provide a more accurate and efficient approaches to deal with wearout device degradation.

The exact physical mechanism involved in each transistor aging effect remains an open subject. The most accepted theory is the existence of several physical mechanisms that contribute to the degradation caused by each effect. Some of these physical mechanisms can contribute to more than one degradation mechanism. One example is the oxide defect generation. These defects are directly related to TDDB. In the same way, the charge trapping/detrapping theory explores not only the intrinsic oxide defects, but also this generated defects, creating also a relation to NBTI effect (ISLAM, 2011).

The experimental characterization measurements are the basis to the advances in the understanding of those aging effects in each new technology node. These measurements methodologies are in constant evolution following the new findings. The used methodology explores the main dependence of each mechanism to obtain accurate behavior. As example, the switching activity is largely explored in HCI characterization methods being avoided in TDDB and NBTI characterization (KEANE, 2010).

As mentioned before, one of possible classification of the addressed aging mechanisms is in static and dynamic degradation conditions. The degradation due to NBTI and TDDB occurs when the transistors are biased negatively or positively. From this perspective, they can be classified as static degradation condition. HCI degradation occurs when the transistor is switching and, consequently, it is in dynamic class. Another important fact is the affected transistor characteristic. HCI and NBTI mainly affect the transistor threshold voltage, whereas TDDB is characterized by the increment in gate tunneling current.

From previous statements, the interaction of each mechanism is computed through the sum of each degradation effect. This approach is used in several other works that treat the interaction between different aging mechanisms (LI, 2008; BERNSTEIN, 2006; LUO, 2010).

4 MOTIVATION AND THESIS CONTRIBUTIONS

The reliability of integrated circuits (ICs) during its entire lifetime is a subject studied for decades. The continued downscaling of feature size in ICs increases the importance of degradation effects. The system reliability becomes a critical concern in nanometer circuits. Solutions in all abstraction levels have been proposed in the literature during last decades. This chapter discusses the solutions addressed to HCI, NBTI and TDDB, especially the ones that deal with the degradation mechanisms at design level. In the following, the main contributions of this thesis are highlighted.

4.1 HCI Aware Solutions

Hot carrier injection has been a reliability concern in MOS devices for decades. The degradation in transistor threshold voltage, and consequently circuit performance, motivates the investigation and development of techniques in several abstraction levels involved on IC designs. The redundancy is usually explored at system level. At manufacturing level, the introduction of lightly doped drains (LDDs) in transistor structure has the objective to lowering the strong lateral electric field in the vicinity of the transistor drain terminal. The reduced electric field prevents HCI (OGURA, 1980). For instance, process solution in high-κ gate dielectric transistors by using high pressure deuterium post metallization annealing (PARK, 2007). The rest of this section is focused at design level solutions.

As previously discussed, the switching probability plays a major rule in V_{th} degradation due to HCI. Associated to the V_{ds} dependence, several works suggest a pin reordering to mitigate HCI effect. In this case, the damage can be reduced connecting signals with low switching probability in transistors connected to the output node (QUADER, 1994). The signal scheduling is also an alternative to mitigate the V_{th} degradation due to HCI (LEBLEBICI, 1996; LI, 1996). Figure 4.1 illustrates the proposed scheduling for a 2-input NAND gate. Another positive point related to this technique is the absence of area penalty. A resizing solution associated to pin reordering that explores the most susceptible transistors to HCI degradation is presented in (DASGUPTA, 1996). The solution presents and average saving of 108% in delay degradation at a cost of increment around 16% in power consumption.

The addition of dummy NMOS transistor at the top of the pull-down plane is also suggested to mitigate the HCI degradation. This dummy transistor is always turned on. Since it never switches, it is not be affected by HCI. By making so, the bottom transistors never experiences large V_{ds} and, consequently, V_{th} degradation due to HCI is reduced (SAKURAI, 1986). Due to the same V_{ds} dependence, when transistor arrangement is taken into account, series connected devices as in the pull-down plane in

NAND gate suffers less degradation due to parallel connected devices as in the pull-down plane in NOR gate (LI, 1996; FANG, 1998; GUERIN, 2008).

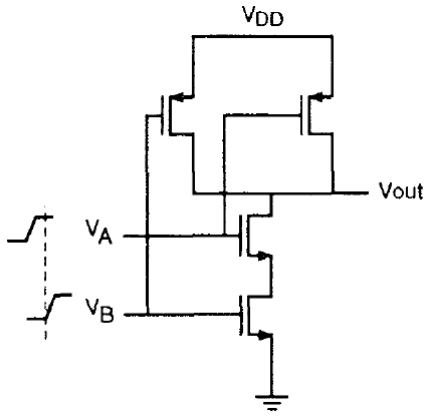


Figure 4.1 – Example of input signal scheduling in a 2-input NAND gate to reduce HCI degradation (LEBLEBICI, 1996).

Another design technique proposes the addition of a self-bootstraping NMOS transistor in stack arrangements to reduce the damage caused by HCI effect. Figure 4.2 illustrates the proposed approach. A small disadvantage is the increment in circuit area (PARK, 1989).

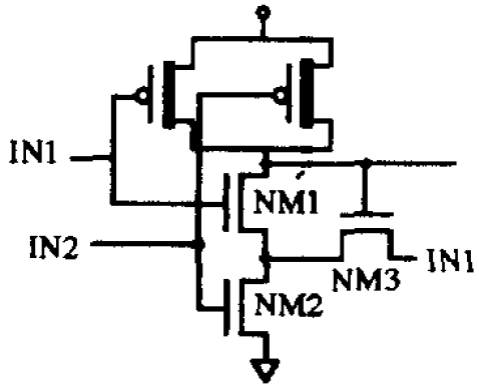


Figure 4.2 – HCI aware design by adding self-bootsrapping transistor (LI, 1993).

Clocked CMOS circuits can also be used to mitigate the HCI effect. Since the clock signal arrives only after all other signals settle, the output only switches due to the clock switching. Putting the clocked transistor connected to ground avoids HCI degradation (LI, 1993). Improved area and complex synchronization are the main drawbacks. An analysis over pass transistors shows a worse degradation than in transistor that are not required to operate in reverse mode, mainly due to the fact that the degradation occurs in both junctions (MISTRY, 1993).

The output capacitance and signal activity are explored in (ROY, 1994) to mitigate hot carrier injection and electromigration. The degradation is estimated at gate level and this information is used to optimize logic synthesis against those effects. A similar approach is proposed in (CHEN, 1997), and presents an average in decreasing of 29% in damage caused by HCI.

A layout-driven hot carrier degradation minimization approach that takes layout information into account is proposed in (CHANG, 2001). The solution combines the

functional symmetry based rewiring technique with traditional gate resizing and pin reordering techniques.

The more recent approaches to deal with HCI degradation usually involve the analysis of more than one aging effect. The discussion about techniques that treat more than one effect is outlined at the end of this chapter.

4.2 NBTI Aware Solutions

NBTI in PMOS transistors has become a major reliability concern in nanometer digital circuit designs. The research community has given significant attention to this effect since it affects the circuit performance over the time, and in extreme cases can cause circuit timing/functional failures. The physical mechanisms associated to this aging effect and analytical models have been discussed in Chapter 3. This section discusses several proposed approaches to treat such undesired degradation. The existing techniques act at all abstraction levels of circuit design methods. The gate and circuit design level solutions are the most explored in this review.

At manufacturing level, the mitigating techniques are centered in increasing the holes mobility to reduce the number of interface traps created and improving the interface structure between the substrate and the oxide. Strained silicon has been pointed as a solution to improve the holes mobility robustness against NBTI effect (ISLAM, 2008).

The temperature is one of the most effective ways to reduce the NBTI degradation. The electrochemical reactions at substrate-oxide interface are thermally activated. A reduction of operating temperature from 125ºC to 75ºC can achieve 37% of delay degradation saving (KHAN, 2011).

At design level, several techniques have been proposed in the literature. One of the most intuitive techniques is to avoid the transistor biasing condition that present the severe NBTI degradation. In this sense, input vectors for minimum standby degradation can be selected to mitigate PMOS aging (WANG, 2007). One important point in this technique is the relation to the minimum leakage vector. A careful tradeoff between both aging and leakage current parameters has to be considered (WANG, 2009). For large circuits when several gates cannot be well controlled by primary input vectors, another technique explore internal node control to guarantee minimal NBTI stress for the gates that are in critical path (BILD, 2009).

Other classes of techniques have been proposed to compensate the NBTI timing degradation. Gate sizing, guard banding, supply and threshold voltage tuning are example of such techniques. The guard banding approach consists in limiting the maximum system clock frequency to compensate for possible future NBTI delay degradation. This guard banding ensures that the system does not fail over the time by sacrificing a percentage of the initially available performance (ABELLA, 2007).

In gate sizing solution, the transistor width of logic gates are increased, increasing so the initial circuit frequency. The oversizing in transistor width has to guarantee that the system still meets the timing requirements during its entire lifetime, even with NBTI degradation. There are two major challenges involved in this scope. The first one is to identify the most sensitive gates to NBTI effect (WANG, 2007). The second is to define the appropriate gate oversizing. In this sense, the NBTI degradation model used to estimate the V_{th} shift is extremely important. A pessimistic approach can be achieved if

only the static stress conditions are taken into account (PAUL, 2007). However, this technique imposes an area overhead and increases the power consumption (VATTIKONDA, 2006). An approach that finds the appropriate relationship between PMOS and NMOS transistors width and present the best compromise in terms of area and performance penalties is proposed in (SILVA, 2009).

Similar to gate sizing solution, V_{dd} and V_{th} tuning would be an effective technique to compensate the performance degradation due to NBTI. According to Figure 4.3, the amount of supply voltage increasing to compensate the NBTI degradation in circuit speed during its lifetime is smaller than the threshold voltage penalty. Adding the fact that is much easier control the V_{dd} change than the V_{th} change, the V_{dd} tuning approach shows to be more practical (VATTIKONDA, 2006). There are two main negative points in this approach. Firstly, the increasing in V_{dd} increases also NBTI degradation, requiring a further increase in V_{dd}. Secondly, increasing V_{dd} increases the power consumption and, therefore, the circuit temperature. Higher temperatures intensify NBTI degradation, requiring a higher V_{dd} value.

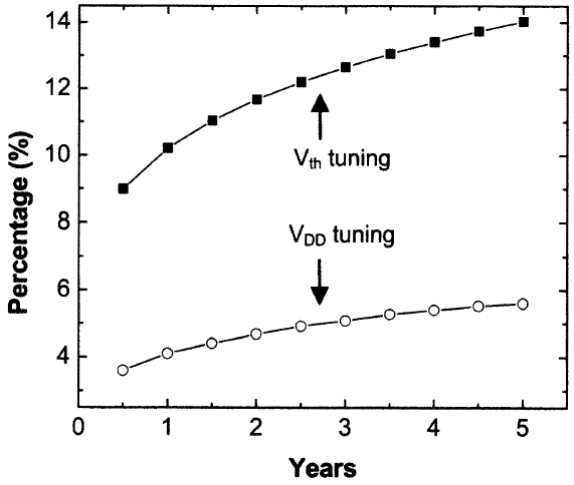


Figure 4.3 – Vdd and Vth adjustment to compensate the NBTI degradation in circuit speed (VATTIKONDA, 2006).

Variations in a fixed operating voltage guard band have been explored in order to compensate NBTI degradation. A schedule voltage scaling that increases gradually the operating voltage during system lifetime is proposed in (ZHANG, 2009). Another alternative explores adaptive supply voltage combined with adaptive body biasing to maintain optimal performance of aged circuits (KUMAR, 2011). The work takes also advantage of a positive consequence from the NBTI degradation that is the subthreshold current reduction due to transistor V_{th} increment. These solutions usually present a lower supply voltage overhead when compared to the fixed guard band supply voltage approach, reducing so the impact of negative points.

Furthermore, the exact impact of supply voltage tuning on NBTI degradation is not clear, and there are contradictory arguments. (KARAKONSTANTIS, 2010) suggests lower V_{dd} to mitigate the delay increment, while (WANG, 2007) negated the argument and favored higher V_{dd}. Additionally, voltage increment should be in limit as it results in higher leakage currents.

(KUMAR, 2011) also presents a hybrid approach that combines merits of both adaptive and synthesis techniques to achieve better results. As input vector approaches,

the synthesis solution can be classified as a class of techniques that mitigate the NBTI degradation. A method to perform technology mapping by taking into account the NBTI effect is presented in (KUMAR, 2007). The delay degradation of every gate from a standard cell library is characterized as function of the input signal probability and the NBTI dynamic behavior. In this step, the influence of series-parallel transistor arrangements is also explored. Such information is used to perform optimization during the technology mapping stage. The work shows that area and power consumption can be saved when compared to sizing solutions.

Several other frameworks are proposed in the literature to mitigate NBTI in synthesis level. (WU, 2009) explores logic restructuring at gate level and pin reordering to mitigate NBTI performance degradation. The logic restructuring explores concepts of function symmetries whereas the pin reordering explores the transistor stacking effect (VATTIKONDA, 2006). A framework to integrate NBTI effect into circuit analysis is proposed in (WANG, 2010). The framework consists in estimating the transistor degradation according to a NBTI long-term model, followed by the characterization of a degraded gate library and circuit analysis. The impact of NBTI is then evaluated under different conditions. In conclusion, temperature and input signal probabilities have higher influence than supply voltage to mitigate NBTI effects. In addition to propagation delay degradation, the signal transition time is also important to define the total gate delay. In this sense, the signal transition degradation due to NBTI effect is explored in (KHAN, 2011).

Although there are many works with different solutions to compensate or mitigate NBTI degradation, still exits several demands of design solution and automated tools capable to address the emerging needs of reliability, mainly at the early stages of the design flow.

4.3 TDDB Aware Solutions

Traditionally, the breakdown of the transistor gate oxide has been usually considered a manufacturing issue. High quality oxides and different dielectric materials are some of the efforts in manufacturing area (CARTIER, 2009; PRASAD, 2008; CRUPI, 2003). At system level, failure techniques have been deeply studied. In this scope, the use of redundancy is largely explored (CORNELIUS, 2008; SEAMROW, 2012). However, besides extensive research in manufacturing and system level approaches, very little effort has been put into specific low-level TDDB design solutions.

From a historical perspective, there are several works that explored the computation in presence of gate oxide short (HAO, 1993; SEGURA, 1995). However, these works do not deal with the TDDB gradual oxide degradation. Several insights to deal with TDDB effect are suggested in (POMPL, 2006). To prevent the gate integrity, transient analysis of the node potential is required. Overshot events in gate terminal should be avoided. Power down techniques present benefits for TDDB reliability since the duty cycle of electrical stress is reduced. Despite of all the suggested techniques, no concrete results is actually presented.

A redundant transistor insertion to improve system reliability in regard to TDDB is proposed in (CORNELIUS, 2008). This work identifies the most vulnerable transistors to TDDB effect, and inserts redundant transistors at previously identified instances. Figure 4.4 illustrates the proposed approach. The work also explores the use of redundant transistor with thicker oxide. The results obtained by this technique have

shown an average improvement in reliability (MTTF) of around 40% at a cost of average delay, area and power degradation of 10%.

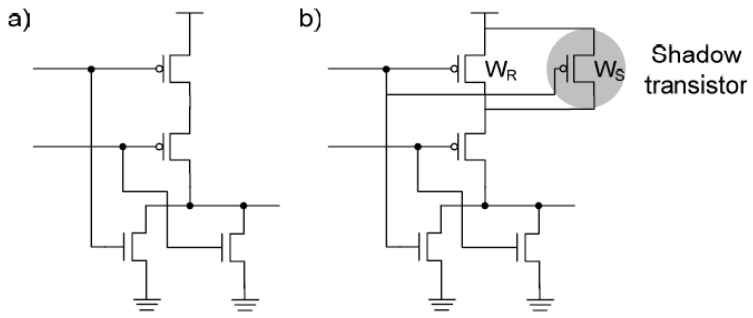


Figure 4.4 – NOR gate: (a) conventional schematic, and (b) with a shadow (redundant) transistor for the upper PMOS (CORNELIUS, 2008).

Another approach that explores redundancy in regard to TDDB has been proposed in (SAEMROW, 2009). In this work, three different design approaches have been proposed and compared. The main difference between the approaches is the abstraction level where the redundancy is applied. Figure 4.5 illustrates the evaluated solutions using a CMOS inverter as example. The best solution increases lifetime reliability up to 200% with no delay cost. However, the penalty is double area and power consumption.

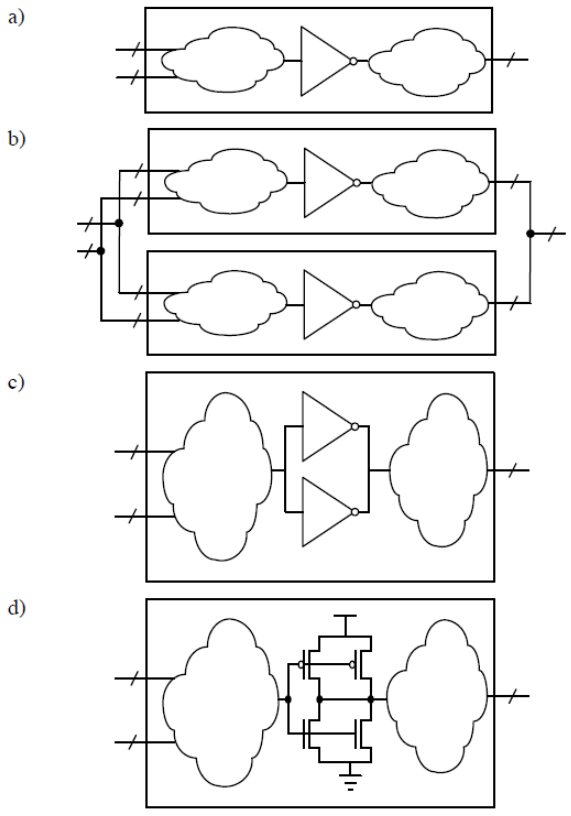


Figure 4.5 – Duplication strategies: (a) original approach, (b) block duplication, (c) gate duplication, (d) transistor duplication (SAEMROW, 2009).

An alternative solution that explores the selective redundancy in only the most vulnerable transistor stacks based on activity and critical propagation delay has been

investigated in (SAEMROW, 2012). An approach the combines the idea of redundancy and the sleep transistor technique to increase the expected circuit lifetime is proposed in (TORRES, 2011). Both solutions present improvements in circuit lifetime at cost in delay, power and area.

The existence of few works that explore the progressive degradation dependence of TDDB at low design level increases the importance of new investigation of design solution and automated tools that are capable to address the TDDB reliability at the early stages of the design flow.

4.4 Interaction

The amount of secondary effects that should be considered in IC design is increasing at every new technology node. Static currents, variability and aging effects are some examples. There are several works where the aging effects, more specifically NTBI, are treated in conjunction with other nanometer effect. The most explored relationship is between NBTI and static currents. The input vector dependence has been explored to mitigate both NBTI degradation and static currents when the system is in standby mode (WANG, 2009). Logic gate sizing method to reduce power and to improve reliability is proposed in (SULIEMAN, 2010). Gate replacement algorithms are explored to deal with both static power and NBTI effect in (WANG, 2009). Specific circuits as full adders are investigate in (CHEN, 2009).

However, with the continued device scaling, there is not only one dominant aging effect. At least, HCI, TDDB and NBTI are been treated with similar severity in nanometer design. It is intuitive that the degradation in system characteristics became even worse when the mechanisms interaction is taken into account. Although a significant number of works deals with the specific aging effect, only in recent years the interaction between mechanisms is being explored.

The interaction between two of the tree mentioned effects is easier to be found. HCI and NBTI are the most investigated one. There is a good reason for that. NBTI is the first effect to have the importance raised in nanometer technologies, whereas HCI has been treated by decades. However, most of the works are focused on properly estimate the degradation of both effects, instead of propose new techniques that considered both degradation penalties or also evaluate the efficiency of the previous purposes considering only one effect (LORENZ, 2009; TU, 2009; HUARD, 2007; GUERIN, 2005; LIU, 2006). NBTI and TDDB have also been evaluated together. In this work, the same behavior is verified. The works are centered in showing the circuit degradation characteristics when both mechanisms are considered at the same time (TERAI, 2007; LUO, 2011).

The treatment of the three NBTI, HCI and TDDB effects at the same time appears in some works. An investigation to improve FPGA lifetime is performed in (SRINIVASAN, 2008). In this work, the degradation is evaluated and FPGA dedicated techniques to improve lifetime are proposed. In terms of IC design, there are works centered in developing simulation methods that are able to consider the device degradation (LI, 2008; MARICAU, 2009). In terms of design for reliability, an approach that explore on-chip real-time reliability monitors to adjust the supply voltage according the most different effects degradation is presented in (KARL, 2008).

From previous discussion, the aging mechanism interaction is largely explored in characterization methodologies and simulation methods. However, there are few design approaches that take into account more than only one degradation mechanism. To avoid the reduction in circuit lifetime, effort should be centered in find solutions to wearout degradation in future technologies.

4.5 Contributions to the State-of-the-Art

From previously discussed topics, it is possible to observe that when designs reach nanometer dimensions, secondary effects reach significant importance and become critical design challenges. These new challenges have to be addressed to maintain the circuit evolution. For this purpose, the thesis is focused on the emerging aging effects. The main contributions of the thesis are explained in the following.

A CMOS logic gate aging cost is the first concept explored in this work. Considering the input signal and switching probability associated to the transistor arrangement, an aging cost for a specific the gate is computed. This aging cost intent to provide a value that reflects the delay degradation caused by NBTI and HCI, and the gate tunneling current due to TDDB. Such a kind of solution is a potential approach when associated to technology mapping algorithms and circuit degradation analysis.

A gate design technique to reduce aging degradation is the second contribution of this work. The proposed technique explores the aging robustness of series transistor association. It consists in a transistor arrangement restructuring and can be applied in any series-parallel transistor arrangement. All three aging mechanisms are explored in the proposed technique. Also, there is no area penalty associated to the transistor arrangement restructuring.

The last major contribution provides insights related to the design of more robust circuits against aging effects. In this sense, the pin reordering approach is firstly explored. Simulation results are used to justify the importance in exploring this concept at circuit level design. A second approach explores the aging robustness of complex logic functions design in single complex stage or in multiple simple stages. If a circuit can be considered a set of multiple stages of gates, then this analysis provides insights to the better choice of used gates at circuit level.

All approaches presented previously are discussed in detail in the next two chapters. The Chapter 5 is dedicated to the gate aging cost estimation, whereas Chapter 6 is centered in design solutions, firstly at transistor level and afterwards at gate level. At the end of Chapter 6, some ‘positive’ aspects that can be explored in relation to the aging effects are also pointed out.

5 DEFINING AGING COSTS

As discussed previously, the aging effects are becoming a critical design issue in nanometer projects. These effects are usually evaluated at the end of the circuit design flow. In several cases, at that point, the designers may to figure out that their circuits will attend the design requirements during the entire lifetime. The treatment of such effects in early stages of the design flow is a good alternative to minimize their influence in the final circuit.

The proposal of this chapter is to present a method to indicate the severity of wearout mechanisms in CMOS logic gates. The aging cost attributed to each gate can be used by logic synthesis tools to produce more reliable circuits. Moreover, this information can be explored in the development of standard cell libraries to produce more reliable gates. The main idea is that a fast classification of the circuit robustness could be performed based on the information of their instances (logic gates).

NBTI, TDDB and HCI are the aging effects addressed in this work. These mechanisms have firstly their degradation considered individually. From this individual information, the obtained values can be combined to compute the mechanisms interaction. As mentioned before, the aging effects have their degradation dependent on the transistor biasing. In order to indicate the degradation severity of a logic gate, it is imperative to consider its transistor arrangement structure. The method proposed in this work can deal with any transistor arrangement, including the traditional series-parallel CMOS topologies and the non-series-parallel (‘bridge’) arrangements (ROSA JR, 2009; KAGARIS, 2006).

Although there are several works that explore design solution related to aging effects, according to the bibliographic research performed herein, there is no work that provides similar severity identification for any of mentioned effects. The interaction between mechanisms is explored in several other works and is used to support the effect interaction taken into account in this proposal. Several logic gates and circuit benchmarks are explored in previous works, but there is no work that provides insights related to the degradation severity of any transistor arrangement without performing electrical simulations.

The degradation severity of each logic gate can be considered as an aging cost. The definition of this cost starts from the computation of the transistors bias for all possible input vector combinations. In this scope, the transistors signal probabilities combined with the transistor arrangement are essential to determine the degradation of static effects (NBTI and TDDB). The transistor switching probability, in turn, required to determine the degradation of HCI effect, is computed considering the logic function switching possibilities and also the transistor arrangement.

The transistor arrangement is a crucial part in logic gate aging evaluation. In order to provide a generic methodology that allows the analysis of gates designed in any logic style, a procedure has been proposed to compute the probabilities of any transistor arrangement. This procedure is presented below and it is divided in two parts for an easy understanding. The first part corresponds to the static transistor conditions identification, and is presented in Figure 5.1.

```
1. Read the transistor netlist
2. For all input vector possibility {
3.    Perform Logical Simulation to define value of all nodes
4.    For all transistors {
5.       Increment transistor counter if transistor is at stress biasing
6.    }
7. }
8. Compute transistor stress probabilities
```

Figure 5.1 – Signal probabilities procedure.

In previous procedure, the transistor netlist is read and a logical simulation is performed for all input vector combination to define the logical value of all netlist nodes. With all node value information, the bias of all transistors is verified and the ones that are at severe stress have their counter incremented. At the end, the transistor stress probability is computed.

The second procedure refers to the switching transistor conditions, and is described in Figure 5.2.

```
1. Read the transistor netlist and find interest transistors (the ones
   connected to output node) and input signals (the ones related to interest
   transistors)
2. For each input vector {
3.    Perform Logical Simulation to define value of all nodes
4. }
5. For each interest signal {
6.    For each transitions of interest signal {
7.       Increment transistor counter if the output node changes from 1 to 0
8.    }
9. }
10.Compute transistor switching probability
```

Figure 5.2 – Switching signal probability procedure.

The switching activity is relevant to HCI effect. Logic gate with higher switching activity suffer more HCI degradation. This effect degradation is exponential dependent on the initial transistor drain-to-source voltage. The initial drain-to-source voltage has its maximum value only at transistor directly connected to the output node. The second procedure presented previously explores this characteristic. When the transistor netlist is read, the transistor connected to output node are classified as transistors of interest, and the respective input signals as signal of interest. This information reduces the logic transition evaluation needed to compute the switching probability. In the presented procedure, only the signals of interest have their transitions evaluated. As HCI is more severe in NMOS transistors, only ‘1’ to ‘0’ (i.e., high-to-low) output transitions are relevant. When such high-to-low output node transition is verified, the transistor of interest associated to respective evaluated signal of interest has its counter incremented. At the end of the procedure, the transistor switching probability is computed.

The previous computed probabilities are used to compute individual transistor degradation. This degradation in transistors characteristics results in circuit delay and power consumption changes. As the aging effects affect different transistor parameters, the logic gate aging cost definition depends on the evaluated effect and the affected parameter. The following sessions present the proposed cost definition for each wearout mechanism evaluated.

5.1 HCI Aging Cost

HCI affect the transistor threshold voltage. The logic gate characteristic affected by this degradation is the gate delay. The logic gate delay is the interval between an input signal value change and an output node value change. It is defined according to the delay arcs, which correspond to the delay measured from a gate input value change to the gate output value change for a specific steady state combination of other input signal values. To qualify the overall gate delay degradation it is necessary to compute the degradation of each delay arc.

Another important concept in the proposed analysis is the transistor paths between the output node and the power rails. Such paths are responsible for the output node changing, being strongly connected to the gate delay. When a path is composed by only one transistor and this device is the switching transistor of a specific delay arc, the transistor can be considered the only one responsible for the output switching. When the switching device belongs to a transistor stack, all devices in the stack contribute to the arc delay. However, in this case, the switching device has a higher contribution to the arc delay.

The arc delay and path concepts, discussed before, are explored in the definition of the HCI aging cost. The degradation in transistor threshold voltage is directly related to the arc delay degradation when the degraded transistor is the unique device in the path responsible by the output node switching. When the path consists in a stack transistor structure, all device degradation has to be computed. As discussed previously, HCI affects mainly the NMOS transistor connected to the output nodes. In this case, only transistors at the top of the stack are degraded. The proposed HCI aging cost reflects the average gate delay degradation. In this sense, all logic functions arcs have to be considered. The delay arcs where the switching transistor is the degraded transistor has the degradation computed by its totality. When the degraded transistor is part of the arc, its degradation in that arc is divided by a technology parameter extracted from empirical simulation of NAND and Inverter gates. This technology parameter can be expressed as following:

$$HCI\_tech\_const = \frac{T_{NAND}}{\frac{2 \cdot D_{NAND} \cdot T_{INV}}{D_{INV}} - T_{NAND}} \tag{5.1}$$

where T_{NAND} and T_{INV} are the degradation in transistor threshold voltage at NAND and Inverter gates, respectively. D_{NAND} and D_{INV} are the average delay degradation for NAND and Inverter gates, respectively, when simulations results with degraded devices are compared to the ones with fresh devices.

The procedure presented in Figure 5.3 describes how the HCI aging cost is computed. The transistor netlist is read, the delay arcs are defined, and the degraded transistors are identified. From previous computed probabilities, the aging model

presented in Chapter 3 is used to compute the threshold voltage degradation of each device. The transistor degradation is used to compute the logic gate degradation observing the role of the degraded device, as discussed before. At the end of the procedure, an average degradation is calculated and the value is normalized to the Inverter degradation. The normalization allows an easy comparison between different gate designs, and avoid the misunderstanding estimation of the precisely gate delay degradation.

```
1. Read the transistor netlist and identify the delay arcs and the degraded
   transistors
2. For each degradaded transistor {
3.     Compute Vth degradation from HCI analytical model, switching
   probabilities and technology parameters
4. }
5. For each arc {
6.     If switching transistor is degraded {
7.        Logic_gate_degradation += Vth_Transistor_Degradation
8.     } else {
9.        Identify the degradaded(s) transistor that are related to the arc
10.          Logic_gate_degradation += Transistor_Degradation/HCI_tech_const
11.       }
12.       counter++;
13.    }
14.}
15.Logic_gate_degradation = Logic_gate_degradation/counter
16.HCI_Aging_Cost = Logic_gate_degradation/Inverter_gate_degradation
```

Figure 5.3 – Procedure to determine the HCI aging cost.

5.2 NBTI Aging Cost

NBTI effect affects the threshold voltage of PMOS transistors. Similarly in HCI effect, the affected parameter at the gate abstraction is the delay. The definition of a NBTI aging cost for a logic gate should also consider the logic function delay arcs. Differently from HCI, that has its high degradation severity concentrated in NMOS devices connected to the output node, NBTI degrades all transistors in the pull-up PMOS plane. This characteristic increases the number of devices that have to be evaluated if a similar HCI aging cost procedure is applied to compute NBTI aging cost. Since the NBTI aging cost does not aim to provide a precise value of the gate delay degradation, but qualify different gates according to the penalties, the fact that all PMOS transistor in pull-up plane are affected allows the application of a different procedure.

As all PMOS transistors in pull-up plane are affected by NBTI effect, the logic gate degradation can be computed considering the average degradation of all devices, the average amount of device in stacks for all delay arcs and a technology constant that emulate the influence of non-switching transistors in degradation delay. The following equation indicates how logic gate degradation due to NBTI is computed considering the previous data:

$$Logic\_Gate\_Degradation = ADD \cdot \left(1 + \frac{ADSA}{NTC}\right) \tag{5.2}$$

where *ADD* is the average device degradation, *ADSA* is the average number of devices in stacks of delay arcs, and *NTC* is the NBTI technology constant defined by:

$$NTC = \frac{ADSA - 1}{\frac{D_{NOR} \cdot AT_{INV}}{D_{INV} \cdot AT_{NOR}} - 1} \tag{5.3}$$

being *ADSA* the average number of devices in stacks of delay arcs. D_{INV} and D_{NOR} are the delay degradation due to NBTI effect of Inverter and NOR gates, respectively. AT_{INV} and AT_{NOR} are the average transistor degradation of Inverter and NOR gates, respectively.

The complete procedure involved in NBTI aging cost determination is described in Figure 5.4.

```
1. Read the transistor netlist and identify the delay arcs and the degraded
   transistors
2. For each degradaded transistor {
3.     Compute Vth degradation from NBTI analytical model, signal
   probabilities and technology parameters
4.     Total_devices_Degradation = Transistor_Vth_Degradation
5. }
6. ADD = Total_device_Degradation/#Transistors
7. For each delay_arc {
8.     Total_arc_stack = # of device in delay arc stack;
9. }
10.ADSA = Total_arc_stack/#delay_arc
11.Logic_Gate_degratadion = ADD*(1+ADSA/NTC);
12.NBTI_Aging_Cost = Logic_gate_degradation/Inverter_gate_degradation
```

Figure 5.4 – Procedure to determine the NBTI aging cost.

5.3 TDDB Aging Cost

Differently from HCI and NBTI, that affect the transistor threshold voltage, TDDB effect increases the transistor gate tunneling current. At gate level analysis, this degradation causes an increment in static power consumption. Since the static power consumption is directly dependent on the gate input vector, an analysis of the degradation for each input vector combination is essential to provide a realistic TDDB aging cost.

The static power consumption is transistor bias dependent. After defining the transistor degradation based on the signal probabilities and TDDB model presented in Chapter 3, the first step to compute the increasing in static current due to TDDB is to identify the gate internal node biasing for each input vector combination. The bias identification consists in defining a value for each node in the transistor arrangement. For simplification, the possible values are ‘0’, V_{dd}, V_{th}, and ‘V_{dd} - V_{th}’. These possible bias conditions are illustrated in Figure 5.5.

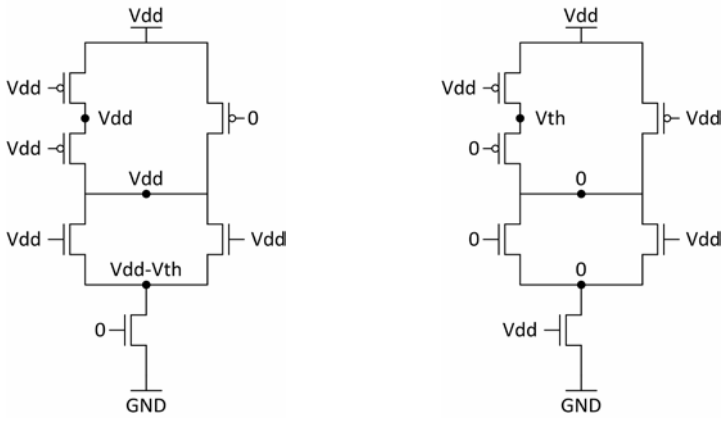


Figure 5.5 – Possible bias conditions in transistor arrangement.

For each input vector, the transistor bias associated to the device degradation is used to compute the contribution of each device. The gate degradation due to TDDB effect is defined as the average degradation of all input vector combination. The maximum degradation is also computed in the procedure. To obtain the TDDB aging cost, both data are normalized from the degradation of Inverter. The procedure is described in Figure 5.6.

```
1. Read the transistor netlist
2. For each transistor {
3.     Compute TDDB degradation from TDDB analytical model, signal
   probabilities and technology parameters
4. }
5. For each input vector combination {
6.     Define logic gate internal nodes bias
7.     input_vector_gate_current = 0;
8.     For each transistor {
9.        input_vector_gate_current += Transistor_Degradation*ABS(Vg-Vd);
10.    }
11.    max_current = MAXIMO(max_current, input_vector_gate_current);
12.    total_current += input_vector_gate_current;
13.    vectors++;
14.}
15.TDDB_Aging_cost = (total_current/vectors)/Inverter_TDDB_Aging_Cost;
16.MAX_TDDB_Aging_cost = max_current/Inverter_MAX_TDDB_Aging_Cost;
```

Figure 5.6 – Procedure to determine the TDDB aging cost.

5.4 Aging Cost Validation

The proposed aging costs results were validated through a qualitative comparison to electrical simulation data. The models presented in Chapter 3 provide the transistor degradation based on computed probabilities. Electrical simulations were performed to extract fresh and degraded characteristics of several gates, and such degradation levels were compared to the proposed aging cost results.

The transistor degradation for each aging effect has been computed considering the models presented in Chapter 3. The needed signal and switching probabilities were obtained considering the gate transistor arrangement and the procedures presented in Figure 5.1 and Figure 5.2. In this aspect, the input signal probability of 0.5 and the same

switching frequency have been applied to all inputs. The aging models have been calibrated to provide in the worst case V_{th} degradation of 50 mV for NBTI and HCI and a gate tunneling current of 1 µA for TBBD. These maximum degradation levels follow similar values used by several works in the literature (LOU, 2011; CHOUDHURY, 2010; TU 2009).

The device degradation is observed in timing and power characteristics of logic gates. Electrical simulations were performed in several gates to obtain the average delay of all arcs and the average static power consumption for all input combinations. Five versions of each gate were created. The original versions are composed by fresh devices. The other four versions consist in netlist with degraded transistors. There are three different netlists with degraded transistors considering only one mechanism in each version. The last version considers the combination of the three effects in the same netlist.

The V_{th} degradation has been inserted in V_{th0} transistor model card parameter. The V_{th0} parameter is part of the definition used by the electrical simulator to compute the transistor threshold voltage. Empirical methods have been used to provide the V_{th} as a function of V_{th0} parameter to guarantee the correct degradation insertion (DOBRESCU, 2000; RUDENKU, 2011). A set of model cards have been created, each one representing a device with different V_{th} . In logic gates netlist, these model cards with degraded threshold voltage have been used to indicate the corresponding degradation of each device.

The gate tunneling current increasing due to TDDB effect is represented by a resistor between gate and drain transistor terminals (CHOUDHURY, 2010). From this approach, in evaluated logic gates, the transistors have been replaced by a subcircuit that comprises a resistor between the gate and drain transistor terminals. The value of the resistor is defined according to the maximum current value provided by the model presented in Chapter 3.

The results of the electrical simulations are used to compute the average degradation levels of each mechanism in the respective affected characteristic. The results are also normalized by the Inverter degradation to allow a comparative analysis to the proposed aging costs.

The logic gates illustrated in Figure 5.7 were used to evaluate the proposed costs. This set of gates explores several transistor arrangements peculiarities. In NAND and NOR gates, simple series and parallel association are evaluated. The composition of simple series-parallel arrangements is presented in AOI and OAI gates. In these gates, the transistor arrangement restructuring is also explored. The CLA units are presented to explore more complex series-parallel associations. Finally, a ‘bridge’ network and its series-parallel CMOS design counterparts are presented to explore non-series-parallel arrangements.

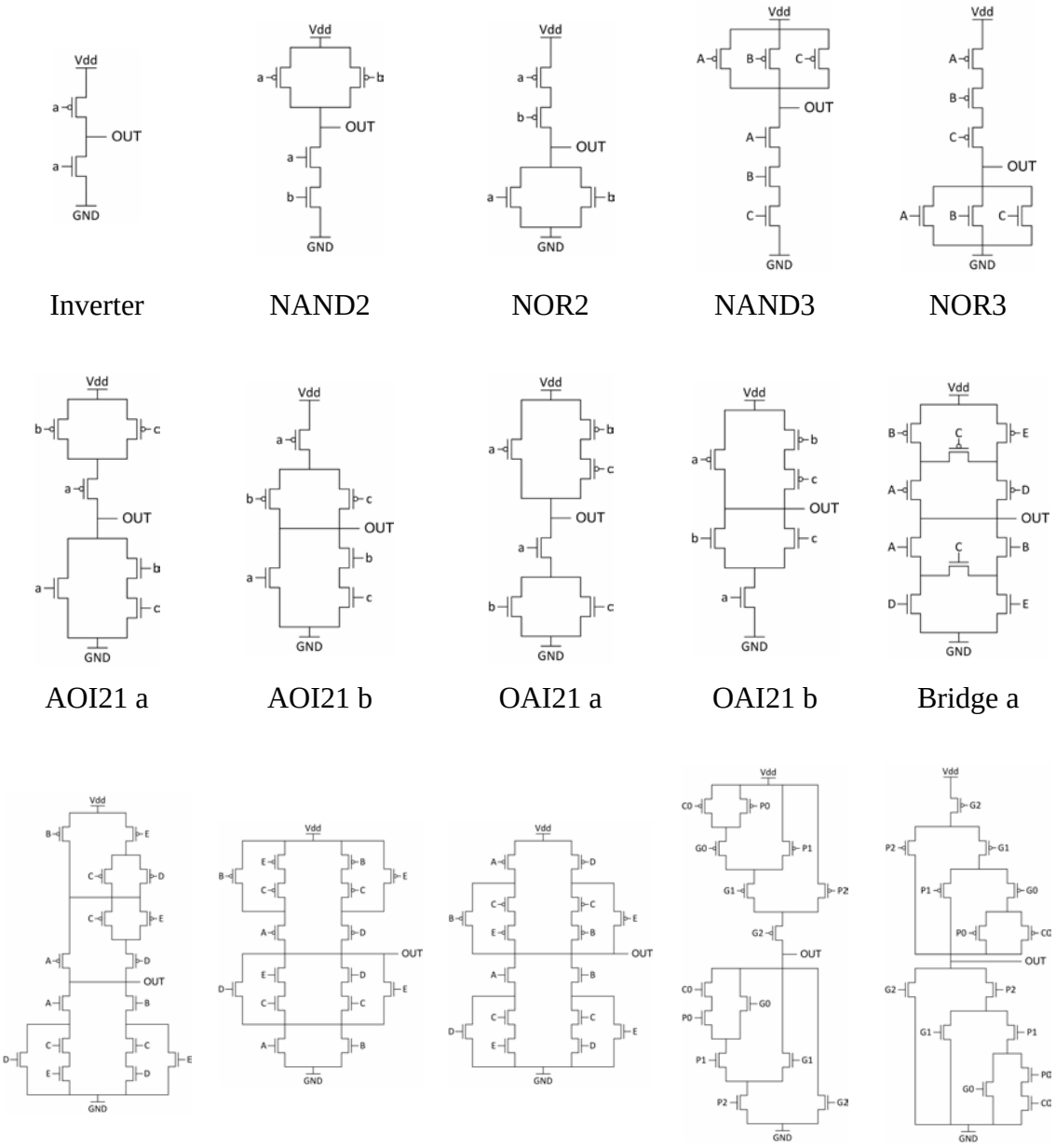


Figure 5.7 – CMOS logic gates used to evaluate the proposed aging cost.

Table 5.1 presents the results of HCI aging cost validation. The logic gates are ordered by the HCI aging cost. In the second column is presented the average high-to-low delay degradation due to HCI effect. Such information has been extracted from the electrical simulations performed using fresh and degraded gates. The third column presents the degradation normalized in respect to the Inverter value. Finally, the proposed HCI aging cost is presented in the fourth column. The obtained results provide several observations:

- As general rule, the HCI aging cost reflects the device degradation in gate delay penalty.
- The perfect agreement with the 2-input NAND gate due to the technology constant extraction is confirmed.

- The simple series and parallel structures present a good behavior according to the NAND and NOR gates results.
- The combination between simple series-parallel arrangements verified in AOI and OAI gates also present a good correlation to experimental results. An interest point in this part is the influence of the pull-up plane in high-to-low propagation delay. This aspect is neglected by the proposed cost that only considers the influence of responsible plane (pull-down to HCI) for the interest output change (high-to-low to HCI). In AOI gates illustrated in Figure 5.7, the difference in the transistor arrangement of pull-plane causes a difference of 7% in average delay degradation. However, this difference does not compromise HCI aging cost classification when compared to the other gates degradation.
- Although all versions of the 'bridge' design present the same HCI aging cost, it reflects the degradation proximity of the experimental results and also order the gates in a satisfactory way.
- The last point is the discrepancy in CLA units (carry out gate). This difference can be considered an extreme case of pull-up plane influence in high-to-low delay. The pull-up plane is not considered in the proposed cost, but it has influence in delay, as mentioned in previous topics. The existence of 4 series transistors in both planes can add several variables in delay computation that are not explored in this fast estimated cost. The 7% difference verified in AOI gates can be larger in CLA units due to this higher number of series transistors. However, when comparing both design solutions, the proposed cost can identify the more robust one.

Table 5.1 – HCI aging cost evaluation results.

Logic Gate	Average High-to-Low Delay Degradation	Normalized Average High-to-Low Delay Degradation	HCI Aging Cost
Inverter	8.3%	1.00	1.00
NOR2	4.0%	0.48	0.50
OAI21 a	3.3%	0.39	0.40
NAND2	3.1%	0.37	0.37
AOI21 a	2.9%	0.35	0.31
AOI21 b	2.7%	0.33	
NOR3	2.2%	0.27	0.28
Bridge b	1.8%	0.22	0.20
Bridge a	1.7%	0.21	
Bridge c	1.7%	0.21	
Bridge d	1.6%	0.20	
OAI21 b	1.6%	0.20	0.19
NAND3	1.4%	0.17	0.18
CLAunit b	2.0%	0.25	0.18
CLAunit a	1.4%	0.17	0.07

Table 5.2 presents the results of NBTI aging cost validation. Similar to Table 5.1, the presented logic gates are ordered according to their NBTI aging cost. In this case, the cost is in crescent order. As NBTI affects PMOS transistors, the low-to-high delay is evaluated. The columns maintain analogous meaning when compared to HCI aging cost analysis. The second column presents the average low-to-high delay degradation extracted from electrical simulations. The third column presents the normalized value of the average delay degradation, and the last column the proposed NBTI aging cost. The obtained results provide several observations:

- The proposed NBTI aging cost has discrepancies in some gates when compared to electrical simulation degradation. However, it remains an excellent agreement to identify the best design for specific function.
- The perfect agreement with NOR2 gate due to technology constant extraction is confirmed.
- Similar to HCI analysis, the pull-down plane affects the degradation in low-to-high delay. It can be verified by comparing experimental results of NAND and OAI gates. This influence is ignored by the proposed cost, and it is one of the reasons for the discrepancies verified.
- As all PMOS transistor are affected by NBTI, independently from their position in pull-up arrangement, and the delay is a function of all devices in the path output – power rails, the average delay degradation is worse in gates with more transistors in series. NOR gates can be used as simple example.

Table 5.2 – NBTI aging cost evaluation results.

Logic Gate	Average Low-to-High Delay Degradation	Normalized Average Low-to-High Delay Degradation	NBTI Aging Cost
Inverter	13.4%	1.00	1.00
NAND2	13.7%	1.03	1.00
NAND3	14.1%	1.05	1.00
OAI21 b	15.5%	1.16	1.21
OAI21 a	15.7%	1.18	
AOI21 b	17.0%	1.27	1.21
NOR2	16.5%	1.23	1.23
AOI21 a	17.3%	1.30	1.29
Bridge d	18.5%	1.38	1.41
NOR3	17.9%	1.34	1.43
CLAunit b	17.9%	1.34	1.43
Bridge a	18.8%	1.41	1.43
Bridge c	19.3%	1.44	1.44
Bridge b	21.0%	1.57	1.51
CLAunit a	20.7%	1.55	1.60

Table 5.3 presents the results of the TDDB aging cost validation. Differently from the previous tables, where the values presented in the second column are the average degradation of the gate characteristic under evaluation, in Table 5.3, the second column present the nominal current value. The TDDB degradation reflects an increasing of gate static power consumption. However, when the logic gate is considered fresh, the dominant component of static power is the subthreshold current. With the degradation, the gate tunneling current becomes the dominant component. As the dominant mechanisms are different in fresh and degraded cases, the second column presents the nominal current value. Another point that endorses this validation is the fact that the gate tunneling current in degraded devices is at least more than 100 times higher than the total static current in fresh gates. This confirms that the nominal value can be considered the correct degradation parameter. The other two columns represent the normalized degradation and the proposed TDDB aging cost. From the obtained results the follow observations can be confirmed:

- The proposed TDDB aging cost presents a good agreement to simulation results, and confirms to be a good alternative to identify the best design for specific function.
- The differences from the aging cost and the experimental results are mainly due to the internal nodes of the transistor arrangements. Although the TDDB procedure considers the V_{th} drop when PMOS transistor is conducting ‘0’ logic and NMOS transistor is conducting ‘1’ logic, the higher gate tunneling current creates several conductive path that can be interpreted as resistor divider. The consequence of this resistor divider is a voltage drop, mainly in nodes that are supposed to attain full supply (or ground), reducing the total gate static current.

Table 5.3 – TDDB aging cost evaluation results.

Logic Gate	Maximum Static Current (nA)	Normalized Maximum Static Current	TDDB Aging Cost
Inverter	1.014	1.00	1.00
NAND2	1.537	1.52	1.52
NOR2	1.538	1.52	1.52
AOI21 b	1.544	1.52	1.63
OAI21 b	1.547	1.53	1.63
AOI21 a	1.662	1.64	1.74
OAI21 a	1.664	1.64	1.74
Bridge a	1.896	1.87	1.85
NAND3	2.040	2.01	2.02
NOR3	2.043	2.02	2.02
Bridge b	3.029	2.99	2.97
Bridge c	3.182	3.14	3.05
Bridge d	3.315	3.27	3.12
CLAunit b	3.199	3.15	3.14
CLAunit a	6.734	6.64	8.25

As mentioned early, the interaction between different mechanisms can be computed as the sum of their contributions. The aging cost can be combined by the same way to provide a cost that reflects more than only one effect. In the following discussion, the interaction between NBTI and HCI is explored. These two mechanisms have been chosen because they affect the same logic gate characteristic. The combination of both NBTI and HCI aging cost is called delay aging cost. Table 5.4 presents the simulation results of average delay degradation when both mechanisms are considered. The average delay is normalized in relation to Inverter delay degradation to facilitate the aging cost analysis. Both NBTI and HCI aging costs are also presented. The last column presents the delay aging cost that consists in the average value between HCI and NBTI aging costs. In the proposed validation methodology, both effects have the same maximum severity of 50 mV and, consequently, have the same weight in the computed average. When the mechanisms have different severities, a weighted average has to be used based on the ratio between the severities of .both aging mechanisms.

The provided cost has achieved the objective of comparing similar functions and different design implementing the same Boolean function. As both NBTI and HCI costs are not used to provide de absolute delay degradation, the presented delay aging cost does not reflect this absolute value. The discrepancies observed in Table 5.4 are originated by the points previously reported for each cost, mainly the fact that HCI and NBTI degradation costs do not consider the influence of complementary plane in degradation delay.

Table 5.4 – Delay aging cost results.

Logic Gate	Average Delay Degradation	Normalized Average Delay Degradation	NBTI Aging Cost	HCI Aging Cost	Delay Aging Cost
Inverter	10.6%	1.00	1.00	1.00	1.00
NAND2	7.9%	0.74	1.00	0.37	0.69
NAND3	7.2%	0.68	1.00	0.18	0.59
NOR2	9.1%	0.86	1.23	0.50	0.87
NOR3	8.1%	0.76	1.43	0.28	0.86
AOI21 a	8.9%	0.84	1.29	0.31	0.80
AOI21 b	8.4%	0.79	1.21	0.31	0.76
OAI21 a	8.5%	0.80	1.21	0.40	0.80
OAI21 b	7.6%	0.71	1.21	0.19	0.70
Bridge b	8.7%	0.82	1.51	0.20	0.85
Bridge a	8.4%	0.79	1.43	0.20	0.81
Bridge c	9.3%	0.88	1.44	0.20	0.82
Bridge d	7.0%	0.66	1.41	0.20	0.80
CLAunit a	9.9%	0.93	1.60	0.07	0.84
CLAunit b	5.9%	0.55	1.43	0.18	0.80

6 DESIGN FOR RELIABILITY

This chapter presents the analysis and solutions of IC design in terms of aging degradation robustness. Initially, a novel design technique that explores the transistor arrangement restructuring to mitigate the aging degradation in CMOS gates is proposed. In the next, different evaluations of circuit design related to aging degradation are performed. Improvements resulted from pin reordering are then quantified through simple cases of study, demonstrating such promising approach, that does not present actually relevant drawbacks. In the following, the design of logic gates using single or multiple stages are investigated in order to provide some design insights at circuit level. At the end of the chapter are discussed some secondary effects that can be explored for circuit improvement in terms of aging effects.

6.1 Transistor Arrangement Restructuring

As mentioned before, in nanometer technologies there is not really a dominant aging mechanism. A design solution that exploits the transistor arrangement restructuring is presented herein. The proposed approach targets the reliability improvement of CMOS gates, taking into account HCI, TDDB and NBTI aging degradation effects.

Considering that most of integrated circuits, nowadays, are designed adopting the standard cell methodology, the solution proposed in this thesis is quite relevant to gate design. As discussed in Section 2.1, the standard cell library composition is an important factor to the final circuit characteristics. Introduce the reliability concepts in the early stages of the IC design flow, increase the chances to obtain a more reliable system, reducing so the cost of higher level techniques.

The following approach can be considered as a design guideline that explores particularities of each class (static and dynamic degradations) of aging mechanism individually. At gate level, the most important design aspects to be explored in terms of reliability improvement are the transistor arrangement associated to the input signals and the switching probabilities. The transistor sizing is another important aspect, but it has not been treated since the author considers that this aspect is more relevant for timing tuning and optimization.

The static degradation mechanisms are the first ones to be evaluated. The proposed technique can be summarized by the following gate design guideline:

- ***When the transistor arrangement is a combination of series-parallel associations, both NBTI and TDDB degradations can be mitigated by placing as many transistor as possible close to the output node.***

The degradation caused by NBTI and TDDB effects is directly related to the electric field across the gate oxide. In digital circuits, this electric field experience his maximum when the PMOS transistor is negative biased (logic value ‘0’ at the gate terminal and ‘1’ at the drain and source terminals) and the NMOS is positive biased (logic value ‘1’ at the gate terminal and ‘0’ at the drain and source terminals). In transistor stacking, the device that is connected to the power rails experiences such maximum electric field every time when its gate terminal assumes the specific logic value mentioned. To the other transistors in the stack, an overall analysis taking into account the input signals probabilities have to be performed.

In summary, the previous analysis concludes that the transistors that are connected at power rails suffer more NBTI and TDDB degradation than the other ones in the gate arrangement. Considering a series-parallel pull-up network, as the one presented in AOI21 gate depicted in Figure 5.7, minimize the number of devices connected to the power rails is an efficient method to reduce the degradation penalties due to NBTI and TDDB. From this perspective, the other version of the pull-up arrangement of the same AOI21 gate depicted in Figure 5.7 is more robust against aging effects.

Since NBTI degradation affects only PMOS transistors, when such strategy is applied to the pull-up PMOS plane, both NBTI and TDDB degradation are mitigated. On the other hand, only TDDB degradation is affected when it is applied to the pull-down NMOS plane. This concept has been already reported considering only NBTI (BUTZEN, 2010).

Electrical simulations have been performed to exemplify the improvements of the proposed approach in terms of reliability. The conditions used to perform these simulations follow the definitions presented in Chapter 5. In summary, the long term models presented in Chapter 3 are used to estimate the device degradation due to aging effects. As the severity of aging mechanisms depends on the technology under evaluation, the degradation applied in this work was considered a maximum V_{th} impact of 50 mV for NBTI and HCE effects, and a range of breakdown gate tunneling current from pico-Ampère (pA) for fresh device to micro-Ampère (μA), i.e. the maximum degraded device, for TDDB effect. The behavior of each mechanism follows the ones already reported in the literature (LI, 2008; QUADER, 1994; CHOUDHURY, 2010). A 32 nm CMOS predictive technology model (PTM) has been used to evaluate the circuits (ZHAO, 2006). The stress probabilities for the devices have been computed according to the procedure presented in Chapter 5. The characterization process considered fanout 4 delay.

Table 6.1 presents the electrical simulation results of some gates depicted in Figure 5.7, for two different design solutions for pull-up PMOS plane. The equivalent logic gates that present similar structure in the pull-down NMOS plane have been omitted since the same TDDB behavior is verified. To perform a fair analysis, all input signals have been considered with the same signal probability.

From the results presented in Table 6.1, it is possible to verify that the transistor arrangement restructuring is a promising alternative to design more reliable gates to Boolean functions. In all evaluated gates presented in Table 6.1 the first design is contradictory to the proposed approach while the second one follows the guideline. The results in terms of rise degradation delay due to NBTI show savings up to 12%. Following the higher temporal severity behavior of the TDDB mechanism, the gate tunneling current due to TDDB experiences more expressive savings, achieving 56% of

gains. The savings are proportional to the ratio between the number of devices connected to power supply in both versions, and also to the number of series transistors in delay arcs.

Table 6.1 – Degradation savings due to transistor arrangement restructuring.

Logic Gate	Rise Delay Degradation due to NBTI (%)	Degradation Savings (%)	Gate Tunneling Current due to TDDB (μA)	Degradation Savings (%)
AOI21 a	17.3	1.7	1.27	7.9
AOI21 b	17.0		1.17	
CLA e	20.4	12.3	2.98	56.0
CLA f	17.9		1.31	
Bridge g	19.2	3.1	2.74	33.6
Bridge h	18.6		1.82	

The dynamic behavior of HCI effect forces a change in the parameter analysis. Instead of signal probability, the switching probability has to be considered in HCI analysis. The switching probability concept used in this analysis is defined as an input signal switching that causes an output switching. Following the discussion performed in Chapter 3, the next analysis is focused on the pull-down NMOS plane due to the higher HCI degradation in such transistor instantiation. The proposed technique to mitigate HCI degradation can be summarized by the following gate design guideline:

- ***When the transistor arrangement is a combination of series-parallel associations, HCI degradation can be mitigated by placing as many transistors as possible far from the output node.***

The degradation caused by HCI effect is directly connected to the lateral electric field through the transistor channel. This lateral electric field is directly related to drain-to-source voltage. In terms of degradation caused by HCI effect, an exponential relationship to drain-to-source voltage (V_{ds}) is observed, as discussed in Chapter 3. In digital CMOS circuits, the maximum drain-to-source voltage is only present in transistors that are connected to the output node. As the transistors with higher V_{ds} are connected at output node, the proposed solution intends to minimize the number of devices connected to the output to reduce the delay degradation penalties due to HCI.

Following the same approach used to static aging effects, electrical simulations have been carried out to exemplify the reliability improvement provided by the proposed approach. The conditions used to perform such simulations follow the definitions presented in the analysis of static degradation mechanisms. The difference is related to the use of the signal switching probability instead of signal probability. To perform an analysis that explore only the transistor arrangement characteristics, all input signal switching probabilities are considered the same. From the input signal switching probability, the transistor switching probability (TSwP) is computed according to the procedure presented in Chapter 5, and used to estimate the V_{th} degradation according to the model presented in Section 3.1.2.

Table 6.2 presents the electrical simulation results of several gates depicted in Figure 5.7 for two different design solutions to the pull-down NMOS plane. For every

evaluated Boolean function, the first gate design is contradictory to the proposed approach whereas the second one follows the guideline.

Table 6.2 – HCI degradation savings due to transistor arrangement restructuring.

Logic Gate	Average Fall Delay Degradation due to HCI (%)	Degradation Savings (%)
OAI21 a	3.3	51.5
OAI21 b	1.6	
CLA f	1.9	10.5
CLA e	1.7	
Bridge h	1.8	11.1
Bridge g	1.6	

From the results presented in Table 6.2, it is possible to verify that the transistor arrangement restructuring is also an alternative to mitigate the degradation caused by HCI effect. The results show savings in the average fall delay degradation up to 50%. In this case, the degradation is strongly related to the average amount of transistors in the delay arcs.

Although the above remarks may be considered complementary, the guidelines to deal with NBTI and HCI can be applied together at same gate since such effects act in different CMOS logic gate planes. On the other hand, the complementarity solution of HCI and TDDB in the pull-down NMOS plane let the designer to choose the proper guideline to be followed according to the severity of each effect.

Considering the difficulty in obtaining the signal and switching behavior before the circuit mapping, the transistor arrangement restructuring can be said to be an efficient design technique to be used in logic gate design. Another important aspect related to the proposed CMOS gate design approach is the fact the no area penalty has been introduced. The proposed technique is also easily used together with other techniques already presented in the literature.

6.2 Design More Reliable Circuits

Some insights about the reliability aspect at circuit abstraction level are discussed in the following. In such aspect, the importance of the pin reordering in symmetric Boolean functions is illustrated through electrical simulations. The second aspect explored herein is a comparative analysis of degradation behavior between the design of Boolean functions using single complex stages and multiple simple stages. This second analysis can be considered as a simplified behavior of digital circuits more complex than individual gates.

6.2.1 Pin Reordering in Symmetrical Functions

Following the approach used in transistor arrangement restructuring, discussed above, the importance of pin reordering in symmetric Boolean functions also explores the particularities of each class (static and dynamic degradations) of aging mechanism individually, being also presented in the form of guidelines. The proposed pin

reordering technique that deal to NBTI and TDDB can be summarized by the following gate design guideline:

- ***To prevent NBTI and TDDB degradation, the transistors with higher ON probability (input '1' for NMOS and input '0' for PMOS) must be placed far from the power supplies.***

All discussions presented in Section 6.1, to validate the transistor arrangement restructuring approach, is also appropriated to the pin reordering in symmetrical functions. In summary, the previous discussion concludes that the transistors connected to the power rails suffer more NBTI and TDDB degradation than the others ones in the gate arrangement.

While the main objective of previous approach was to show the potential of restructuring the transistor network to mitigate the wearout effects, this solution is interesting to show the higher signal probability influence in static aging effect degradation. As mentioned before, when this strategy is applied to the pull-up PMOS plane, both NBTI and TDDB degradations are mitigated. However, when the pin reordering is applied to the pull-down NMOS plane, only TDDB degradation is affected because NBTI degradation acts only in PMOS devices.

Table 6.3 presents the electrical simulation results of a 2-input NOR2 gate, depicted in Figure 5.7, taking into account different input signal probabilities. The first hypothesis is contradictory to the pin reordering suggestion, whereas the second hypothesis follows the guideline.

Table 6.3 – NOR gate degradation when different input signals probabilities are applied.

Input Signal	Signal Probability	Average Rise Delay Degradation due to NBTI (%)	Gate Tunneling Current due to TDDB (μA)
a	0.25	16.7	5.25
b	0.75		
a	0.75	15.1	2.88
b	0.25		

From the results presented in Table 6.3, it is possible to verify the influence of pin reordering in aging degradation. The results in terms of the average rise degradation delay due to NBTI show savings around 9.5 %. In terms of gate tunneling current due to TDDB, the saving is more significant, achieving 45% of savings. This more expressive saving in TDDB follows the temporal behavior of both mechanisms, discussed in Chapter 3. When a NAND gate is evaluated, similar TDDB behavior is verified, while the NBTI degradation is not affected since the PMOS transistors are in parallel arrangement.

To evaluate the influence of the pin reordering in HCI degradation, the signal probability used in the static degradation analysis has to be replaced by the switching probability parameter. One more time, the switching probability concept used in this analysis is defined as an input signal switching that causes an output switching, and the following analysis is centered in the pull-down NMOS plane due to the higher HCI degradation in this transistor instantiation. The pin reordering solution to mitigate HCI degradation can be summarized by the following gate design guideline:

- ***To prevent HCI degradation, the transistors with higher switching probability must be placed far from output nodes.***

Considering the exponential dependence of V_{ds} and the switching necessity, it is intuitive that the transistors connected at the output node suffer more HCI degradation than the other ones in a transistor stack. From this perspective, an efficient way to mitigate HCI degradation is to place the inputs with higher switching probabilities far from the output node. Similarly to the static degradation effects, all discussions presented in Section 6.1, to validate the transistor arrangement restructuring approach, is also appropriated to the pin reordering solution.

Electrical simulations have also been carried out to exemplify the reliability improvement of the pin reordering. The conditions used to perform these simulations follow the definitions presented in Section 6.1. However, in this experiment, different switching probabilities are explored. Table 6.4 presents the electrical simulation results of NAND gate, depicted in Figure 5.7, considering different input signal switching probabilities.

Table 6.4 – HCI degradation in NAND gate applying different input signals switching activity.

Normalized Signal Switching Probability of Transistor Connected to Output Node	Fall Delay Degradation due to HCI (%)
1	9.0
0.8	8.0
0.6	6.8
0.4	5.5
0.2	3.8

The maximum threshold voltage degradation due to HCI effect, considering the normalized signal switching probability presented in Table 6.4, is 50 mV. The threshold voltage degradation to other signal switching probabilities is computed according to Equation (3.4). The results presented in Table 6.4 shows the potential degradation savings in fall delay due to HCI effect. A difference in switching probability from 0.2 to 1 can results in 57% of degradation savings in fall delay.

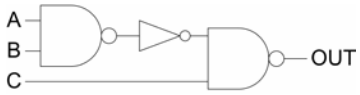
As presented in the experiments reported in Table 6.3 and in Table 6.4, the pin reordering is an excellent alternative to deal with aging effects. This approach has already been reported considering HCI and NBTI (DASGUPTA. 1996; WANG. 2007; KIAMEHR. 2012). As in transistor arrangement restructuring, there is no area penalty by reordering the input signals. The main difference in these two approaches is that the pin reordering is performed at logic synthesis stage while the transistor arrangement restructuring is a logic gate design solution.

6.2.2 Complex Logic Functions Design Analysis

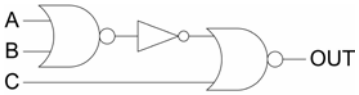
A complex logic function can be designed in only one single complex stage or in multiple simple stages. No analysis regarding the robustness to the aging effects was performed in order to find out if there is a better approach so far. From the discussed aging mechanisms characteristics, it is possible to say that the logic planes that present

transistor stacks tend to be more robust against aging degradation than the planes that have only single devices between the power rail and the output node. Such statement induces the conclusion that complex functions designed in one single stage present smaller aging degradation than the same function designed in multiple stage solution. Another important aspect that can be summarized is that the designing of a logic function with more than one stage usually leads to a higher device count, increasing the number of transistors under aging degradation.

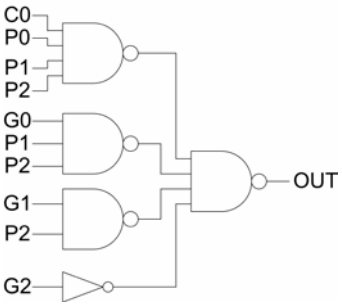
From this perspective, four logic functions have been designed in a multiple stages version, and electrical simulations were carried out to extract the degradation behavior. For two of those functions, two different versions of multiple stage designs were evaluated. The multiple stage design solutions are illustrated in Figure 6.1.



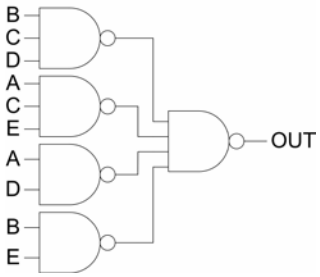
NAND3 MS



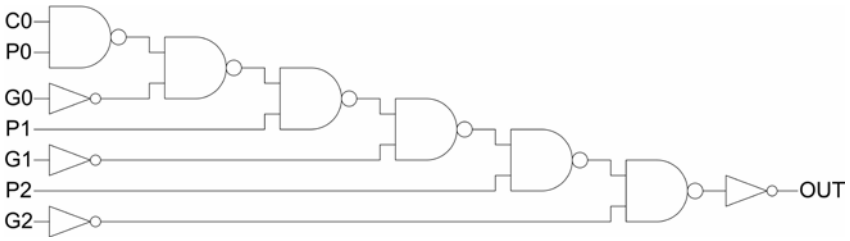
NOR3 MS



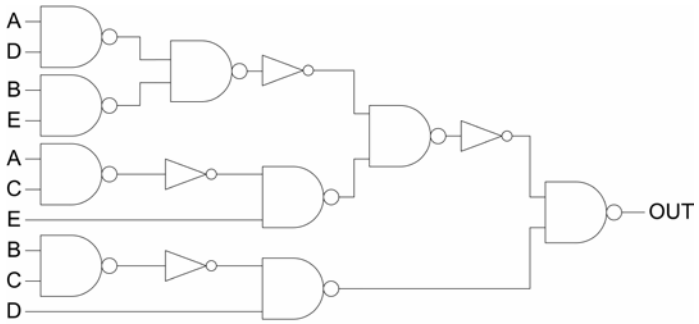
CLA MS1



Bridge MS1



CLA MS2



Bridge MS2

Figure 6.1 – Multiple stage design solution.

The electrical simulations consider the same conditions used in previous reported results. All inputs have the same switching activity and signal probability of 0.5. In order to obtain the switching activity and the signal probability of internal nodes in the multiple stages solutions, the circuits were described using a flatten transistor netlist and the probabilities were computed according to procedures described in Chapter 5.

Table 6.5 presents the simulation results of multiple stages gates depicted in Figure 6.1 and the respective single stage gates illustrated in Figure 5.7.

Table 6.5 – Aging degradation in single and multiple stages design solutions.

Logic Gate	Normalized Average Delay Degradation (%)			Gate Tunneling Current due to TDDB
	NBTI	HCI	NBTI + HCI	
NAND3	6.5	0.6	7.2	1.17
NAND3 MS	7.3	2.0	9.3	8.62
NOR3	6.9	1.3	8.1	1.25
NOR3 MS	7.5	2.2	9.8	8.62
CLA	4.6	1.3	5.9	1.95
CLA MS1	7.8	1.1	9.0	8.40
CLA MS2	7.4	1.6	9.1	10.26
Bridge b	6.2	0.9	7.0	4.75
Bridge MS1	7.6	1.3	9.0	10.14
Bridge MS2	7.9	2.1	10.1	42.13

Differently from other analysis, where the fall and rise delays were observed according to the degradation mechanism, Table 6.5 presents the average delay degradation considering both cases. As the NBTI affects only PMOS transistors, only the rise delay is degraded. In fact, a small improvement is verified in fall delay when NBTI degradation is considered. This NBTI behavior will be discussed in next section as a secondary aspect associated to the degradation mechanisms. The complementary behavior is verified in HCI analysis. As the data presented in Table 6.5 considers the average of rise and fall delays, it is expected that this average values assume almost half of the degradation compared to the degradation when only rise or fall delay are taken into account in respect to the respective aging effect. This observation justifies the smaller degradation values when compared to the results presented in Table 6.3 and in Table 6.4.

The results shown in Table 6.5 confirm the points discussed at the beginning of this section. The multiple stage solutions presented higher degradation than the single complex stage designs. In the delay analysis, the differences between both approaches can achieve 50%. In the gate tunneling current analysis, the increment caused by the simpler structures in multiple stage design is even worse, achieving in the worst case almost one order of magnitude of difference.

The design of a complex Boolean function can be considered as a simplification of a digital circuit design. These complex functions can be designed as a set of simple interconnected logic gates. In this perspective, the circuit that is designed using the standard cell design flow can be also considered as a large set of interconnected logic

gates. From this perspective, the use of complex gates in circuit design can be an alternative to produce more reliable circuits in terms of gate oxide degradation.

6.2.3 Secondary Effects

As discussed early, the NBTI degradation increases de rise gate delay. However, this degradation in V_{th} of PMOS transistor also reflects in a small decrease in fall gate delay. This small decrease in fall delay is exemplified in single stage gates of Table 6.6. This could be expected as the transistor with a higher V_{th} tends to be cutoff early and as consequence, the fall output transition is accelerated, reducing the gate delay. The same behavior is verified in HCI effect, but with complementary edge delay.

From Table 6.6 is also possible to observe that the rise delay degradation is not so expressive in multiple stage gates as in single stage ones. The output rise delay in multiple stage solution is the caused by fall delay in previous stage. As the pull-down plane does not suffer NBTI degradation, the fall delay of previous stage compensates some of the logic gate rise delay degradation. Similar analysis can be performed to explain the fall delay degradation in multiple stage versions. A fall transition in output node is caused by a rise transition in previous stage. This rise transition in previous stage senses the degradation of pull-up PMOS transistors. As consequence, the output fall transition experiences some degradation. This balance between fall and rise delay degradations in multiple stages could be considered positive in terms of equivalent rise and fall delay degradations. However, the average delay degradation in multiple stages versions presents worse results when compared to single complex stage. Also, in real circuit, a path is composed by several stages, that intuitively balances the degradation.

Table 6.6 – Rise and fall delay degradation due to NBTI in single and multiple stage gates.

Logic Gate	Normalized Delay Degradation (%)		
	Rise	Fall	Average
NAND3	14.1	0	6.5
NAND3 MS	11.6	3.3	7.3
NOR3	17.9	- 1.9	6.9
NOR3 MS	12.7	3.1	7.5
CLA	17.9	- 3.0	4.6
CLA MS1	8.7	7.0	7.8
CLA MS2	9.3	5.8	7.4
Bridge b	18.5	- 2.4	6.2
Bridge MS1	9.4	5.9	7.6
Bridge MS2	9.6	6.2	7.9

The fall delay reduction due to NBTI observed in single stage gates is not the only positive aspect verified due to aging effects. The last characteristic explorer in this section refers to the positive aspects of aging effects in circuit design. The subtreshold current discussed in Section 2.2.1 presents an exponential dependence to V_{th}. A direct aspect to be considered is that the V_{th} increment due to NBTI and HCI implies lower

subthreshold current over time. Table 6.7 illustrates the average subthreshold current reduction due to NBTI and HCI effects considering the same degradation severity of previous experiments. However, this reduction in subthreshold current is almost insignificant in relation to the increment in gate tunneling current due to TDDB effect.

Such high gate tunneling current due to TDDB affects the circuit signal integrity. In extreme cases of hard breakdown, the logic functionality can be compromised. While the progressive breakdown is characterized, the elevated gate tunneling current acts as a resistive divider and the voltages do not attain at their nominal value. In other words, the output node of logic gates does not attain the supply voltage for logic value ‘1’ and ground voltage for the logic value ‘0’. This signal degradation reduces the voltage excursion, reducing so the gate delay. Table 6.7 also describes the average date delay reduction due to TDDB. In some cases, this improvement achieves almost 4%. However, as the gate currents increase, a hard breakdown is observed and the circuit functionality can be compromised.

Table 6.7 – Secondary effects of aging mechanism.

Logic Gate	Average Subthreshold Current Reduction due to NBTI (%)	Average Subthreshold Current Reduction due to HCI (%)	Average Gate Delay Reduction due to TDDB (%)
NAND3	9.3	21.8	0.9
NAND3 MS	16.8	28.0	3.2
NOR3	9.9	35.3	2.7
NOR3 MS	17.9	33.0	3.9
CLA	10.3	23.9	2.1
CLA MS1	7.3	32.5	4.0
CLA MS2	10.1	35.1	1.6
Bridge v2	9.9	26.8	2.9
Bridge MS1	8.6	32.4	3.3
Bridge MS2	14.4	31.0	1.0

7 CONCLUSIONS

This thesis has explored solutions to design more reliable circuits in nanometer technologies. With the technology scaling, new challenges are faced out to circuit designers. The aging effects are the main cause of circuit degradation over time. To guarantee the correct circuit functionality during its entire lifetime, aging effects have to be considered in the circuit design stage.

Two approaches are explored in this thesis to address solutions to design more reliable circuits. The first solution proposes a logic gate aging cost to be used by logic synthesis algorithms. The second approach explored circuit design techniques. In this scope, a transistor arrangement restructuring has been presented. The importance of the input pin reordering according to the input signal and switching probabilities has been quantified. Finally, circuit design considerations are discussed based on complex logic gates design.

The proposed approaches were verified through electrical simulations. The aging effects degradation has been computed using analytical models adapted to consider the real time that the devices are under stress. This concept has explored the transistor arrangement and signal and switching probability. The obtained results have shown that the proposed aging cost provides a good agreement to delay and gate current degradation. The circuit design approaches have shown good degradation recovery and the flexibility to be used together with other techniques.

7.1 Summary of Contributions

The major thesis contributions related to more robust IC design against aging effects are summarized below.

- **Gate aging cost**: It has been presented the concepts and procedures associated to the development of the logic gate aging cost. This aging cost is an important figure-of-metric to allow the exploration of aging effects degradation at initial steps of standard cell design flow. It can be also used to compute the expected degradation of a digital circuit without requiring electrical simulations.
- **Transistor arrangement restructuring**: A logic gate design technique has been proposed to produce more robust gates. This technique explores the transistor stack robustness against aging effect in series-parallel arrangement. The technique presents no area penalties and electrical simulation results have demonstrated good degradation savings.

- **Quantification of the importance of pin reordering approach**: The pin reordering is an intuitive technique that also explores the aging degradation mitigation in series transistors association. The amount of degradation recovered has been quantified to three aging effects, and the results show that it is essential explore this approach at circuit level in order to produce more reliable circuits.
- **Evaluation of complex logic function designs**: A comparative analysis between different approaches of how to design a complex Boolean function provides initial insights about the benefits of using single stage complex gates to produce more reliable circuits. From this analysis, the main benefit in using single complex stage is related to the transistor stack robustness against aging effects. To perform the analysis, algorithms to compute the signal and switching probabilities of the multiple stage circuits have been developed.

7.2 Future Works

The contributions of this thesis do not give a complete picture to the aging aware design problem. Various extensions of this work are possible, some of which are discussed below.

- **Implementation of technology mapping algorithm that considered the logic gate aging cost**: To allow the efficient utilization of the proposed logic gate aging cost, the development or adaption of technology mapping algorithms are necessary. For more efficient result, the influence of input slope and output capacitance should be evaluated in the proposed cost. The logic gate aging cost associated to technology mapping algorithms will treat the aging problem at a very beginning in the design flow. This initial treatment has a great potential to produce more reliable circuits.
- **Implementation of an analysis tool that is capable to estimate the degradation level of circuits considering the logic gate aging cost**: Another way to explore the gate aging cost is in association to static timing analysis and aging degradation static analysis based on the intermediate nodes signal and switching probabilities. The algorithms used to compute the aging degradation of the multiple stage logic function can be considered an initial point, but they treat the problem at transistor level. This consideration does not allow the application of those algorithms in large circuits. More effort should be place in this scope to generate the aging degradation circuit analysis. In this approach, the evaluation of input slope and output capacitance should also be investigated.
- **To compare the efficiency of the use of complex gates in large benchmarks circuits**: The initial analysis of using single stage complex gate to reduce the aging effect degradation has to be extended to large circuits to confirm the initial insights presented previously. The large circuit analysis will allow a complete analysis considering even the penalties in routing complexity and the presence of the complex functions in circuit benchmarks.
- **To incorporate the new upcoming aging effect in proposed analysis**: As the technology is in constant scaling, new degradation mechanisms are

becoming relevant. In high-κ devices, the PBTI in NMOS transistors achieve almost the same order of degradation magnitude than NBTI in PMOS devices. The device dimension shrinking introduces the concept of cold carrier effect in transistor switching behavior. The effect of radiation in silicon devices is also increasing in importance in each new technology process. Although Total Dose Ionization (TID) is decreasing importance in nanometer technologies, new upcoming wearout aspects related to radiation effects can appears and should be computed in overtime device degradation. These mechanisms have to be introduced in the aging effect analysis to provide the correct aging behavior in new nanoscaled technology process.

REFERÊNCIAS

ABELLA, J.; VERA. X.; GONZALEZ. A. Penelope: The NBTI aware processor. In: INT. SYMP.MICROARCHITECTURE. 2007. **Proceedings...** [S.l.]. 2007. p. 85–95.

ABOUZEID, P. et al. Logic synthesis for automatic layout. In: THE EUROPEAN EVENT IN ASIC DESIGN. 1992. **Proceedings…** [S.l:s.n.]. 1992. p. 146-151.

AITKEN, R. C. The Challenges of correlating silicon and models in high variability CMOS processes In: INTERNATIONAL SYMPOSIUM ON PHYSICAL DESIGN. 2009. **Proceedings…** [S.l:s.n.]. 2009. p. 181-182.

BASTOS, R. P. "Design a Robust Microprocessor to Soft Errors". **Master Thesis.** Instituto de Informática. UFRGS. 2006.

BERKELAAR, M.; JESS, J. Technology Mapping for Standard-cell Generators. In: INTERNATIONAL CONFERENCE COMPUTER-AIDED DESIGN. 1988. Santa Clara. USA. **Digest of Technical Papers**. New York. USA: IEEE. 1988. p. 470-473.

BERNSTEIN, J. B. Electronic Circuit Reliability Modeling. **Microelectronics Reliability**. vol 46, n. 12, p. 1957-1979. Dec. 2006.

BHUSHAN, M. et al. Ring oscillators for CMOS process tuning and variability control. **IEEE Transactions on Semiconductor Manufacturing**. vol. 19 no. 1. p. 10-18. Feb. 2006

BORAK, S. et al. Parameter variations and impact on circuits and microarchitecture. In: DESIGN AUTOMATION CONFERENCE. 2003. **Proceedings…** [S.l:s.n.]. 2003. p. 338-342.

BORAK, S. et. al. Parameter variation and impact on circuits and microarchitecture. In: DESIGN AUTOMATION CONFERENCE. 2003. **Proceedings…** [S.l:s.n.]. 2003. p. 338-342.

CARTIER, E.; KERBER, A. Stress Induced Leakage Current and Defect Generation in nFETs with HfO2/TiN Gate Stacks during Positive Bias Temperature Stress, INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM. **Proceedings...** p. 486-492, 2009.

CHANG, C. J. et. al. Layout-Driven Hot-Carrier Degradation Minimization Using Logic Restructuring Techniques. In: DESIGN AUTOMATION CONFERENCE. 2001. **Proceedings…** [S.l:s.n.]. 2001. p. 97-102.

CHEN, Z; KOREN, I. Technology Mapping for Hot-Carrier Reliability Enhancement. **Proceedings of the SPIE**. p. 42-50. 1997.

CHEN. G. et al. Dynamic NBTI of PMOS transistors and its impact on device lifetime. In: RELIABILITY PHYSICS SYMPOSIUM. 2003. **Proceedings...** [S.l.]. 2003. p. 196-202.

CHOUDHURY, M.; CHANDRA, V.; MOHANRAM, K.; AITKEN, R. Analytical model for TDDB-based performance degradation in combinational logic, DESIGN, AUTOMATION & TEST IN EUROPE CONFERENCE & EXHIBITION (DATE), **Proceedings...** p.423-428, 2010.

COLINGE. J. P. **Silicon-on-Insulator technology**. 2nd Edition. Springer. 1997

CORNELIUS, C. et al. Encountering GOB with Shadow Transistors to Increase Reliability, SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEM DESIGN, **Proceedings...** p. 1-6. 2008.

CORREIA, V.; REIS, A. I. Advanced technology mapping for standard-cell generators. In: SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEM DESIGN. 2004. Porto de Galinhas. Brasil. **Proceedings…**Los Alamitos: IEEE. 2004. p. 254-259.

CRUPI, F. et al. Correlation between stress-induced leakage current (SILC) and the HfO2 bulk trap density in a SiO2/HfO2 stack, INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM, **Proceedings...** p. 181– 187, 2003.

DA ROSA JUNIOR, L. S. ; SCHNEIDER, F. ; RIBAS, R. P. ; REIS, A. I. Switch Level Optimization of Digital CMOS Gate Networks. 10TH IEEE INTERNATIONAL SYMPOSIUM ON QUALITY ELECTRONIC DESIGN, **Proceedings...** p. 324-329, 2009.

DASGUPTA, A.; KARRI, R. Hot-Carrier Reliability Enhancement via Input Reordering and Transistor Sizing. In: DESIGN AUTOMATION CONFERENCE. 1996. **Proceedings…** [S.l:s.n.]. 1996. p. 819-824.

DENAIS. M. et. al. On-the-fly characterization of NBTI in ultra-thin gate oxide PMOSFET's. In: IEEE INT. ELECTRON DEVICES MEET. **Proceedings...** [S.l.] IEEE. 2004, p. 109–112.

DOBRESCU, L.; PETROV, M.; DOBRESCU, D.; RAVARIU, C. Threshold voltage extraction methods for MOS transistors, INTERNATIONAL SEMICONDUCTOR CONFERENCE (CAS), **Proceedings...** vol. 1, p.371-374 vol.1, 2000

DRESSENDORFER, P. V. **Ionizing Radiation Effects in MOS Devices and Circuits**. New York: John Wiley & Sons. 1989.

FANG, P. et. al. Design in Hot-Carrier Reliability for High Performance Logic Applications. In: IEEE CUSTOM INTEGRATED CIRCUITS CONFERENCE. 1998. **Proceedings...** New York: IEEE. 1998. p. 525-531.

FRENCH, R. H. et al. High Index Immersion Lithography with Second Generation Immersion Fluids to Enable Numerical Apertures of 1.55 for Cost Effective 32nm Half Pitches. **Proceedings of SPIE**. vol. 6520. p. 1-12. Mar. 2007.

GUAN, B.; SECHEN, C. Large standard cell libraries and their impact on layout area and circuit performance. In: INTERNATIONAL CONFERENCE ON COMPUTER DESIGN. 1996. Austin. USA. **Proceedings…** New York: IEEE. 1996. p. 378-383.

HAO, H.; McCluskey, E. J. Analysis of gate oxide shorts in CMOS circuits, **IEEE Transactions on Computers** , vol.42, no.12, p.1510-1516, 1993.

HUANG, L.; WONG, M. D. F. Optical proximity correction (OPC): friendly maze routing. In: DESIGN AUTOMATION CONFERENCE. 2004. **Proceedings…** [S.l:s.n.]. 2004. p. 186-191.

HUANG. W. et. al. Compact thermal modeling for temperature-aware design. In: DESIGN AUTOMATION CONFERENCE. 2004. **Proceedings…** [S.l.]. New York,. 2004. p. 878-883.

HUARD, V. et al. Design in Reliability Approach for Hot Carrier Degradations in Advanced Nodes. **IEEE Transactions on Device and Materials Reliability**. vol. 7 no. 4. pp. 558-570. Dec. 2007

HUARD. V.; et al. NBTI degradation: From physical mechanisms tomodelling. **Microelectron. Reliab.** vol. 46, no. 1, p. 1–23, Jan. 2006.

INTEL COOPERATION WEBSITE. Available at: http://www.intel.com/technology/mooreslaw/. Visited on: Aug. 2010.

ISLAM, A. E. et al. Essential Aspect of Negative Bias Temperature Instability (NBTI). **ECS Transactions**. vol. 35 no. 4. p. 145-174. 2011

JHAVERI, T. et al. Co-Optimization of Circuits. Layout and Lithography for Predictive Technology Scaling Beyond Gratings. **IEEE Trans. on CAD of Integrated Circuits and Systems**. New York. v.29. n.4. p. 509-527. Apr. 2010.

JIANG, W. Hot Carrier Reliability Assessment in CMOS Digital Integrated Circuits. **Thesis**, 1998.

JOHNSTON. A. Scaling and Technology Issues for Soft Error Rates. In: RESEARCH CONFERENCE ON RELIABILITY. 2000. **Proceedings…** [S.l.]. 2000. p.1-8.

KAGARIS, D.; HANIOTAKIS, T. Transistor-level optimization of supergates, 7TH INTERNATIONAL SYMPOSIUM ON QUALITY ELECTRONIC DESIGN (ISQED), **Proceedings...** p.684-690, 2006.

KAO, J. T.; CHANDRAKASAN, A. P. Dual-threshold voltage techniques for low-power digital circuits. **IEEE Journal of Solid State Circuits**. New York. v.35. n.7. p. 1009-1018. July 2000.

KARL. E. et. al. Compact in-situ sensors for monitoring negative-bias-temperature-instability effect and oxide degradation. In: IEEE INT. SOLID STATE CIRCUITS CONF. 2008. **Proceedings…**[s.l.]: IEEE. 2008, p. 410–411.

KEANE. J. et al. An All-in-One Silicon Odometer for Separately Monitoring HCI. BTI. and TDDB. **IEEE Journal of Solid State Circuits**. New York. v. 45, n. 4. p. 817-829. Apr. 2010.

KIAMEHR. S.; FIROUZI. F.; TAHOORI. M. B. Input and transistor reordering for NBTI and HCI reduction in complex CMOS gates. In: GREAT LAKES SYMPOSIUM ON VLSI. 2012. **Proceedings…** [S.l.]. New York. 2012. p. 201-206.

KITTI, J. A. et al. High-k dielectrics for future generation memory devices. **Microelectronic** Engineering. [S.l]. v.86. n.7-9. p. 1789-1795. Jul.-Sep. 2009.

LABEL. K. A. et al. A roadmap for NASA's radiation effects research in emerging microelectronics and photonics. In: AEROSPACE CONFERENCE. 2000. **Proceedings...** [S.l.]. 2000. p. 535-545.

LEBLEBICI, Y. Design Consideration for CMOS Digital Circuits with improved Hot-Carrier Reliability. **IEEE Journal of Solid State Circuits**. New York. v.31. n.7. p. 1014-1024. July 1996.

LI, P.; HAJJ, I. N. Computer-Aided Redesign of VLSI Circuits for Hot-Carrier Reliability. In: INT. CONF. ON COMPUTER DESIGN. 1993. **Proceedings...** [S. l.]: IEEE. 1993. p. 534-537.

LI, P.; HAJJ, I. N. Computer-Aided Redesign of VLSI Circuits for Hot-Carrier Reliability. **IEEE Trans. on CAD of Integrated Circuits and Systems**. New York. v.15. n.5. p. 453-464. May 1996.

LI, X; QIN, J.; BERNSTEIN, J. B. Compact Modeling of MOSFET Wearout Mechanisms for Circuit-Reliability Simulation. **IEEE Transactions on Device and Materials Reliability**. vol. 8 n. 2. p. 98 - 121. Mar. 2008

LINDER. B. P. et al. Voltage dependence of hard breakdown growth and the reliability implication in thin dielectrics. **IEEE Electron Device Letters**. vol. 23. n. 11. p. 661–663. Nov. 2002.

LOU, H. Circuit Level Delay Modeling Considering both TDDB and NBTI. In: INTERNATIONAL SYMPOSIUM ON QUALITY ELECTRONIC DESIGN, **Proceedings...** p.1-8, 2011.

LUO, H. et al. Circuit-level delay modeling considering both TDDB and NBTI, 12TH INTERNATIONAL SYMPOSIUM ON QUALITY ELECTRONIC DESIGN (ISQED), **Proceedings...** p.1-8, 2011.

MACK, C. A. **Field Guide to Optical Lithography**. 1st Edition. SPIE Publications. 2006.

MARQUES, F. S. et al. DAG Based Library-Free Technology Mapping. In: ACM GREAT LAKES SYMPOSIUM ON VLSI. 2007. Lago Maggiore. Italy. **Proceedings…** [S.l.]: ACM. 2007. p. 293-298.

MASSENGILL. L. W. et al. Analysis of Single-Event Effects in Combinational Logic – Simulation of the AM2901 Bitlice Processor. **IEEE Transactions on Nuclear Science.** vol. 47. n. 6. p. 2609-2615. Dec. 2000.

MATSUNAGA, J. et al. Characterization of two step impact ionization and its influence on NMOS and PMOS VLSIs. In: INTERNATIONAL ELECTRON DEVICE MEETING. 1980. **Technical Digest** [S.l:s.n.]. 1980. p. 736-739

MISTRY, K. R. et al. Circuit Design Guidelines for n-channel MOSFET Hot Carrier Robustness. **IEEE Transactions on Electron Devices**. vol. 40. no. 7. p. 1284-1295. July 1993.

MONSIEUR. F.et al. A thorough investigation of progressive breakdown inultra-thin oxides.physical understanding and application for industrial reliability assessment. In: INT. RELIABILITY PHYSICS SYMPOSIUM. 2002. **Proceedings...** [S.l.]. 2002. pp. 45–54.

MOORE, G. E. No exponential is forever: but "Forever" can be delayed! In: IEEE INT. CONF. SOLID STATE CIRCUITS. 2003. **Proceedings…** [S.l.]: IEEE. 2003. p. 20-23.

MUTOH, S. et al. 1-V Power Supply High-speed Digital Circuit Technology with Multi-threshold Voltage CMOS. **IEEE Journal of Solid State Circuits**. New York. v.30. n.8. p. 847-854. Aug. 1995.

NARENDRA, S. et al. Forward Body Bias for Microprocessors in 130-nm Technology Generation and Beyond. **IEEE Journal of Solid State Circuits**. New York. v.38. n.5. p. 696-701. May 2003.

NARENDRA, S. G.; CHANDRAKASAN, A. **Leakage in Nanometer CMOS Technologies**. New York: Springer, 2006. 307 p.

NICOLAIDIS. M Time Redundancy Based Soft-Error Tolerance to Rescue Nanometer Technologies. In: VLSI TEST SYMPOSIUM. 1999. **Proceedings...** [S.l.]. 1999. pp. 86.

NIGAM. T. et al. Accurate model for time-dependent dielectric breakdown of high-k metal gate stacks. In: INT. RELIABILITY PHYSICS SYMPOSIUM. 2009. **Proceedings...** [S.l.]. 2009. pp. 523–530.

OGURA, S. et al. Design and Characteristics of the lightly doped drain-source (LDD) insulated gate field effect transistor. **IEEE Transactions on Electron Devices**. vol. 27. no. 9. p. 1359-1367. Aug. 1980.

ORSHANSKY, M. et al. **Design for Manufacturability and Statistical Design: a constructive approach**. New York: Springer. 2008.

PALLISGAARD, H. Rethinking the Cell Library Design Process for Advanced Nanometer Process Technologies. **Chip Design Magazine**. Available at: <http://chipdesignmag.com/display.php?articleId=3378>. Visited on: Sep. 2012.

PANG, L.; NIKOLIC, B. Measurements and Analysis of process variability in 90nm CMOS. **IEEE Journal of Solid State Circuits**. New York. v.44. n.5. p. 1655-1663. May 2009.

PARK, H. et al. Improved Hot Carrier Reliability Characteristics of MOSFET with High-K Gate Dielectric by Using High Pressure Deuterium Post Metalization Annealing. **Japanese Journal of Applied Physics**. vol. 46 no. 33. p. 768 - 788. Aug. 2007.

PETERSON. W. **Error-correcting codes.** Cambridge. 1980.

PRASAD, C. et al. Dielectric Breakdown in a 45 nm High-K/Metal Gate Process Technology, INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM, **Proceedings...** p. 667-668, 2008.

QUADER, K. N. et. al. Hot Carrier Reliability Design Guidelines for CMOS Logic Circuits. **IEEE Journal of Solid State Circuits**. New York. v.29. n.3. p. 253-262. Mar. 1994.

RABAEY, J. M.; CHANDRAKASAN, A.; NIKOLIC, B. **Digital Integrated Circuits**. 2nd Edition. Prentice-Hall. 2003.

RICCI, A.; DE MUNARI, I.; CIAMPOLINI, P. An Evolutionary Approach for Standard-Cell Library Reduction. In: GREAT LAKES SYMPOSIUM ON VLSI. 2007. **Proceedings...** [S. l.]: ACM. 2007. p. 305-310.

ROY, K. et al. Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits. **Proceedings of the IEEE**. New York. v. 91. n. 2. p. 302-327. Feb. 2003.

RUDENKO, T. et al. On the MOSFET Threshold Voltage Extraction by Transconductance and Transconductance-to-Current Ratio Change Methods: Part I - Effect of Gate-Voltage-Dependent Mobility, **IEEE Transactions on Electron Devices**, vol.58, no.12, p.4172-4179, 2011.

SAEMROW, H. et al. Selective redundancy to improve reliability and to slow down delay degradation due to gate oxide breakdown, DESIGN AND DIAGNOSTICS OF ELECTRONIC CIRCUITS & SYSTEMS (DDECS), 2012 IEEE 15TH INTERNATIONAL SYMPOSIUM ON, **Proceedings...** p.12-15, 2012.

SAEMROW, H. et al. Twin Logic Gates - Improved Logic Reliability by Redundancy concerning GOB", SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEM DESIGN, **Proceedings...** p. 12-15 , 2009

SAKURAI, T. et al. Hot carrier generation in submicrometer VLSI environment. **IEEE Journal of Solid State Circuits**. New York. v.21. n.1. p. 187-192. Feb. 1986.

SCOTT, K.; KEUTZER, K. Improving Cell Libraries for Synthesis. In: IEEE CUSTOM INTEGRATED CIRCUITS CONFERENCE. 1994. San Diego. USA. **Proceedings...** New York: IEEE. 1994. p. 128-131.

SEGURA, J.; DE BENITO, C.; RUBIO, A.; HAWKINS, C.F. A detailed analysis of GOS defects in MOS transistors: testing implications at circuit level, INTERNATIONAL TEST CONFERENCE, **Proceedings...** p.544-551, 1995.

SHEN. C. et al. Characterization and physical origin of fast Vth transient in NBTI of pMOSFETs with SiON dielectrics. In: IEEE ELECTRON DEVICES MEETING. 2006. **Proceedings...** [S.l.]. IEEE. 2006, p. 1–4.

SILVA, D. N.; REIS, A. I.; RIBAS, R. P. CMOS logic gate performance variability related to transistor network arrangements. **Microelectronics Reliability**. vol 49. NO. 9-11. p. 977-981. Nov. 2009.

SIVAKUMAR, S. Lithography Challenges for 32nm Technologies and Beyond. In: INTERNATIONAL ELECTRON DEVICE MEETING. 2006. **Technical Digest** [S.l:s.n.]. 2006. p. 1-4

STATHIS, J. et al. Reliability of ultra-thin oxides in CMOS circuits. **Microelectronics Reliability**. vol 43. p. 1353-1360. 2003.

SYLVESTER, D.; AGARWAL, K.; SHAH, S. Variability in nanometer CMOS: Impact. analysis. and minimization. **Integration. the VLSI Journal**. vol. 41 no. 3. pp. 319-339. May 2008

TAKEDA. E.; YANG. C. Y.; MIURA-HAMADA. A. **Hot-Carrier Effects in MOS Devices**. Academic Press. 1995.

TAM, S.; KO, P. K.; HU, C. Lucky-electron model of channel hot electron injection in MOSFETs. **IEEE Transactions on Electron Devices**. vol. 31 no. 9. p. 1116-1125. Sep. 1984

TAROG, E. S. Design techniques to improve time dependent dielectric breakdown based failure for CMOS circuits. Thesis, 2010

TONG. Y. et al. A novel methodology to analyze time-dependent dielectric breakdown failure mechanism of copper/low-k interconnects. In: INTERNATIONAL

SYMPOSIUM ON THE PHYSICAL AND FAILURE ANALYSIS OF INTEGRATED CIRCUITS. 2009. **Proceedings...** [S.l.]. 2009. p. 719-722.

TU, C.H. et al. Transistor variability after CHC and NBTI stress in 90 nm pMOSFET technology, **Electronics Letters**, vol.45, no.16, p.854-856, 2009.

VATTIKONDA. R. Modeling and minimization of PMOS NBTI effect for robust nanometer design. In: DESIGN AUTOMATION CONFERENCE. 2006. **Proceedings...** [S.l.]. 2006. p. 1047-1052.

WAGNER, F. R.; REIS, A. I.; RIBAS, R. P. **Fundamentos de circuitos digitais**. 1.ed. Porto Alegre: Instituto de Informática da UFRGS: Sagra Luzzatto. 2006.

WANG, Y. et al. On the Efficacy of Input Vector Control to Mitigate NBTI Effects and Leakage Power. In: INTERNATIONAL SYMPOSIUM ON QUALITY ELECTRONIC DESIGN, **Proceedings...** p. 19-26, 2009.

WANG. W. et al. The impact of NBTI on the performance of combinational and sequential circuits. In: DESIGN AUTOMATION CONFERENCE. 2007. **Proceedings...** [S.l.]. 2007. p. 364-369.

WEI, L. et al. Design and Optimization of Dual-Threshold Circuits for Low-Voltage Low-Power Applications. **IEEE Trans. on VLSI Systems**. New York. v.7. n.1. p. 16-24. Mar. 1999.

WESTE, N.; HARRIS, D. **CMOS VLSI Design. A Circuits and Systems Perspective**. 3rd Edition. Addison Wesley. 2004.

WONG, A. K. **Resolution Enhancement Techniques in Optical Lithography**. 1st Edition. SPIE Publications. 2001.

YONG, L. et al. Computer-aided phase shift mask design with reduced complexity. **IEEE Transactions on Semiconductor Manufacturing**. vol. 9 no. 2. p. 170-181. May 1996

ZHAO, W.; CAO, Y. New generarion of Predictive Technology Model for Sub-45 nm Early Design Exploration, **IEEE Transactions on Electron Devices**, vol.53, no.11, p. 2816 – 1823, Nov. 2006.