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CMOS Digital Integrated Circuit Design Faced to NBTI and Other Nanometric Effects

Thesis presented in partial fulfillment of the requirements for the degree of Master in Microelectronics

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LIST OF ABREVIATIONS

BTI	Bias Temperature Instability
CMOS	Complementary Metal-Oxide-Semiconductor
CPLD	Complex Programmable Logic Device
DC	Direct Current
ESD	Electrostatic Discharge
FOTF	Fast On-The-Fly
FPGA	Field Programmable Gate Array
FPM	Fast Pulse Measurement
GND	Ground
HCI	Hot Carriers Injection
I/O	Input/Output
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
LET	Linear Energy Transfer
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NBTI	Negative Bias Temperature Instability
NMOS	Negative-Channel MOSFET
OFIT	On-The-Fly Interface Trap
OTF	On-The-Fly
PBTI	Positive Bias Temperature Instability
PMOS	Positive-Channel MOSFET
PTM	Predictive Technology Model
R-D	Reaction-Diffusion
SEE	Single-Event Effect
SET	Single-Event Transient
SEU	Single-Event Upset

SRAM	Static Random Access Memory
STA	Static Timing Analysis
TDDB	Time-Dependent Dielectric Breakdown
VLSI	Very Large Scale of Integration
WL	Word Line

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ABSTRACT

This thesis explores the challenges worsened by the technology miniaturization in fabrication and design of digital integrated circuits. The physical effects of nanometric regime reduce the production yield and shorten the devices lifetime, restricting the usefulness of standard design flows and threatening the evolution of CMOS technologies. This thesis exposes a consistent bibliographic review about the main aggressive physical effects of nanometric regime. NBTI has received special attention in reliability literature, so this text follows the same strategy, deeply exploring this aging effect. A broad set of NBTI evaluation and mitigation techniques are explained, including developed works in each one of these categories. The proposed circuit as NBTI evaluation technique allows the use of electrical simulation for circuit degradation analysis. The analysis of the transistors arrangement restructuring as a technique for NBTI degradation reduction shows satisfactory results, while does not restrict the use of other combined techniques.

Keywords: Microelectronics, NBTI, CMOS, Nanotechnology, Integrated Circuits, Digital Design, Logic Gate, Aging Effects, Reliability, Yield.

Projeto de Circuitos Integrados Digitais CMOS Face ao NBTI e Outros Efeitos Nanométricos

RESUMO

Esta dissertação explora os desafios agravados pela miniaturização da tecnologia na fabricação e projeto de circuitos integrados digitais. Os efeitos físicos do regime nanométrico reduzem o rendimento da produção e encurtam a vida útil dos dispositivos, restringindo a utilidade dos padrões de projeto convencionais e ameaçando a evolução da tecnologia CMOS como um todo. Nesta dissertação é exposta uma consistente revisão bibliográfica dos principais efeitos físicos parasitas presentes no regime nanométrico. Como o NBTI tem recebido destaque na literatura relacionada à confiabilidade de circuitos, este efeito de envelhecimento recebe destaque também neste texto, sendo explorado mais detalhadamente. Diversas técnicas de avaliação de redução do NBTI são demonstradas, sendo apresentados, em cada um destes tópicos, trabalhos desenvolvidos no âmbito desta dissertação e seus resultados. O circuito proposto como técnica de avaliação de NBTI permite uso de simulações elétricas para análise de degradação de circuitos. A análise da influência do rearranjo da estrutura de transistores para reduzir a degradação quanto ao NBTI apresenta bons resultados e não impede o uso de outras técnicas combinadas.

Palavras-chave: Microeletrônica, NBTI, CMOS, Nanotecnologia, Circuitos Integrados, Projeto de Circuitos Digitais, Portas Lógicas, Efeitos de Envelhecimento.

1 INTRODUCTION

Hardware systems can be developed over microcontroller platforms, programmable devices (FPGAS or CLPDS) or by integrated circuits (ICs) technologies. Digital ICs have been widely used due to their greater robustness against signal degradation. This characteristic carries a series of consequent benefits, like the ease of data control and storage, and the increased accuracy, reliability and lifetime.

CMOS has become the prevailing technology for very large scale integrated circuits, and its success is due to more than two decades of scaling to ever smaller dimensions for higher packing density, faster circuit speed, and lower power dissipation (TAUR, 1997).

However, the relentless scaling has brought not only benefits but also challenges. Mainly in nanometric regimes, a series of physical effects which previously was only a concern in analog circuits, now is disturbing also digital ICs (MCPHERSON, 2006)(KUHN, 2009).

These effects are intensified by technology scaling characteristics, like dimensions shrinking, structures atoms amount diminution, electric field rising, and supply voltage reduction. Due to these effects, there are a series of undesired reflexes in circuits, like growing variability, performance degradation and reliability drop.

The intensification of nanometric regime physical effects decreases the production yield and shortens the lifetime of devices. These consequences restrict the usefulness of standard project flows and threaten the convenience of the forthcoming smaller CMOS technologies (JAHVERI, 2010).

Among these new technologies challenges, the nowadays primary limiting factor of circuits' lifetime is the Negative Bias Temperature Instability (NBTI) (PAUL, 2006)(KUMAR, 2007)(WANG W., 2008)(GUARDIANI, 2009)(QI, 2010).

This thesis provides an overview about nanometric physical effects, and a deeper analysis on the Negative Bias Temperature Instability. Its main objective is to build the basis of knowledge about the established NBTI evaluation and mitigation techniques, providing a consistent background to the robustness increasing against this effect in digital ICs.

The remaining of this thesis is organized as follows:

Chapter 2 presents the overview about effects of interest in order to aware the reader about their broadness and about the position of NBTI among them.

Chapter 3 introduces the theory about NBTI, which composes the fundaments to the understanding of its evaluation and mitigation techniques, presented in following chapters.

Chapter 4 focuses in the NBTI evaluation techniques, as they are required to the proofing of all analysis.

Chapter 5 exposes the established robustness increasing techniques against NBTI, providing the tools to IC lifetime reliability enhancement.

Both chapter 4 and 5 have a final subsection detailing the related works developed in the scope of this thesis.

Finally, chapter 6 presents this thesis conclusions and future works.

2 NANOMETER SCALE EFFECTS IN DIGITAL INTEGRATED CIRCUITS

The CMOS technology scaling has raised the importance of previously negligible physical effects in digital integrated circuits, imposing many challenges (TAUR, 1997)(MCPHERSON, 2006)(KUHN, 2009) and even inspiring previews about the advance end (SKOTNICKI, 2005). These effects can be viewed as elements of two main categories: design and manufacturing challenges of nanometric regime, and lifetime reliability issues. Both categories will be briefly explored in the following subsections.

2.1 Nanometric Regime Design and Manufacturing Challenges

This is a set of challenges which will need to be overcome in order to produce a well functioning nanometric circuit, robust in its operational environment, but with no assumptions (yet) about very long period of usability. They can be understood as the elements behind three main concerns upon technology scaling: manufacturing variability, sensitivity increase, and undesired behavior of some electrical characteristics.

Manufacturing variability refers to the difficulty in reaching predictable and uniform results during each fabrication process step, like high pattern fidelity in lithography steps, or nearly constant amount of injected dopants in implantation steps. This is a high relevance concern of technology scaling (ORSHANSKY, 2008) which will be briefly exposed in Section 2.1.1.

The sensitivity increase means that the circuit is easier affected by undesired voltage fluctuations as its dimensions reduce. These fluctuations may induce logical mistakes, expressed as errors in the processed or stored data or physical damage, like an oxide breakdown or a metal melting. They are generated from many possible sources, both from the circuit itself, like coupling noise, as from the environment, like electrostatic discharges or charged particles. Electrostatic discharge (ESD) is detailed in Section 2.1.2, Single Event Effects (SEE) in Section 2.1.3 and noise in Section 2.1.4.

Some electrical characteristics, as resistances and capacitances, present undesired behaviors when devices reach nanometric dimensions. Main concerns in this topic are: the increase in the materials resistivity due to the interfacial and grain boundary scattering (MCPHERSON, 2006) and the raising of previously negligible parasites, like fringe capacitances and some resistances categories (KUHN, 2009). In a more specific point of view, the increasing of interconnections resistance catalyses studied effects like IR- drop, described in Section 2.1.5, and the loading effect, which is briefly explained in Section 2.1.6.

2.1.1 Manufacturing variability

The concept of variability relies on the unpredictability of how close will be the real circuit behavior of the planned one. This is a pretty much generic concept which covers even environmental variations beyond expected limits. This work will focus on the “physical variability” category, which is defined by Orshansky (2008) as the one caused by the circuit manufacturing, and so will used as synonymous of manufacturing variability. Figure 2.1 draws the example of one possible manufacturing variability reflex. It shows a large difference on electrical characteristics of manufactured microprocessors, even though they have the same layout.

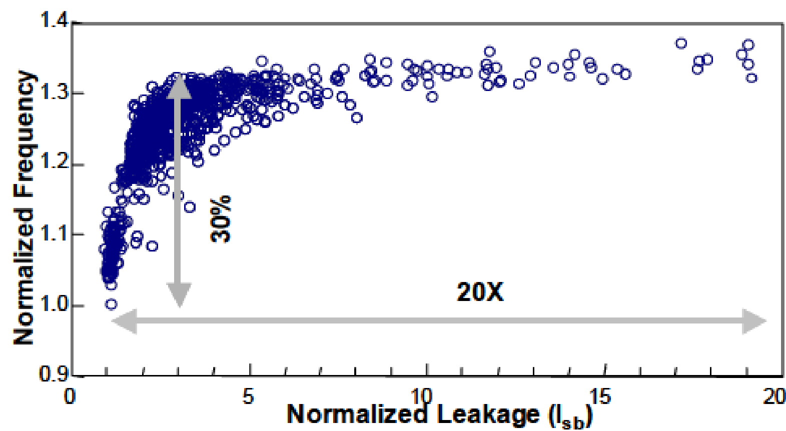


Figure 2.1: Distributions of frequency and standby leakage current of microprocessors in a wafer. (BOKAR, 2003)

Orshansky (2008) also separates physical variability in two components: front-end variability, which results from the earlier steps of fabrication process (devices creation), and back-end variability, which results from the later steps of fabrication (interconnections creation).

Some components of the manufacturing variability have correlation with design patterns and are enough well understood to be mathematically modeled. These models are utilized as prediction tools in project time. A variability component is considered random when the modeling is too complex that becomes prohibitive or when there is no sufficient knowledge about a phenomenon to create the corresponding model. The only assumption made when dealing with random variability is the range of variation on the parameters of interest. The usual reliability strategy against random-variability is to compensate the worst corner with overdesign (ORSHANSKY, 2008).

The amount of physical variability present on a circuit depends on a series of variables; between them are the circuit area, the complexity of the fabrication process and the applied layout techniques (CHIANG, 2007). The scaling of CMOS technologies increases the magnitude of this variability category. One contributing factor is the rise of multiple systematic sources of parameter variability caused by the interaction between the manufacturing process and the design patterns. For example, optical proximity effects cause polysilicon feature sizes to vary depending on the local layout surroundings, as exposed in Figure 2.2. Another factor is that, while technology scaling reduces the nominal values of key process parameters, such as effective channel length,

the ability to correspondingly improve manufacturing tolerances, as well as developing layout compensation techniques, is limited (ORSHANSKY, 2008).

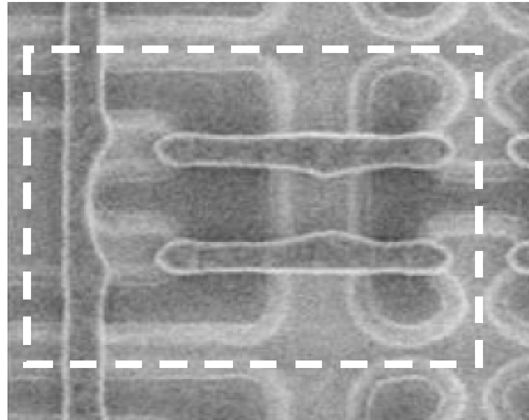


Figure 2.2: Example of neighbors-dependent width variation. (KUHN, 2007)

If beyond the previewed margins, the manufacturing variability may result in non-functional circuits, which must be detected and discarded. The production yield decreases as the amount of discarded ICs increases, and the yield is one of main concerns to the continuous progress of the technology as we know (JAHVERI, 2010).

2.1.2 Electrostatic Discharge

The electrostatic discharge (ESD) actually must be understood not only as the discharge itself, but as the sequence of two events: the charging (slowly or quickly) of a node which does not have a path to ground, followed by its quickly discharging.

The occurrence probability of ESDs is commonly not negligible, since the charging process may have many sources: the mechanical contact and separation of two surfaces with different electron affinity (triboelectric charging), the misuse of air ionizers (ionic charging), the direct transferring from a charged object into an IC (direct charging), the immersion into an external electrostatic field or the electrostatic field increasing (field-induced charging) (AMERASEKERA, 2002). Figure 3.2 illustrates two situations in which ESD could occur usually used in the effect modeling.

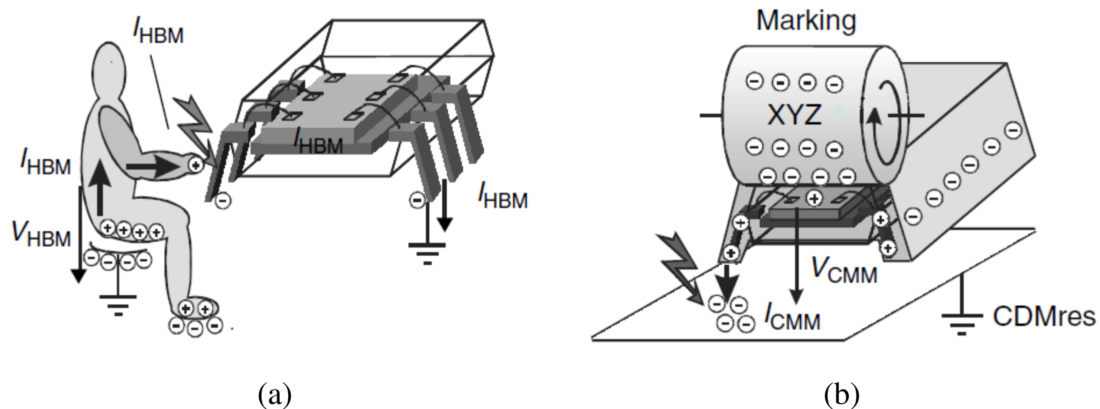


Figure 2.3: Examples of charge distributions causing ESD: (a) human body model and (b) machine model. (AMERASEKERA, 2002)

The avoidance of ESD in ICs is highly desirable, since the discharge current may produce overvoltage, causing damages like oxide breakdown or even metal melting (WESTE, 2004).

However, the ESD avoidance may be not trivial as this effect may occur in many different periods. The main ESD problem in a wafer fabrication area is static charge generation. Prevention methods include the use of antistatic coatings to the materials or the use of air ionizers to neutralize charges. Damage caused by human handling can be reduced by proper use of wrist straps for grounding the accumulated charges and shielded bags for carrying the individual wafers. As a second step to reduce ESD effects, protection circuits are implemented within the IC chip. The packaging procedure itself can cause serious damage; antistatic precautions are also needed during the wire bonding and assembly phases. Even with good protection circuits, other forms of ESD from the charged boards are possible. Thus ESD precautions are important during system assembly as well (AMERASEKERA, 2002).

A relatively weak protection is better than nothing, and so ESD-aware designs containing protection circuits attached to the I/O pads has been a usual option. A good ESD protection circuit must quickly sink the ESD event without becoming damaged while limiting the voltage across parallel sensitive devices, and it must also meet the functional specifications of the I/O. It means to have a fair performance in four categories: robustness, effectiveness, speed, and transparency (AMERASEKERA, 2002).

Some of the concerns for protection devices in deep submicron processes include the thin gate oxides and small channel lengths. From the design viewpoint, circuits fabricated in these technologies have very high densities with large pad counts. The resultant pad-to-pad spacing is small, and so is the total area available for the ESD protection circuit is reduced (AMERASEKERA, 1995).

2.1.3 Single Event Effects

Single Event Effects (SEE) are basically deltas of tension induced by charged particles (radiation) hitting the circuit. The two main sources of radiation that may affect the circuits are alpha particles, originated in the chip itself by the decay of impurities, and neutrons in cosmic rays, which may collide with a silicon nucleus causing ionization (KARNIK, 2004), as depicted in Figure 2.4

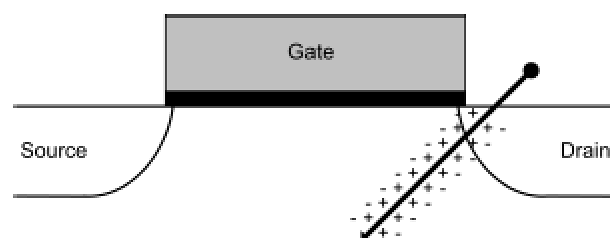


Figure 2.4: Particle incidence on a MOS transistor. (BUTZEN, 2009)

Single Event Effects comprehend Single Event Transients (SETs) and Single Event Upsets (SEUs). The charge deposition caused by the impact of a particle on silicon may switch the logical state of nodes. However, after the deposited charge dissipates, the effects of these events usually disappear. For this reason, they are called Single Event Transients (SETs) and the faults caused by SETs are called transient faults. If the particles energy is high enough to generate charge above the critical charge of the node,

the SET is able to switch the logical state of the node, and the erroneous value can be propagated trough the logic to the output of the network and eventually reach a memory element. If this happens during the latching window of the memory element, this incorrect information can be stored, resulting in a Single Event Upset (SEU). Other possibility of SEU is the particle hitting directly the memory element. SEUs are considered soft errors, because the upset memory element remains operational and able to eventually store new information (HEIJMEN, 2002).

The incidence of particles in the IC may be avoided a special encapsulation, which is usually expansive. Moreover, the SEE can be masked, either logically, electrically or by the lack of a latching window, in which case it generates no error at all if occurs in a combinational section of the circuit. However, in order to cope with errors that may occur when the event is not masked a proper detection and mitigation technique must be applied to ensure tolerant operation (LISBÔA, 2009).

The detection and mitigation techniques may be hardware-based or software-based. Software techniques exploit detection mechanisms developed purely in software, with only extra memory as the allowed overhead (data redundancy); one example is the use of hamming code. Hardware based techniques exploit the introduction of hardware modifications or extra hardware addition; possibilities in this category include re-execution of code (temporal redundancy) and modular replication or insertion of checkers (area redundancy) (LISBÔA, 2009).

With the technology scaling, soft errors become an even higher concern for reasons like:

- Besides higher densities, the availability of faster devices is another feature of future technologies, and it has been predicted that, for those technologies, even particles with modest linear energy transfer (LET) values will produce transients lasting longer than the predicted cycle time of circuits (FERLET-CAVROIS, 2006).
- Manufacturing process variations, higher complexity for manufacturing test due to increased components density in the circuits, and other related problems increases the sensitivity of the circuit (AGARWAL, 2005).
- Smaller devices and higher densities reduce the distance between neighbor nodes in a circuit and increase the possibility of more than one transient fault occurring at the same time. Those multiple simultaneous faults are still due to a single particle hitting the silicon, in which case secondary particles can be emitted in several directions, as illustrated in Figure 2.5 (ROSSI, 2005).

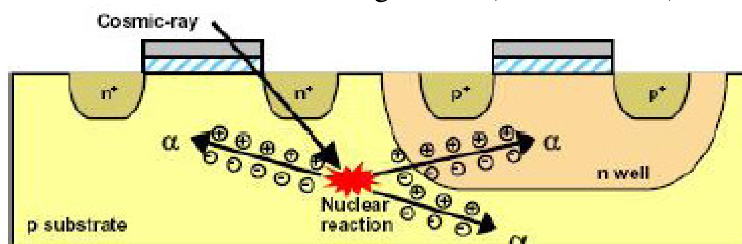


Figure 2.5: One particle, multiple effects. (ROSSI, 2005)

2.1.4 Noise

Noise can be defined as anything that causes the voltage of a node to deviate from the nominal supply or ground rails when it should otherwise have a stable high or low

value (i.e., the node is not switching) as determined by the logic and delay of the circuit (SHEPARD, 1996).

This is a broad definition which induces the creation of subcategories. One division is according to the temporal dimension of the noise in comparison to the digital circuit clock. If the changes in the steady-state logic occur on a time scale which is very slow with respect to the system clock it is called a DC noise. If the voltage peak width is near to the clock period it is said to be a pulse noise (SHEPARD, 1996). Figure 2.6 illustrates these concepts.

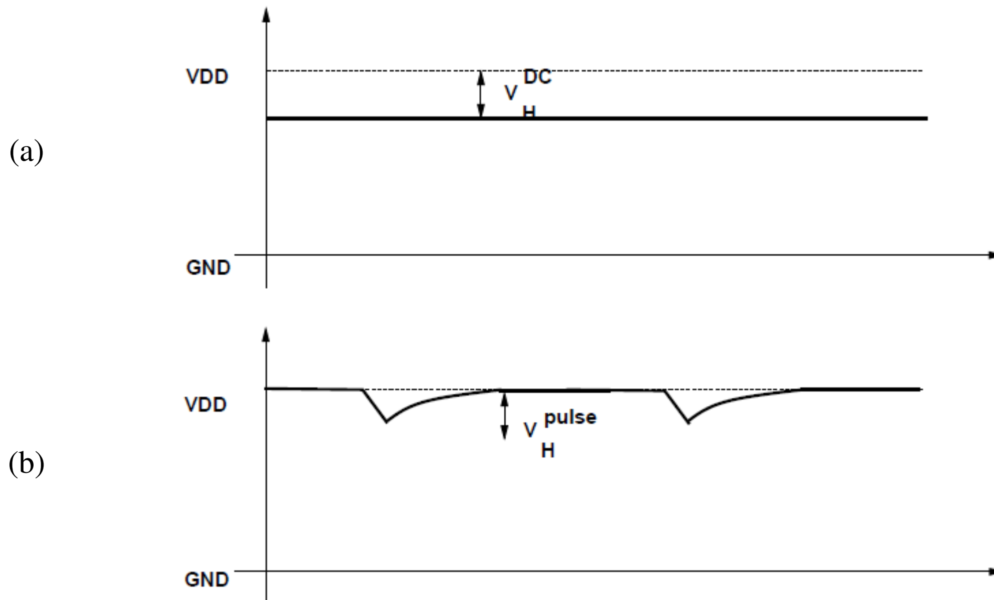


Figure 2.6: Time domain abstractions for noise: (a) DC noise and (b) pulse noise. (SHEPARD, 1996)

The generality of the noise definition also allows including many events as noise sources. Extern sources like electrostatic charge, single event effects, non-nominal supply sources and intern sources like coupling, leakage currents or charge sharing are possible candidates. It is noteworthy that many of these mentioned noise sources becomes more aggressive with technology scaling.

New technologies are more challenging for robust design against noise also due to other factors like: smaller sizes are more sensitive to harsh environment, increased frequencies implies faster switching current increasing emitted noise, and decreased supply voltages reduces noise margins making ICs more sensitive (BEN DHIA, 2006).

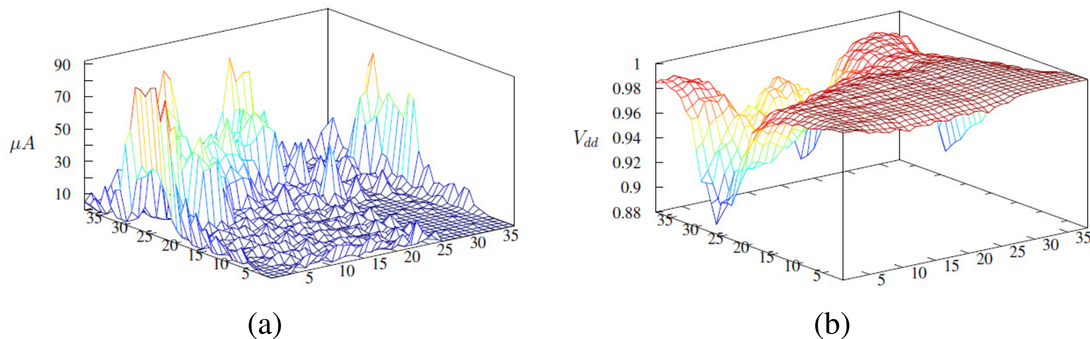
Crosstalk noise fits in the pulse noise category and due its highlighted importance (DARTU, 1997) it is not uncommon to hear the term 'noise' itself is used with crosstalk connotation. Crosstalk noise is relevant when coupling capacitances between the IC interconnections are high. It acts through the induction of a voltage shift in one coupled node when the other presents a sharp change.

The main harm of noises in ICs is the degradation in temporal and energetic performance, which increases the computation fail probability (DARTU, 1997).

2.1.5 IR Drop

IR-drop refers to the amount of decrease (increase) in the power (ground) rail voltage due to the resistance of the it's conducting lines, connecting the external power (ground) source and the node of interest in the circuit (SAXENA, 2003).

Figure 2.7 shows the current and voltage distributions in supply rails of a benchmark (KUMAR, 2009). It can be seen from Figure 2.7 (a), that there are regions which draw larger current than other parts, resulting in large current peaks in parts of the circuit. Consequently, those parts have a larger IR drop leading to lower V_{dd} in the region, as shown in Figure 2.7 (b).



(a) (b)

Figure 2.7: IR-drop example: (a) current distribution and (b) voltage distribution in supply rails of a benchmark. (KUMAR, 2009)

As the current flowing through supply lines, the IR-Drop has a static and a dynamic component. The static component is generated by the subthreshold and leakage currents, and the dynamic by the switching currents (WESTE, 2004). To the dynamic point of view, the IR-drop is slightly similar to crosstalk noise, in the sense that a failure symptom due to increased switching activity could point either to IR-drop or crosstalk problem (SAXENA, 2003).

One concern due to IR-drop is computational failure. The exact physics behind each failure may vary. In some cases, it is due to an excessive delay between the last shift event and the next capture cycle. It also might be that in the center portion of a wire-bonded design, the cumulative effects of even static IR-drop are high enough that "excessive" demands on power supply cannot be met (SAXENA, 2003).

IR-drop mitigation techniques aim to reduce the variation of the supplied energy along all portions of the circuit. It can be reached through a wider and better distributed supply rails, or through IR-drop aware placement and routing algorithms, as proposed by Kumar (2009).

In nanometric technologies, IR-drop tends to worse, since narrower conducting lines present more resistance, and the power consumption is proportionally larger (due to subthreshold and leakage currents increase, and also to the larger integration which increase dynamic currents).

2.1.6 Leakage Currents

The leakage currents in digital ICs becomes more expressive as the devices dimensions shrinks. In nanometer technologies this problem becomes more complex. In these technologies, the total standby power consumption of a circuit cannot be estimated just by summing individual leakages from logic cells, since leakage currents of distinct cells interact with each other through internal circuit nodes (inter-cell connectivity).

Such interaction is known as ‘loading effect’ (BUTZEN, 2010a) (MUKHOPADHYAY, 2006).

Figure 2.8 illustrates the leakage currents of two cascaded CMOS inverters. Considering input logic value equal to ‘0’ (0 V), all leakage currents (subthreshold, gate oxide, BTBT) on the first inverter (driver), and the gate leakage currents of second inverter (receiver) contribute to decrease the voltage V_n at intermediate node (ideally in V_{dd} - power supply voltage). Such potential reduction tends to reduce those leakage components directly associated to this node. However, the voltage reduction in V_n changes the gate-source potential (V_{gs}) at the PMOS transistor on the receiver, increasing significantly its subthreshold current (exponentially dependent on V_{gs}). A similar analysis can be easily done considering the input logic value of the inverter chain equal to ‘1’ (V_{dd}). In summary, the loading effect reduces all currents directly linked to the evaluation node while increases significantly the subthreshold leakage on the next stage (BUTZEN, 2010a).

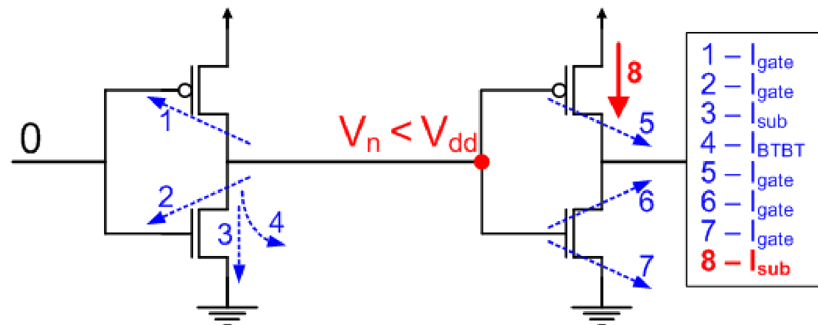


Figure 2.8: Leakage currents associated to the intermediate node potential V_n in two cascaded CMOS inverters. (BUTZEN, 2010a)

Mukhopadhyay (2006) and Rastogi (2007) analyze the impact of loading effect in total leakage estimation. Those works claims the loading effect modifies the leakage of logic gates by approximately 5% to 8%. However, in a recent developed work we have shown that their estimation is optimistic due to the ignoring of the inter-cell connection resistance (BUTZEN, 2010a). As shown in Figure 2.9, the routing resistance becomes more influent in the leakage of the circuit as circuits become larger. It makes sense, since in larger circuits the average resistance of nets is usually higher. The magnitude of the loading effect influence in the leakage currents of these benchmarks is negligible. However, if the loading effect is taken into consideration, the interconnect resistances must be present into its calculation, because the difference in its results can reach up to 100% (BUTZEN, 2010a).

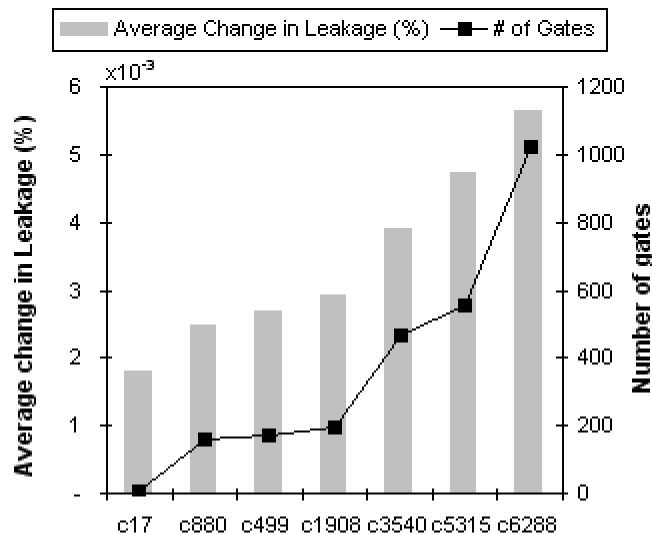


Figure 2.9: Benchmarks leakage and number of gates (BUTZEN, 2010a). The ‘change’ in average leakage is compared to the analysis where routing resistances where not considered.

Thus, in large circuits, designed in future CMOS technologies (with higher leakage and resistance values), not only the loading effect, but also the wire resistance influence in the final leakage circuit, are expected to be more expressive, becoming also a technology scaling concern.

2.2 Lifetime Reliability Issues

Lifetime reliability is to warrant that a functional integrated circuit will still satisfactorily working along a predefined time interval, usually years. Lifetime reliability issues encompass the aging effects: effects which gradually degrade the IC performance possibly causing failures.

Some of the main aging effects will be briefly reviewed in the next subsections.

2.2.1 Time Dependent Dielectric Breakdown

The time-dependent dielectric breakdown (TDDB) is the gradual loss of the insulating property in the transistor gate oxide. This effect, also named ‘progressive breakdown’ (MONSIEUR, 2002), is a gradual hard breakdown, and is distinct from soft breakdown which is a stable, low current that is typically not observed in small devices (STATHIS, 2003).

TDDB is based on insulator defects. Since its fabrication process, the insulating layer presents a small amount of defects, which does not compromise its properties. In the moment that an electric field is applied over the oxide, new defects are gradually generated. This electric field drags ions which recombine with the insulating material, creating a defect in its crystalline structure.

The defects may reach enough number to create a conducting path through the insulating layer - a dielectric breakdown - which will be quickly widen compromising the correctness of the device operation. Figure 3.2 presents a transversal view of the transistor, illustrating defects and a conducting path in the gate oxide.

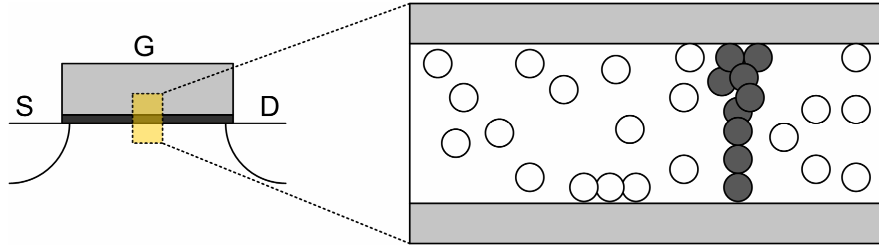


Figure 2.10: Transversal view of a transistor with defects and a conducting path in its gate oxide. (BUTZEN, 2009)

The quickness in the elimination of the insulating property of the gate oxide is directly proportional to the oxide thickness and to the electric field magnitude. Thinner oxides need less aligned defects to get through its dimensions. Higher electrical fields accelerate the defects generation process. Figure 2.11 depicts the dependence of the breakdown process (increase in the leakage current) on the applied gate voltage.

With technology scaling, the oxide thickness is constantly shrinking, provoking an increase in the electric fields trough it, both catalyzing factors to TDDB degradation, arising the importance of this effect in nowadays technologies.

Supply voltage downscale and use of thicker oxides are the trivial solutions for TDDB (STHATHIS, 2003). Another possibility is the stress probability management: as the input vectors may determine the presence or absence of the aggressive electrical field, they can be explored to minimize degradation.

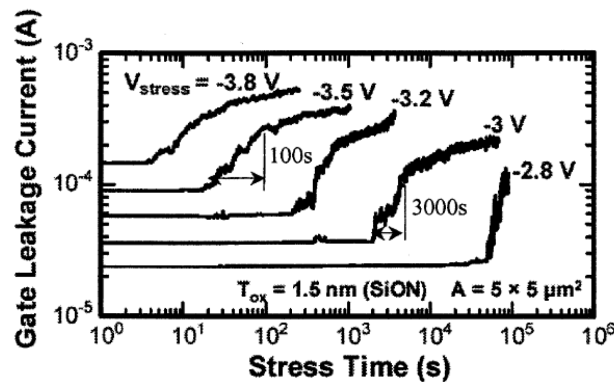


Figure 2.11: Example of progressive breakdown, showing the slow, voltage-dependent growth of leakage current after oxide breakdown. (STATHIS, 2003)

2.2.2 Hot Carriers Injection

The effect called hot carriers injection is related to the transistors state switching. When the transistor changes its steady state, from a non-conducting to a conducting one, highly energized charges flow through the formed channel. However, a certain percentage of electrons moving along the channel from the source to the drain may attain high kinetic energies which enable these hot electrons to overcome the interface potential barrier and enter the gate oxide. In order for channel hot electrons to reach the gate oxide, these electrons must gain sufficient kinetic energy from the channel electric field and have their momentums redirected towards the Si-SiO_2 interface (LEBLEBIC, 1993). Figure 2.12 illustrates this phenomenon.

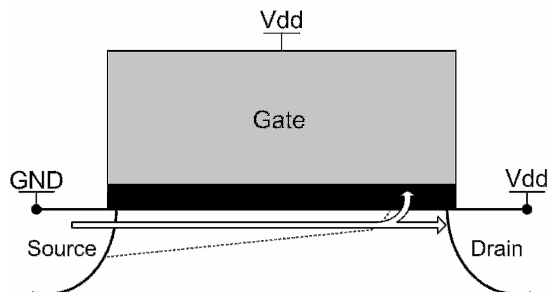


Figure 2.12: Hot carriers effect illustration: charges are injected in the transistors gate oxide. (BUTZEN, 2009)

Due to its acting mechanism, the hot carriers injection profile presents a high concentration of trapped charges in the oxide portion nearest to the drain, does not compromising the entire insulator.

The hot-carrier induced damage in transistors has been found to result in either trapping of carriers on defect sites in the oxide or the creation of interface states at the silicon-oxide interface, or both. The damage caused by hot-carrier injection affects the transistor by changing its transconductance, shifting threshold voltage and affecting the drain current capability. However, hot carriers affect distinctly different transistor types: while in NMOS the current capacity is reduced, in PMOS it is increased. Nevertheless, HCI, leads to the degradation of circuits performance over time (LEBLEBIC, 1993).

Advances in VLSI fabrication technologies are primarily based on the reduction of device dimensions, such as the channel length, the junction depth and the gate oxide thickness, without proportional scaling of the power supply voltage. This decrease in critical device dimensions to sub-micron ranges, accompanied by increasing substrate doping densities, results in a significant increase of the horizontal and vertical electric field in the channel region, increasing the HCI phenomenon occurrence and so the circuit degradation.

Due to their concepts affinity (both involve charge traps in transistors oxides) and high relevance, in recent works (HUARD, 2007)(WANG W., 2007b), NBTI and HCI have been attached to each other in modeling sections. Using this approach it is possible to achieve a more accurate lifetime reliability prediction.

2.2.3 Electromigration

Differently from the majority of mentioned effects, this phenomenon main victims in digital ICs are not transistors, but metal interconnections. The term “electromigration” is applied to mass transport in solid state metals when the metals are stressed at high current densities. This might result in a steady change of conductor dimensions, thereby causing the creation of either voids or the creation of hillocks and whiskers in the affected regions (LIENIG, 2005). Gradual particles migration can lead to the rupture of metal nets, as depicted in Figure 2.13.

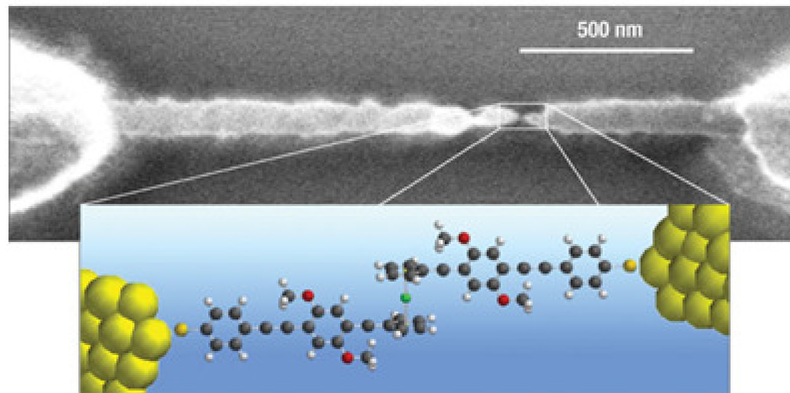


Figure 2.13: Net rupture due to electromigration. (REED, 2004)

The electromigration concern is highlighted with technology scaling. The nanometric technologies increase the devices integration into the same region, and this large integration increases the necessary to operation currents. Besides that, the interconnections width is shrank as fabrication processes evolve. This way, the amount of necessary transported atoms to generate a conductor break is reduced.

A usual technique for electromigration robustness is to design the layout metal wires widths larger than the minimum ones. This technique is traditional in defining the minimum width in supply networks, since these nets current densities are the highest ones (WESTE, 2004). Other solution is to manage current densities defining maximum fanouts to interconnected nodes. A solution which is not available during the, but in the fabrication process construction, is to change utilized material in conducting nets building (REED, 2004).

2.2.4 BTI

As the BTI category has a highlighted importance in this thesis, so it will be explored in more details in next chapters.

3 BTI

The BTIs: negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI) are aging effects which can be understood as a series of atomic restructurings (trap generation) in the oxide-bulk interface of transistors.

3.1 Basics

The atomic restructuring in BTIs is highly influenced by the electric field through the oxide; it means that these effects have a **defined severe stress condition**, which depends on transistors biasing. For the NBTI, the stress condition is when the transistor is negative-biased (V_{gs} ~ -V_{dd}), as depicted in Figure 3.1(a), which is a usual biasing situation in PMOS transistors. Intuitively, the stress condition of PBTI is when the transistor is positive-biased (V_{gs} ~ -V_{dd}), as usual in NMOS transistors (Figure 3.1 b).

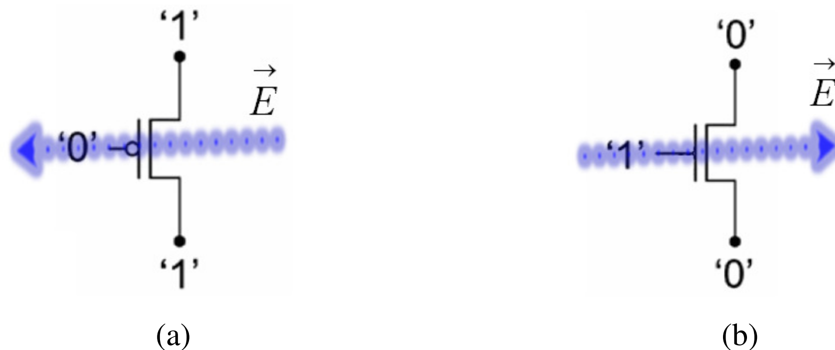


Figure 3.1: Transistors biasing in: (a) NBTI stress and (b) PBTI stress.

Although many physical details still under investigation, it has been widely accepted (ALAM, 2005)(SCHRODER, 2007) that the electrical field across the oxide causes continuous trap generation in Si-SiO_2 interface of transistor. These traps usually originate from Si-H bonds generated after the Hydrogen passivation process to remove dangling Si atoms at the Si-SiO2 interface (PIERRET, 1996). However, under stressed operating condition, these bonds can easily break with time and generate positive interfacial traps (donor-like state), as depicted in Figure 3.2. This understanding is described by Reaction-diffusion (R-D) analytical models (JEPPSON, 1977)(ALAM, 2005)(VATTIKONDA, 2006) (further explored in chapter 4), where 'the reaction' means the Si-H bonds breaking and 'the diffusion' means the movement of newly released hydrogen away from the interface.

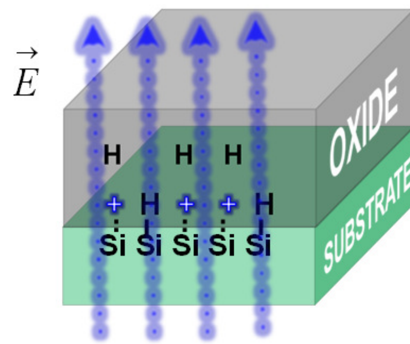


Figure 3.2: Positive interface traps generation due to electric field (NBTI stress electric field example).

In the absence of the stressing electric field, the transistor is in the recovery phase. In this phase, some previous released and diffused hydrogen anneal back to the Si-SiO_2 interface, reestablishing their position in some created dangling bond and neutralizing these traps. However, this 'regeneration' process is commonly not absolute, since hydrogen may also recombine as H_2 and stuck in the oxide body, leaving uncovered traps. This explanation is illustrated in Figure 3.3

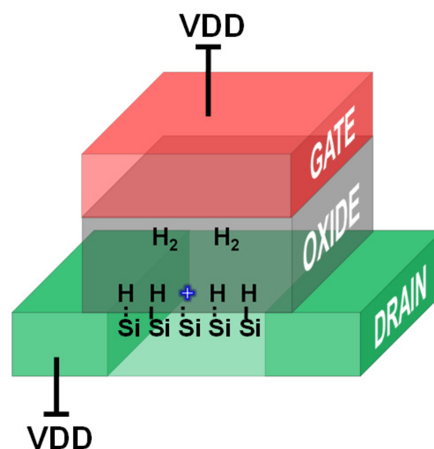


Figure 3.3: Example of NBTI recovery condition, some previous released hydrogen goes back to the interface (neutralizing traps) and some recombine and don't return.

The consequences of generated traps on the devices are observed as degradation on drive current, circuit speed, noise margin, and the matching property. Although, transistors threshold voltage shift has been the dominant attention focus since it encompasses all these mentioned consequences. During the time in which the transistor is under the stress condition the threshold voltage increases, while in the recovery time this V_{th} shift shrinks, but is never nullified, as shows the Figure 3.4.

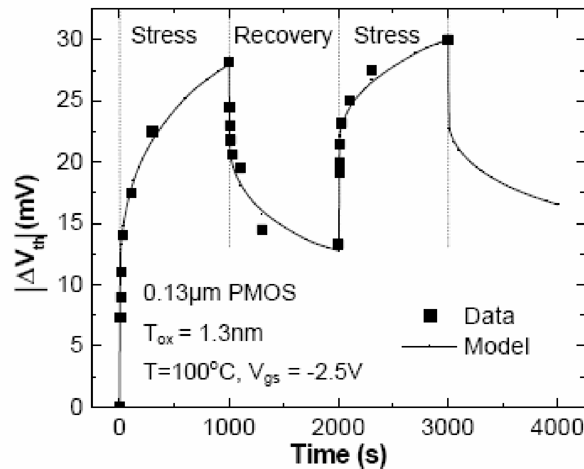


Figure 3.4: ΔV_{th} during dynamic NBTI phases. (VATTIKONDA, 2006)

The temperature is also a fundamental factor in NBTI and PBTI. As higher is the temperature, more aggressive is the degradation. The Figure 3.5 illustrates this behavior. However, some works have shown that really high temperatures (like 300ºC) may help the annealing process of the recovery phase, acting as a healer against degradation (BENARD, 2008).

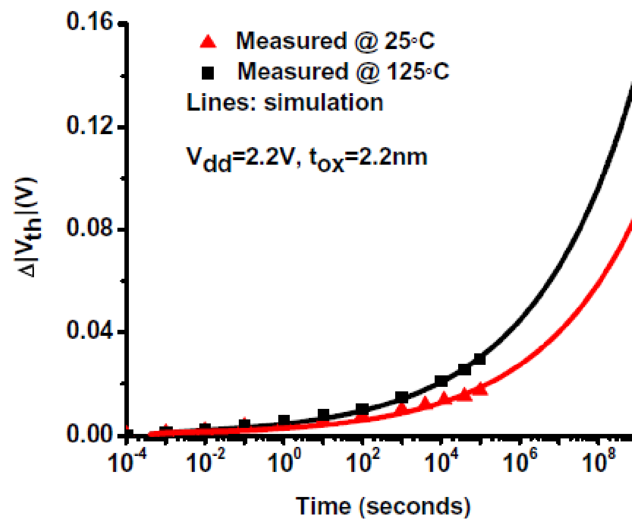


Figure 3.5: Temperature influence in ΔV_{th} shift due to NBTI. (ZHANG, 2008)

Any other variable which has influence in the mentioned components of the BTI aging process (like a different material in the substrate-insulator interface which affects the bonds strength, or a thicker oxide which reduces the electric field) will affect the induced degradation behavior. The designer has access to some of these variables and may intentionally manipulate them to decrease the stress severity over his design.

3.2 Scaling Influence

Physical explanations of NBTI and PBTI process have been known for decades in the device reliability community (YOSHIO, 1966). However, it has recently gained attention, mostly due to the wide usage of ultra-thin oxide devices. Specifically, International Technology Road Map for Semiconductor (ITRS) projects oxide thickness

of less than 10Å in sub-32nm technology nodes (ITRS, 2008). These **thin oxides substantially increases the vertical oxide field** (E_{ox}) to the range of few MV/cm, which in turn can result in more severe BTI degradations and corresponding V_{th} increase of transistors (ALAM, 2003).

Furthermore, NBTI and PBTI are caused during static stress on the oxide even without current flow. Consequently, their degradation is exacerbated in the nanoscale design as advanced digital systems tend to have longer standby time for lower power consumption (VATTIKONDA, 2006).

3.3 NBTI

Therefore, Negative Bias Temperature Instability (NBTI) is only a subset of possible BTI effects, and its influence is severe only in one transistor type: PMOS. Nevertheless the NBTI in PMOS transistors has been the category of major interest as, for nanometric technology nodes, it has become a primary limiting factor of circuit lifetime (PAUL, 2006)(KUMAR, 2007)(WANG W., 2008)(GUARDIANI, 2009)(QI, 2010). The Figure 3.6 depicts this highlighted influence.

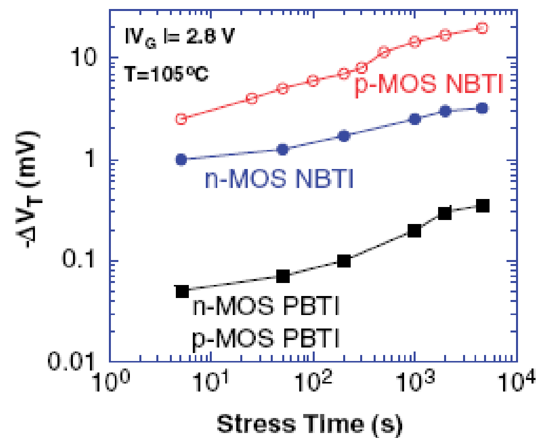


Figure 3.6: Threshold voltage shifts for p- and n-MOSFETs for positive and negative gate bias. (SCHRODER, 2006)

Indeed, as gate oxide gets thinner than 4nm, the threshold voltage change caused by NBTI for the PMOS transistor has become the dominant factor to limit the circuit life time, which is much shorter than that defined by hot-carrier induced degradation (HCI) of the NMOS transistor (VATTIKONDA, 2006).

As the NBTI effect becomes more severe with continuous scaling, it is critical to understand and minimize the impact of this effect in circuits' design, to ensure the reliable operation for a desired period of time. The next two chapters go deeper in this effect details, focusing on its evaluation and mitigation, and revealing developed works and obtained results.

4 NBTI EVALUATION TECHNIQUES

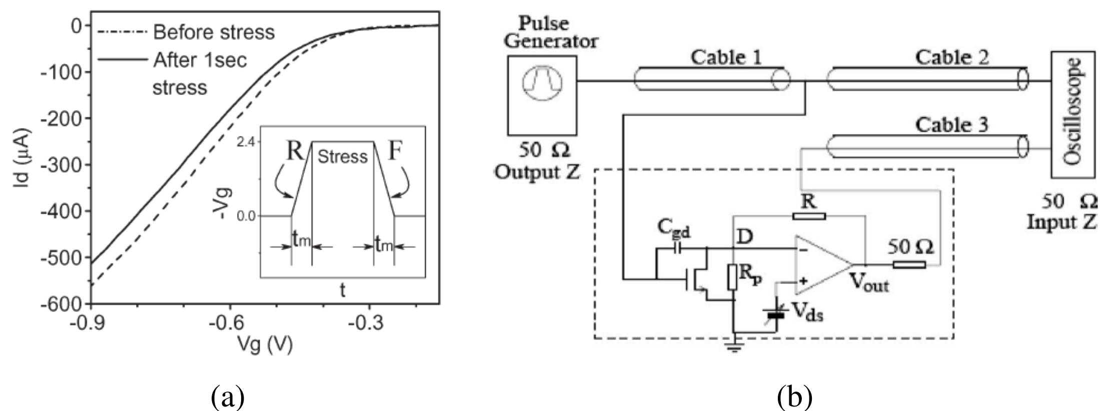
This chapter will discuss evaluation techniques on NBTI, starting from physical measurements, and then getting through devices degradation modeling and expanding these concepts to enable circuit-level analysis.

4.1 Physical Measurements

An elementary step of any evaluation is to be able of obtaining physical measures of the effect, because it makes possible the characterization of the effect's behavior.

Traditionally, NBTI has been characterized by stressing a device, then interrupting the stress to measure a device parameter, stress again, measure again, and so on. The threshold voltage is the main parameter affected by NBTI, and was usually determined from I_d–V_d and I_d–V_g quasi-dc measurements (SCHRODER, 2006). However, since authors like Ershov (2003) shown that the time between the stress period and the measurement of its consequences is quite important, techniques were developed to minimize and eliminate this gap time.

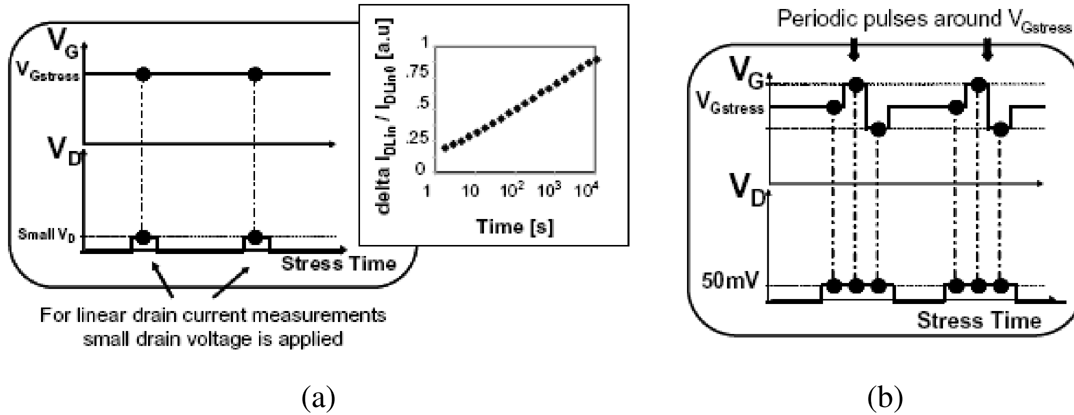
The fast pulse measurement (FPM) method was developed to measure the threshold voltage degradation fast enough to be considered as free of recovery effect (SHEN, 2004). This method has been constantly improved (YANG, 2005) (SHEN, 2006) and the measurement time already reached less 100 ns (LI, 2008). The measurements of I_d and V_g (from which it is possible to deduce V_{th}) are realized during the edges of a pulse applied device's gate, as illustrated in Figure 4.1 (a). The measurement system, whose schematic is shown in Figure 4.1 (b), is built so that Vg is the voltage of the input pulse itself, and I_d is the output of an operational amplifier.



(a) (b)

Figure 4.1: FPM method – (a) measurement range t_m and (b) schematic of measurement system. (SHEN, 2004).

The “on-the-fly” (OTF) method, proposed by Huard (2006), also has as goal to insure that no unwanted recovery occurs during device parameters measurement. The drain voltage degradation is recorded without interrupting the stress period, applying a low drain voltage, while the gate voltage remains in its stress condition (Figure 4.2 (a)). Since the drain current does not depend solely on threshold voltage, small gate voltage pulses are superimposed, allowing the transconductance to be determined, as exposed in Figure 4.2 (b).



(a) (b)

Figure 4.2: Schematic of first level OTF, where linear drain current shifts can be monitored (a), and schematic of second level OTF (b), where the drain current shifts as well as the associated transconductance variations can be monitored. (HUARD, 2006)

OTF method’s main source of error is the stress before the first measurement, which distort the “fresh device” referential. To compensate this weak point, variations of the OTF method has been proposed, like fast OTF (FOTF) and OTF interface trap (OFIT), the details of such proposals can be found in Li (2008). FPM also has a source of error relying into the (possible) small recovery during the measurement. Table 4.1 summarizes measurement techniques sources of errors (SHEN, 2006).

Method	Source of error	Effect on measured ΔV_{th}
Slow on-the-fly	Initial pre-stress I_d measurement (V_g = V_{stress}) is too slow, during which I_d degrades.	Large under-estimation
Fast on-the-fly	Initial pre-stress I_d measurement (100-200 ns) induces small stress and thus small Id degradation.	Small under-estimation
Fast I_d - V_g	Small recovery after stress is removed, during V_g sweep measurement (100-200 ns).	Small under-estimation

Table 4.1: Summary of measurement techniques. (SHEN, 2006)

Measurements methods have still evolving and their improvements, as well as comparisons between them, have been a common topic in recent researches. (JI, 2009) (JI, 2010)

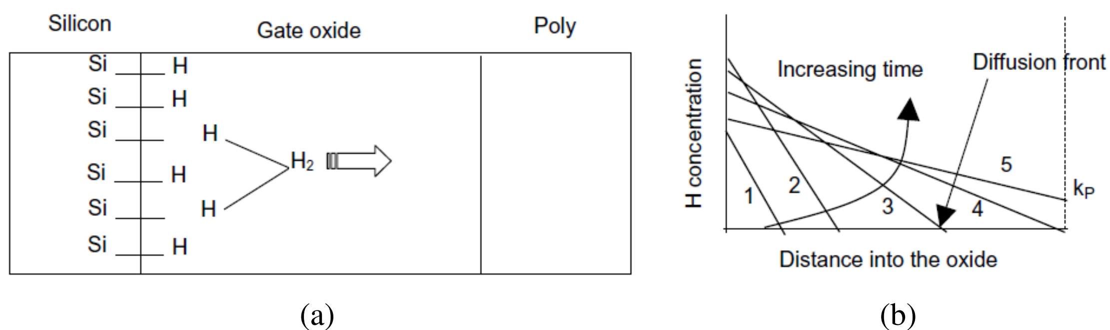
4.2 Devices Degradation Analytical Models

Well executed series of measurements (in convenient range of conditions and enough number of samples) make possible to characterize the degradation's behavior, and then to create predictive mathematical models which follow this behavior.

Alam (2005) has demonstrated this process of observation, understanding and modeling. In his work, experimental signatures of NBTI were enumerated, indicating that the time evolution of V_{th} degradation is described by an imperfect power-law relationship (i.e., $\Delta V_{th} \sim t^n$ with $n \sim ¼$) influenced by many variables such as temperature, bias condition, oxide thickness and the chemical elements around its interfaces. From the analysis of these signatures, he created an enhanced reaction-diffusion (R-D) model, in which the origination of channel-oxide positive interface traps (Nit) is the only responsible for threshold voltage degradation (JEPPSON, 1977).

In reaction-diffusion models, the interface traps which appears when the device is stressed are assumed to be originated by the dissociation (reaction) of Si-H bonds in the oxide-channel interface followed by the propagating (diffusion) of hydrogen cells through the oxide, as depicted in Figure 4.3 (a).When the device is not in a stress condition, a partial recover occurs, since the hydrogen cells that have not recombined into H_2 may get back to the oxide-bulk interface and neutralize some traps.

The Figure 4.3 (b) illustrates the hydrogen profile in the oxide during stress phase. The area under the hydrogen profile equals generated interface traps. The shape and sequence of these profiles reflect the reaction-limited (1, 2) and diffusion-limited (3, 4) regimes. Once the diffusion front reaches the SiO_2/poly-interface (5), faster diffusivity of H_2 in poly ensures that the concentration of H_2 at the poly-oxide interface will change only modestly. This would lead to a sharper gradient in the hydrogen profile resulting in faster H removal from the Si/oxide interface, and would trigger enhanced interface trap generation (ALAM, 2005).



(a) (b)

Figure 4.3: (a) Schematic description of the reaction–diffusion model used to interpret interface-trap generation during NBTI stress. (b) Hydrogen profile in the oxide during NBTI stress. (ALAM, 2005)

The work described by Vattikonda (2006) and Bhardwaj (2006) proposes a more generic model than Alam (2005). Vattikonda's (2006) model is also based in reaction and diffusion, but accepts H as much as H_2 as diffusing element - the choice is made through regulating formulation exponents values - and suppresses the limitation of assuming infinite oxide thickness (as Alam (2005) assumed).

Additionally, this model provides a rising in the abstraction level by presenting a clear formulation of the threshold voltage shifts, which allows the model use without the need of a detailed understanding about interface traps generation. Vattikonda (2006)

formulation includes two equations for V_{th} shifts behavior, one for the stress phase (4.1) and one for recovery phase (4.2).

$$\Delta V_{th}_stress = \sqrt{K_v^2.(t-t_0)^{1/2} + \Delta V_{th0}^{\;2}} + \delta_v \quad (4.1)$$

$$\Delta V_{th}_recovery = (\Delta V_{th0} - \delta_v).\left[1-\sqrt{\eta.(t-t_0)/t}\right] \quad (4.2)$$

In this formulation, the time t is calculated in seconds, starting from a referential t_0 which flags the last transition between phases. K_v is represented in (4.3. In Table 4.2, the default values of Vattikonda's (2006) model coefficients are given for a 45nm technology.

$$K_v = A.t_{ox}.\sqrt{C_{ox}.(V_{gs}-V_{th})}.[1-V_{ds}/(\gamma.(V_{gs}-V_{th}))].\exp(E_{ox}/E_0).\exp(-E_a/kT) \quad (4.3)$$

A = 1.8 mV/nm/C$^{0.5}$	η = 0.35	E_0 = 2.0 Mv/cm
γ = 1.3	δ_v = 5.0 mV	Ea = 0.13 eV

Table 4.2: Model parameter values.

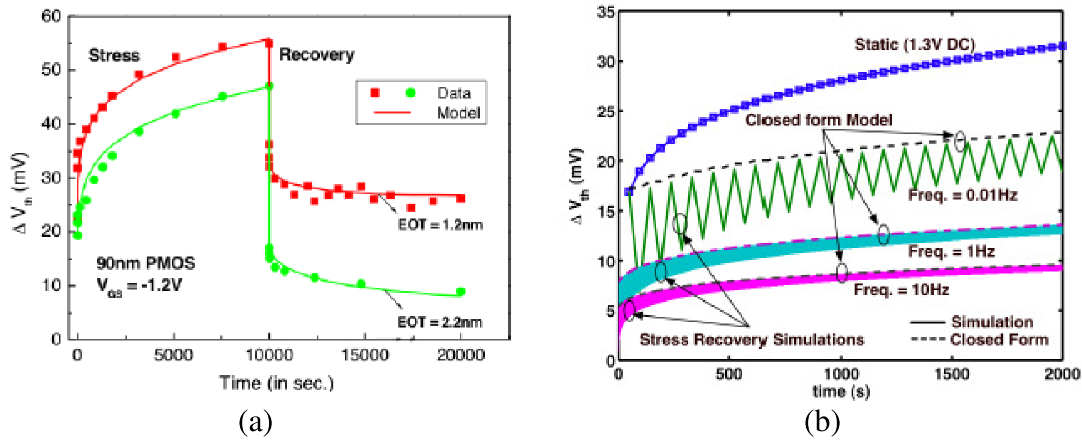
The Bhardwaj (2006) formulation presents, besides the two first mentioned, a long-term V_{th} degradation equation (4.4) which, unlike (4.1) and (4.2), is essentially independent of operation frequency in high-frequencies range. This model represents an upper bound of the previous one, having a much more stable behavior, as depicted in Figure 4.4 (b). In this equation, n is a time exponent, and may present value 1/6 or 1/4 according to the best-fitting diffusion model chosen.

$$\Delta V_{th}_longterm = \left(\frac{\sqrt{K_v^2.\alpha.T_{clk}}}{1-\beta_t^{1/2n}}\right)^{2n} \quad (4.4)$$

In this equation, α is the duty cycle, T_{clk} is the clock period, β are described in (4.5 and the other symbols are constants, being ξ_1 = 0.9 and ξ_2 = 0.5, while t_e either equals t_{ox} or the diffusion distance of hydrogen in the initial stage of recovery.

$$\beta_t = 1 - \frac{2.\xi_1.t_e + \sqrt{\xi_2.C.(1-\alpha).T_{clk}}}{2.t_{ox} + \sqrt{C.t}} \quad (4.5)$$

The Figure 4.4 (a) illustrates the matching between dynamic stress/recovery equations and measured data, while the comparison between the dynamic model and long term degradation model is exposed in the Figure 4.4 (b).



(a) (b)

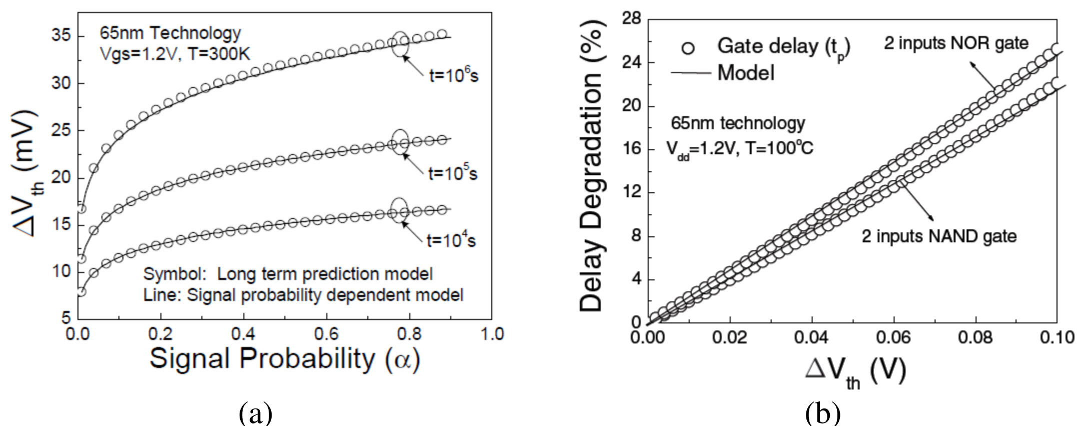
Figure 4.4: Verification of dynamic NBTI model validity (a) and comparison between dynamic model (colored thicker/zigzag lines) and (b) long-term model (dashed lines). (BHARDWAJ, 2006)

Somehow as Bhardwaj (2006), simplifications which discard precision over the necessary and ease computation had became a fashion in modeling. Wang W. (2007a) further simplified the long-term model (4.4) as described in (4.6, where b = 3,9 .10^{-3} V.s$^{-1/6}$. This model is dependent only on signal probability (α) and stress time, and its validation depicted in Figure 4.5 (a).

$$\Delta V_{th} = b.\alpha^{n}.t^{n} \tag{4.6}$$

Simple models, in addition to saving computational time, also facilitate the transformation of threshold voltage degradation equations into a gates' delay degradation prediction. The transformation of the previous model (4.6) into a delay degradation model is described in Wang W. (2008), resulting in the (4.7), in which c is a constant which depends on gate type, as depicted in Figure 4.5 (b).

$$\Delta D_{n_i} = c.\alpha^{n}.t^{n} \tag{4.7}$$



(a) (b)

Figure 4.5: (a) The signal probability dependent model verification (WANG, W. 2007a) (b) Delay model verification (WANG, W. 2008).

This thread of models evolution (Vattikonda (2006) – Bhardwaj (2006) – Wang (2007a)) is just an example of many existing ones, and received more attention in this text since these models are applied in developed works described in forward sections.

Thus, in order to exemplify other well established works about this topic, an interesting evolution in analytical models allows to consider temperature variation over time (LUO, 2007), through the use of an active/standby rate, assuming different temperatures for this two operation modes, as depicted in Figure 4.6. This model is also converted into a delay degradation model based on the widely accepted delay degradation model (PAUL, 2006). Another example is the analytical model built by Kumar (2006) which evolved to a complete NBTI aware circuits synthesis framework described in another his subsequent work (KUMAR, 2007).

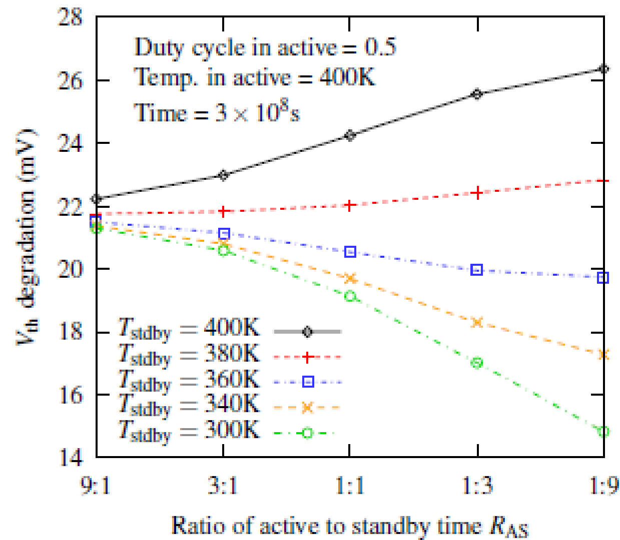


Figure 4.6: Impact of activity/standby ratio on V_{th} degradation. (LUO, 2007)

Recently, Ielmini (2009) has reviewed the weak points of R-D based models, providing his suggestion of solution (a new relaxation-based model). His work represents an expressive recall that the fresh of NBTI devices degradation analytical models hold them immerse in constant evolution and progressive understanding.

4.3 Circuit-Level Analysis

As soon as V_{th} or delay degradation due to NBTI is modeled for a single device or gate, there are different techniques for expanding and applying these models into larger systems, in order to evaluate circuits' performance degradation.

One option is to create an electric circuit schematic which behaviors exactly like a degrading transistor, then to utilize instances of this element to compose a circuit, and perform electrical simulations to observe the degradation effects over time. One implementation of this technique is proposed (SCHUCH, 2009) and is better explained in section 4.4.

Some works (PAUL, 2005)(PAUL, 2006) have shown that knowing the threshold voltage degradation of a single transistor due to NBTI, one can predict the performance degradation of a circuit by providing the degraded values of V_{th} as input to circuit delay models like Sakurai's (1991) one. These works expose benchmarks critical path delay degradation over time, as shown in Figure 4.7, but do not further explore the behavior of multiple paths.

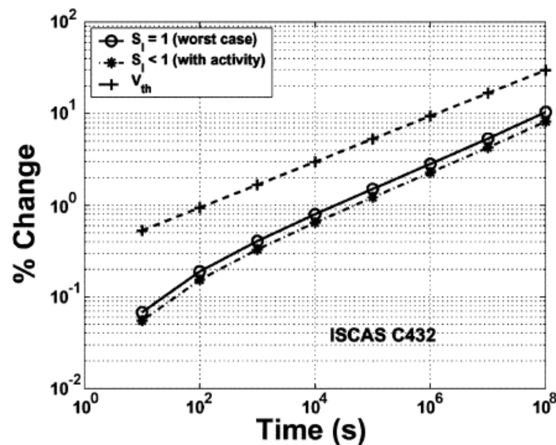


Figure 4.7: Percentage degradation in the performance of ISCAS C432 benchmark circuit (1) with worst case (S = 1) NBTI stress and (2) with activity dependent effect. (PAUL, 2005)

One similar, although more automated, approach is proposed by Wang W. (2008). By using a compact delay degradation model based on signal probabilities, an algorithm named "NBTI aware STA", depicted in Figure 4.8 (a), performs a loop in which the delay degradation of each node is calculated and propagated over its path. After the execution of this algorithm, the delay information of each node and each path of circuit is available, making possible to identify potential critical paths for treatment, as exposed in Figure 4.8 (b).

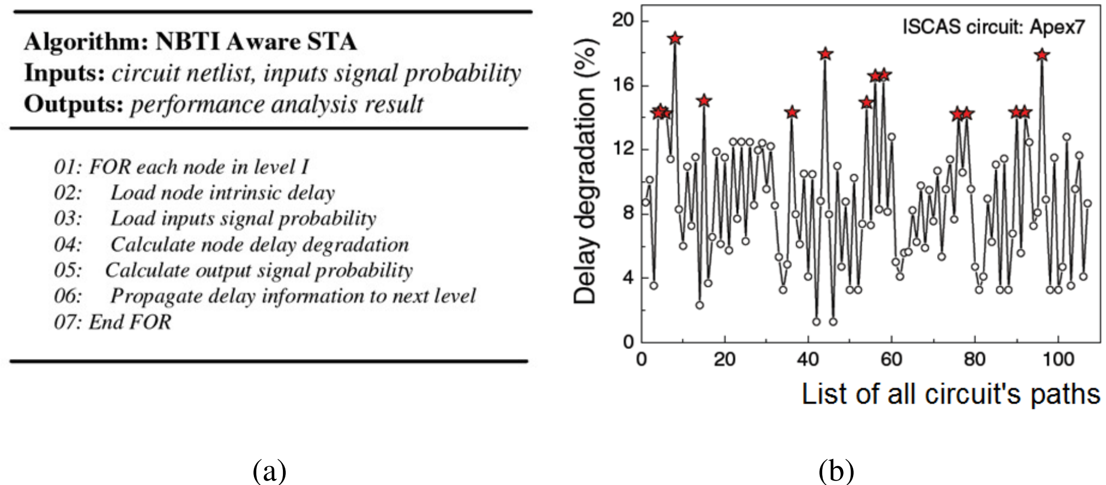
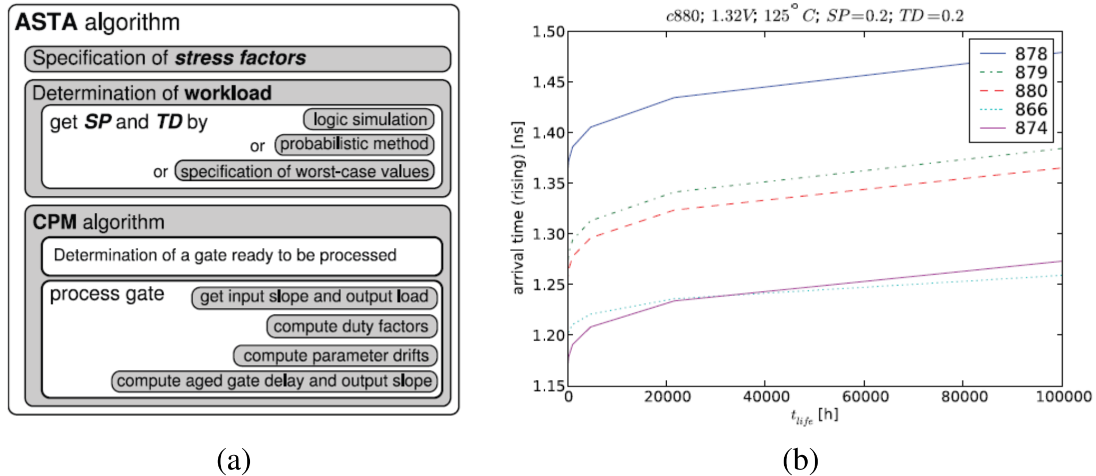


Figure 4.8: (a) NBTI aware static timing analysis algorithm. (b) Searching results of potential critical paths on ISCAS85 Apex7 circuit benchmark. (WANG, W. 2008)

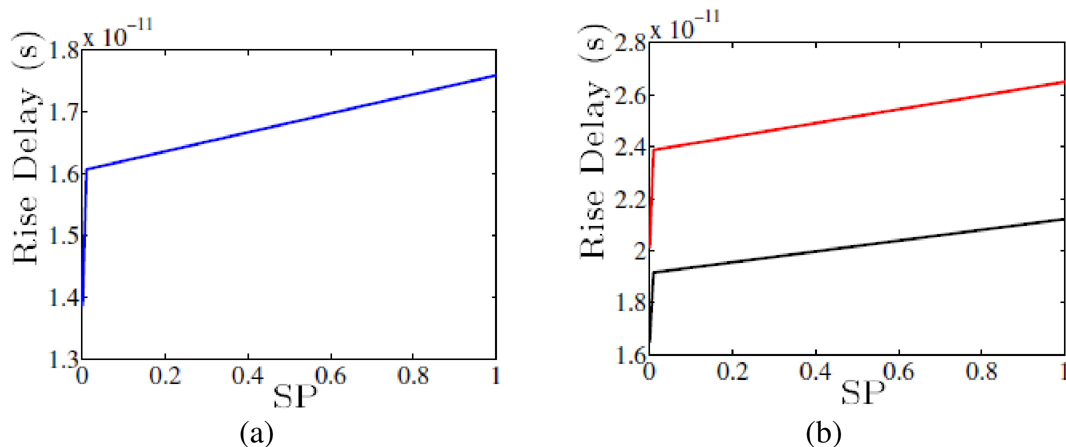
Another implementation of aging-aware STA is proposed by Lorenz (2009). As shown in Figure 4.9 (a), this is a more generic algorithm, which can be applied for both NBTI and HCI degradation, and which supports alternative modules of signal-probability and time-degradation calculation. Figure 4.9 (b) is an illustration of resulting data for multiple paths of a benchmark circuit. One evolution brought by this approach is the use and calculation, respectively, of input and output slopes.



(a) (b)

Figure 4.9: (a) Main steps of the aging analysis flow. (b) The five slowest output arrival times over lifetime for ISCAS circuit c880. The signals 866 and 874 change their order with time. (LORENZ, 2009)

For larger circuits, built through standard-cell flow, a possibility which arises is to characterize an "aged" cell library and then to utilize an ordinary commercial flow (and its STA) to predict the circuit behavior. The challenge in this method is that the degradation of each cell is dependent of its input vectors along time. Kumar (2007) follows this strategy and overcomes the mentioned challenge by defining the delay of each cell as a signal-probability dependent function, as shown in Figure 4.10. Nevertheless, the degradation time is restricted to one value which must be previously specified, usually 10 years (KUMAR, 2007).



(a) (b)

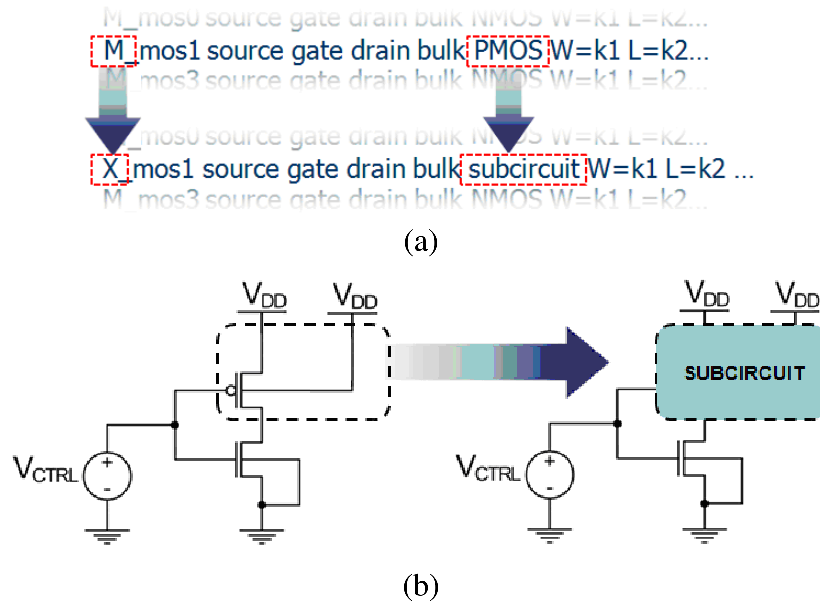
Figure 4.10: Rise delay of (a) an inverter and (b) a two input NAND (b) as functions of input signal-probability (SP), for 10 years of degradation. (KUMAR, 2007)

4.4 Equivalent Circuit for NBTI Evaluation in CMOS Logic Gates

In order to have an estimative about circuit lifetime, electrical simulation may be wanted, however, there is no transistor model that dynamically takes account of NBTI effect during circuit electrical simulation. The objective of this developed work is to suppress this lack, allowing the evaluation of the NBTI effect in circuit design by using electric simulator (spice) for degradation prediction. This work was presented in SBMicro symposium of 2009 (SCHUCH, 2009), and its spice implementation is in the Appendix.

4.4.1 Methodology

To reach its objective, the main idea in the implementation of this work is to replace conventional PMOS transistors utilized in electrical simulations by an equivalent circuit, which behaves exactly like the replaced transistors at the begin, but suffers with aging (modifying its electrical characteristics) according to its operation time and conditions. This idea is expressed in Figure 4.11.



(a)

(b)

Figure 4.11: (a) In spice, a careful subcircuit construction may allow the replacement of a transistor with little syntax changes. (b) The desired result is to replace the PMOS transistors by subcircuits which behave like aging transistors.

It is well-known that the threshold voltage of a transistor is a parameter dependent of its bulk-source voltage, as expressed in (4.8) (WESTE, 2004):

$$V_{th} = V_{th0} + \gamma\left(\sqrt{\Phi_s + V_{SB}} - \sqrt{\Phi_s}\right) \quad (4.8)$$

The proposed subcircuit (SCHUCH, 2009) explores this dependence: a threshold voltage shift is induced (simulating NBTI aging) through dynamically adjusting the PMOS transistors bulk voltage. As depicted in Figure 4.12, the bulk voltage is changed by a controlled voltage source, whose control circuit takes into account the individual stress historic of the device, making use of an analytical model to generate “on-the-fly” the convenient adjust voltage.

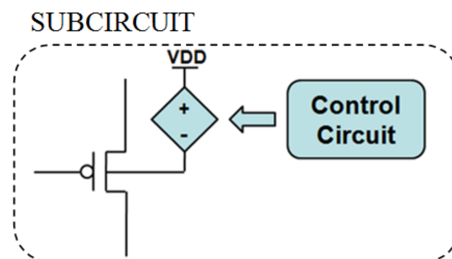


Figure 4.12: The proposed subcircuit is composed by a PMOS in which the bulk voltage changes according to its degradation, controlled by a control circuit expressing an analytical model.

Vattikonda's (2006) analytical model, presented in section 4.2, was the chosen one for this implementation, and the proposed control circuit which is able to express this model's behavior is depicted in Figure 4.13.

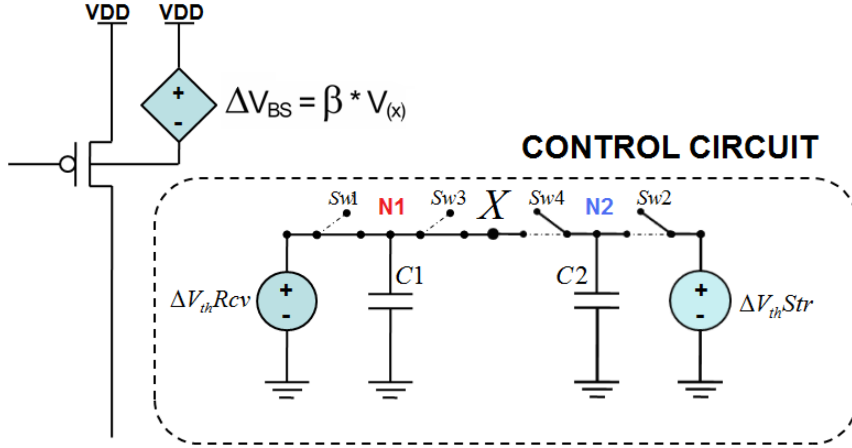


Figure 4.13: The proposed topology for the control circuit, in order to replicate the Vattikonda's (2006) analytical model behavior.

As the chosen analytical model expresses NBTI degradation separated into two equations, corresponding to stress (4.1) and recovery (4.2) phases, there are two variable voltage sources in the control circuit, and each one voltage is calculated by one of these equations.

Nevertheless, both equations are dependent on an initial threshold voltage value, which must be refreshed as transistor operates (and degrades); it means that the stress degradation calculus depends on the last threshold voltage of the recovery phase, and that the recovery calculus depends on the last threshold voltage of the stress phase. The represented capacitors and ideal switches were inserted in the control circuit to deal with this peculiarity. This way, the voltage equations attributed to the variable voltage sources depend on N1 and N2 nodes as described in (4.9) and (4.10).

$$\Delta V_{th}_Str = \sqrt{K_v^2.(t-t_0)^{1/2} + V(N1)} + \delta_v \tag{4.9}$$

$$\Delta V_{th}_Rcv = (V(N2) - \delta_v).\left[1 - \sqrt{\eta.(t-t_0)/t}\right] \tag{4.10}$$

The switches are controlled by transistor's V_{gs}. When the transistor is in the stress phase (V_{gs} ~ $-V_{dd}$) the switches Sw2 and Sw4 are the only ones conducting, thus the voltages in the node X and in the node N2 just follow the voltage variation given by the stress voltage source; when the transistor condition moves to the recovery phase (V_{gs} ~ 0), the switches Sw1 and Sw3 are the only ones conducting, so the capacitor C2 now acts like a memorizing element, keeping in the node N2 a stable voltage value which can used as initial value in the recovery calculation (expressed in the recovery voltage source and followed by nodes N1 and X).

The Figure 4.14 exemplifies the control circuit operation by its nodes voltage values.

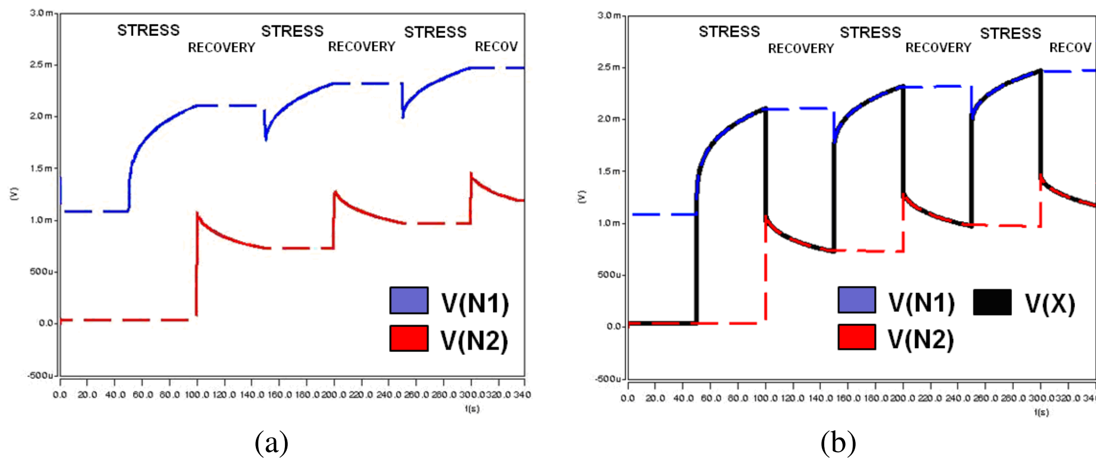


Figure 4.14: Voltage over time graphs. (a) The voltage in N1 and N2 nodes according to the transistor operation, regarding that one node voltage still stable while the other is being calculated. (b) The voltage in node X is the result of a convenient selection between V(N1) and V(N2), showing equivalence to the chosen analytical model behavior.

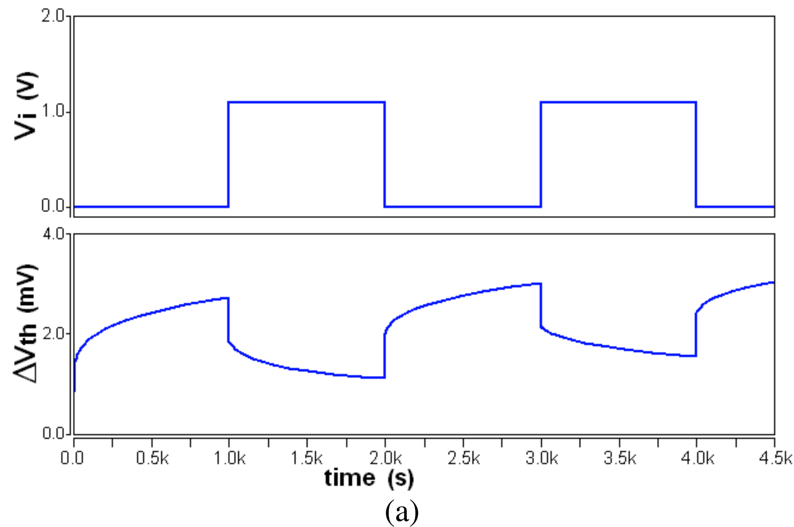
The values of Vattikonda's model coefficients are given for the utilized technology 45 nm PTM process (PTM, 2009) are the same previously presented in Table 4.2.

4.4.2 Simulation Results and Analysis

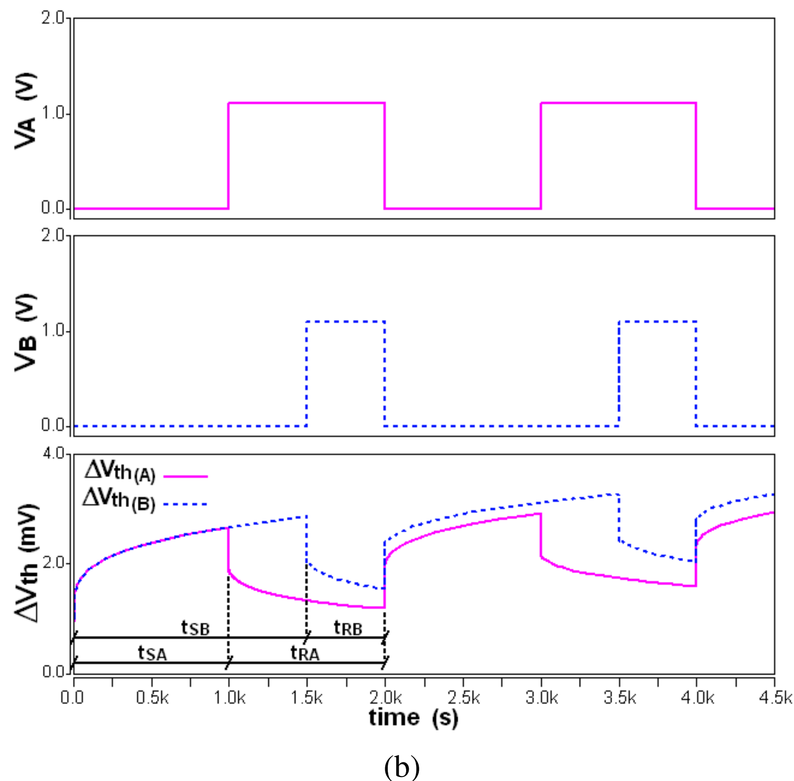
In order to validate the proposed circuit, HSPICE electrical simulations were carried out in two different CMOS logic gates, an Inverter and a 2-input Nand, being calculated the threshold voltage degradation for each of them. Moreover, the rise transition delay degradation (in comparison with the operation time) was also obtained. For simulations, 45 nm PTM process parameters (PTM, 2009), operating temperature of 100ºC, and supply voltage of 1.1V were taken into account.

For Inverter gate, it was applied an input signal with a duty cycle of 50% (stress time = recovery time), during a period long enough to evaluate the degradation of PMOS V_{th} in long term regime. In the case of Nand simulation, it was applied two different input signals (different duty cycles - 50% and 25%), one on each input, in order to prove that, using this method, it is possible to obtain the degradation of each transistor individually.

In Figure 4.15, it is shown the degradation of both logic cells, by presenting ΔV_{th} behavior. Notice that, on the Nand gate the transistor that was stimulated with 25% duty cycle signal (dotted line in Figure 4.15 b) suffered more degradation than the other input, excited with 50% duty cycle signal (filled line in Figure 4.15 b).



(a)



(b)

Figure 4.15: Results obtained by HSPICE simulation of the threshold voltage degradation in Inverter (a) and 2-input Nand (b). The labels t_{SA}, t_{SB}, t_{RA} and t_{RB} are the stress time and the recovery time for both inputs – A and B – respectively.

The executed experiments replacing gates PMOS transistors by the proposed subcircuit generated the threshold voltage shifts presented in Table 4.3, considering the duty cycles for Nand inputs as depicted in Figure 4.15 (b).

The threshold voltage shift may cause delay degradation, so another experiment was built to better visualize this behavior. In this experiment, a ring oscillator composed by seven connected inverters which uses the proposed subcircuit was aged for five years. Then its oscillation frequency was compared to the original one, presenting a degradation of 18%, as depicted in Figure 4.16.

Operation Time	Inverter	Nand	
		Input_A	Input_B
1 hour	2,3 %	2,2 %	2,5 %
1 day	4,4 %	4,4 %	5,4 %
1 month	9,4 %	9,2 %	11,7 %
1 year	16,2 %	15,9 %	20 %
5 years	22,7 %	22,3 %	27,8 %

Table 4.3: ΔV_{th} induced by the proposed circuit according to gates operation time. (SCHUCH, 2009)

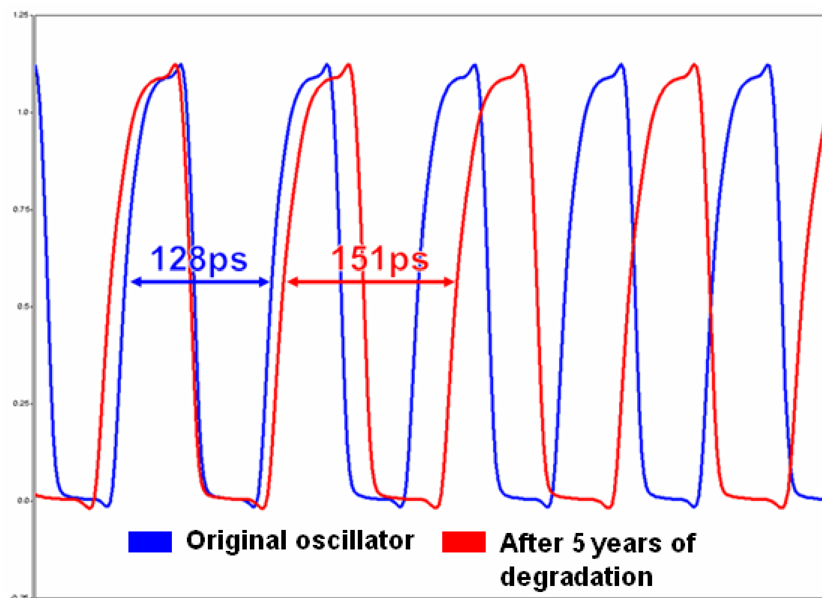


Figure 4.16: Electrical simulation result comparing oscillation frequency of a fresh oscillator and of a five-year degraded one.

Moreover, the proposed subcircuit was implemented and validated as an option to make an analytical model (VATTIKONDA, 2006) usable into electrical simulation. Designers may use this subcircuit instead of the PMOS transistor whenever the NBTI effect evaluation is desirable.

5 ROBUSTNESS INCREASING AGAINST NBTI

Designers have different ways of dealing with NBTI. The degradation in certain devices can be avoided by duty cycle management, transistor restructuring, standby input vectors selection or similar practices. Also, “on-the-fly” monitoring and correction techniques can be used to compose an adaptive design, which compensates the aging effects as they occur. Alternatively, even with no interference in the degradation process (no avoidance nor correction), guard-banding/over-design can be used to increase the margins in which the circuit still functional, increasing its life-time. Some of these techniques are explored in the next sections of this chapter.

5.1 Stress Reduction Techniques

Although operational frequency relation with NBTI is not so simple, the duty cycle has direct influence on the stress/recovery time over devices, thus in their degradation. Vattikonda (2006) brings the duty cycle tuning as stress reduction technique, exploring its effectiveness, as depicted in Figure 5.1 (a). For circuits standby periods, the input vectors control (IVC) technique (WANG, Y. 2007) aims to find the set of vectors which less contributes to degradation, reducing delay shifts as shown in Figure 5.1 (b).

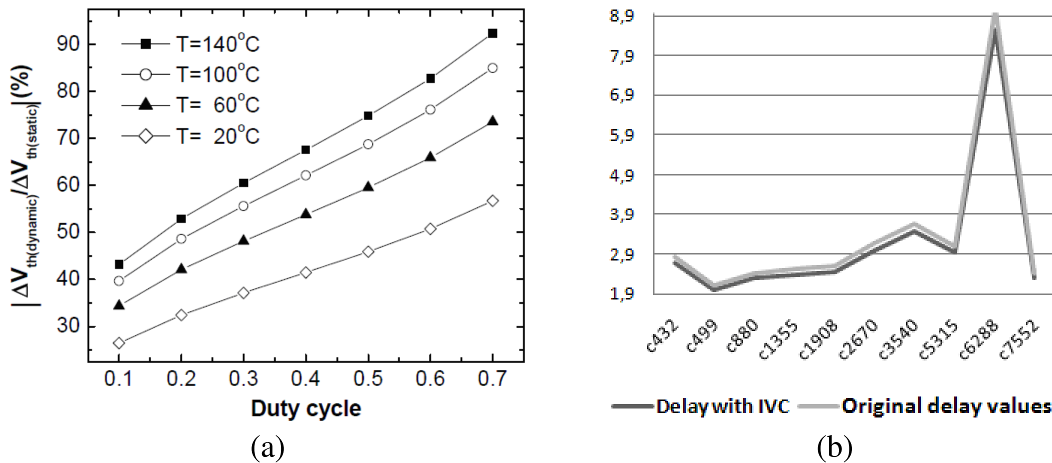


Figure 5.1: The effectiveness of (a) tuning duty cycle (VATTIKONDA, 2006) and (b) input vectors control technique (WANG, Y. 2007).

Other practices, exemplified in Figure 5.2, which also manage devices stress time comprehend logical restructuring (WU, 2009) and transistors stacks rearrangement (WU, 2009) (KUMAR, 2007). Logical restructuring explores functional symmetries to swap circuit inputs while keeps the functional equivalence. Transistors stack rearrangement the focus of evaluation in Butzen (2010b) and will be detailed in section 5.4.

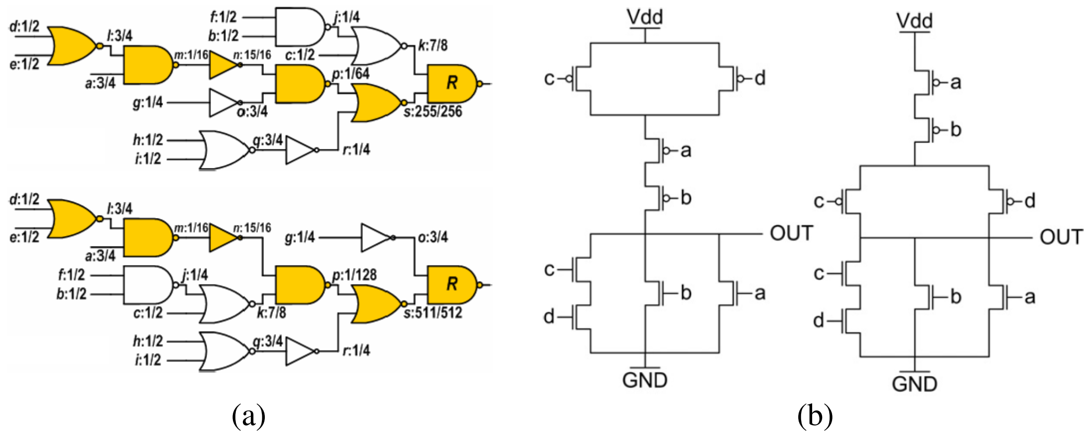


Figure 5.2: (a) An example of logic restructuring (WU, 2009). (b) An example of transistors arrangement restructuring (BUTZEN, 2010b).

Stand-by V_{dd} scaling, further explored for leakage reduction by Qin (2004), it is also mentioned by Kang (2008) as a stress reduction technique. It does not reduce the degradation by managing stress time/probability, but decreasing the electric fields involved in stress condition, reducing its resultant degradation.

5.2 Monitoring and Self-Adaptation

Another strategy to increase robustness against NBTI is the combined use of failure prediction (through degradation sensing) and self-correction/self-adaptation techniques.

One aging sensor design approach, proposed by Agarwal (2007), comprehends to modify a standard flip-flop by inserting a “monitoring” circuit block which detects any significant shifts in delay of the combinational logic whose output is connected to the data input of that latch of flip-flop. This is done by inserting in parallel to the FF an **aging robust** delay element (by managing its stress probability) and a stability checker. The delay element defines how long after the clock transition the stability checker will start operating, and if a transition occurs during its operation it will be considered a guardband violation. Guardband violations suggest near future fails due to aging. The Figure 5.3 illustrates this proposal.

The sensor approach proposed by Qi (2008) is simpler than the one discussed previously: it is a current-mirror based module which estimates the circuit aging by its own PMOS transistors degradation. As show in the schematic of Figure 5.4, the drain current of transistors P5 and N5 must be the same, so as the P5 ages (increasing its ON resistance) the voltage drop of V_{ddh} to V_{out} increases, this way V_{out} can be taken as metric for NBTI monitoring. The accuracy of this approach is not its strong point, but the fact of being very easily integrated to the corrective technique of adaptive body bias (which will be explained later on), due to its “analog” output, may be of designer interest.

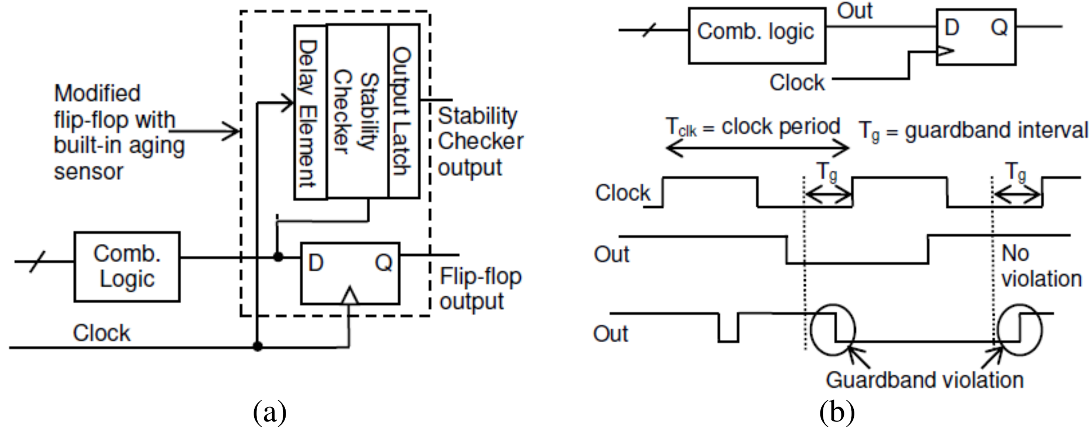


Figure 5.3: (a) Flip-flop with built-in aging sensor. (b) Guardband violation due to transistor aging. (AGARWAL, 2007)

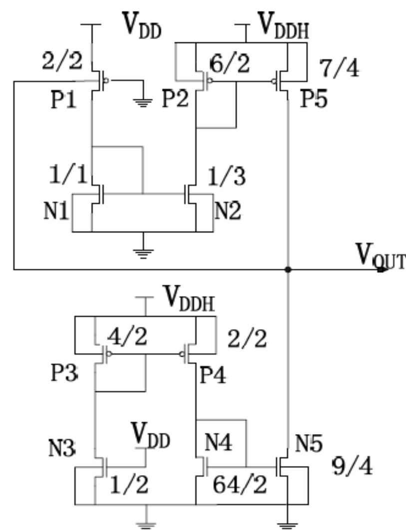
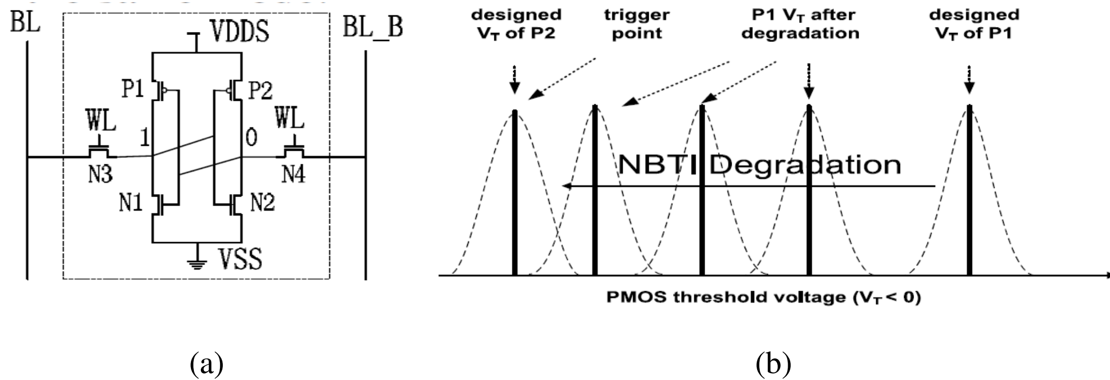


Figure 5.4: Current-mirrors based NBTI sensor schematic. (QI, 2008)

More recently, Qi (2010) explored another sensor design which was previously exposed by Guardiani (2009) and looks like a natural evolution of Cabe's (2009) proposal. As depicted in Figure 5.5 (a), this sensor is essentially an asymmetric 6T SRAM cell, it means, with initially unbalanced PMOS transistors. The sensor works in two modes: tracking and pooling. In the pooling mode, the sensor is disabled shortly by collapsing its word line (WL) and its supply VDDS to 0 for one or several clock cycles. While still keeping WL=0, restoring VDDS starts a fight between the two cross coupled inverters, and the stronger transistor (let's assume P1) ends up storing '1', avoiding this way the aging of P2 while itself degrades. After some degradation time, P1 and P2 become equally strong, and the first P2 "win" is used as aging alert, thus, this sensor' output is binary (enough aged/not enough) differently of Figure 5.4.

Previous works (CABE, 2009) show that to achieve reasonable sensing precision in the presence of variation, thousands of sensors may be required, so the small area of 6T SRAM sensor is a great benefit.



(a) (b)

Figure 5.5: (a) Sensor schematic. P1 is sized up to be stronger than P2 initially. Essentially an asymmetric SRAM cell with separate power supply. (b) NBTI degrades the stronger P1 over time. The solid lines are nominal design parameters and the dashed lines illustrate the effect of process variation. P1 and P2 may have different distributions. (QI, 2010)

All these sensors architectures are meant to be embedded monitors of transistor aging, having no intention of providing detailed information to the exterior of the chip as, for example, measurements techniques mentioned in section 4.1 have. Thus the sensors must be always implemented together with (and be controllers of) correction/adaptation techniques, otherwise there will be no reason for their monitoring. Some self-correction/self-adaptation designs for NBTI-induced aging include:

1. Variable clock frequency: The clock frequency may be reduced over time depending on the actual usage and aging of the chip in the field, increasing the paths delay margin, but this is rarely desired.
2. Adaptive body bias: Since the primary effect of NBTI is to increase the magnitude of threshold voltage of a PMOS transistor, forward biasing the source-body junction can compensate the change. The tradeoff involved in using forward body bias for aging is the decrease in magnitude of threshold voltages for PMOS transistors that have not aged, as this will result in increased leakage power. Nevertheless, this technique has been widely explored and it is easily integrated to sensors architectures similar to Qi's (2008) proposal (illustrated in Figure 5.4) since its output value can be directly used as body voltage regulator.
3. Adaptive power supply: Increasing the voltage supply will reduce delays, correcting any delay degradation caused by NBTI. The penalties in employing this strategy are: accelerating the aging process due to the increase in electric fields, and increasing power consumption. Also, it must be ensured that the increased supply voltage still within the maximum limit set by the technology. Zhang (2009) details this technique and proposes a scheduled voltage scaling for increasing circuit lifetime.
4. Dynamic modular substitution: As degradation signals are emitted by sensors, some reserve modules can start operating to replace the aged ones. This strategy fits perfectly to the 6T SRAM sensor approach of Qi (2010), since this sensor emits warnings exactly when it is operating as a symmetric 6T cell, thus the SRAM array lifetime can be extended as the sensor cells gradually replace failed cells through address mapping.

5.3 Over-Design

Over-designing, in this context, means to design the circuit faster than the necessary to its initial correct operation, creating an operational margin that guarantees the circuit will still functional even after suffering temporal performance degradation due to NBTI. The Figure 5.6 depicts a transistor's current degradation over its lifetime, illustrating the difference between employing over-design or adaptive design techniques.

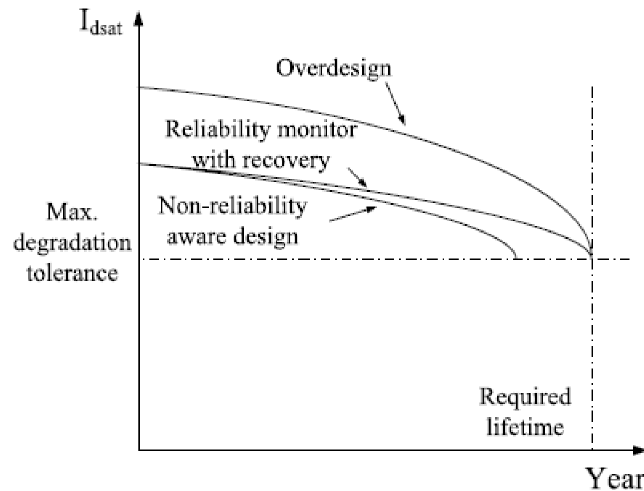


Figure 5.6: Circuit performance degradation comparison with different reliability aware designs. (QI, 2008)

The design margin desired in over-design strategy can be reached by different ways, like resizing devices at transistor-level or switching functional equivalent cells which have different delay characteristics.

An efficient transistor-level sizing technique is proposed by Kang (2006). In a rough overview, his work calculates, by applying a degradation model over a delay model (SAKURAI, 1991), each gate's delay as a function of its transistors sizes and degradation time; then uses Lagrangian Relaxation to solve a computational problem which aims minimizing area (sum of transistors' widths) while respecting some constraints like the maximum allowed delay. As NBTI affects significantly only PMOS transistors, the problem formulation is such that constraints are written for both the rising and falling arrival times, avoiding unnecessary oversizing of pull-down networks. Also, to reduce the complexity dependence on the number of devices, from exponential to linear, the proposed algorithm transforms the primary output delay constraint into constraints at each logic gates.

When it is provided a cells library, in which the designer cannot modify the cells but only choose between them, the overdesign also can be utilized, since there are sufficient choosing options. Kumar (2007) presents an NBTI-aware mapping which reaches this goal. As mentioned in section 4.3, their work characterizes cells' delay as input signals probability dependent functions. This way, only the cells which are able to still respecting circuit's delay constraints after the degradation period are chosen. This idea is illustrated in Figure 5.7.

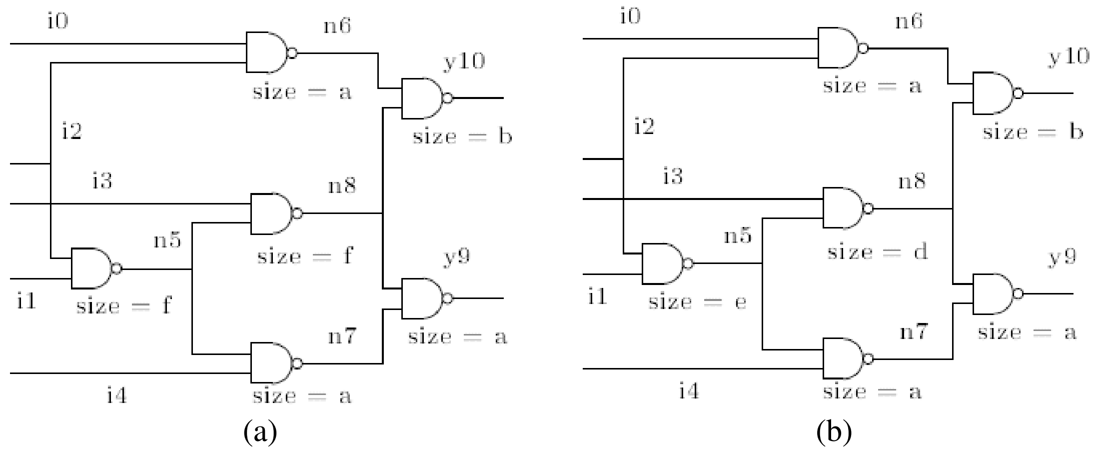


Figure 5.7: Results of technology NBTI-aware mapping for C17 benchmark. (a) Worst-case and (b) signal-probability based with area recover. “a” represents the minimum size. (KUMAR, 2007)

5.4 Transistor Network Restructuring Against NBTI Degradation

As exposed in previous sections, different solutions to mitigate NBTI degradation and achieve a robust design have been proposed in the literature. The developed work presented in this section evaluates the NBTI degradation at both circuit and gate levels, through a previously unexplored focus. At gate level, the transistor arrangement restructuring in the PMOS pull-up plane is investigated. At circuit level, NBTI effect is evaluated in circuits decomposed into more than one stage. This work is published in Microelectronics Reliability, 2010 (BUTZEN, 2010b).

5.4.1 Methodology

The long term NBTI prediction model proposed by Wang W. (2007a) is used to estimate the V_{th} degradation due to this effect for a given time ‘t’ and a signal probability ‘α’, as previously described in the NBTI modeling subsection, and replicated here:

$$\Delta V_{th} = b.\alpha^{n}.t^{n} \tag{4.6}$$

Regarding that b = 3,9 .10^{-3} V.$s^{-1/6}$ and ‘n’ is the time exponential constant and equals to 0.16.

The threshold voltage degradation has been estimated over 10 years and for several signal probabilities using the 45nm CMOS PTM process (PTM, 2010).

The stress probabilities for the devices have been computed considering equal signal probability of 0.5 for all primary inputs, and the particular position of each device in the transistor stack. In logic functions designed as circuits decomposed into multiple stages, each internal circuit node also considers its previous logic gate function probability.

Electrical characterization has been executed for different design versions of logic functions, considering fan-out 4 delay (nominal and degraded delay).

5.4.2 Simulation Results and Analysis

5.4.2.1 Transistor Restructuring

As mentioned previously, a logic function can be designed using different transistor networks. Figure 5.9 (a) and (b) illustrates two different pull-up PMOS designs for the AOI21 logic gate. These solutions present naturally different delay and power consumption behaviors. They also suffer different levels of degradation due to NBTI. In this section, the pull-up PMOS transistor arrangement is restructured to explore the NBTI degradation dependence.

Assuming all gate inputs with equal signal probability (50%), PMOS transistors that are connected to the power supply (V_{dd}) suffer more V_{th} degradation than the ones which are not connected directly to V_{dd}, as depicted in Figure 5.8. Based on the previous statement, a more robust CMOS gate design, with respect to NBTI degradation, may connect as few as possible transistors to the power supply.

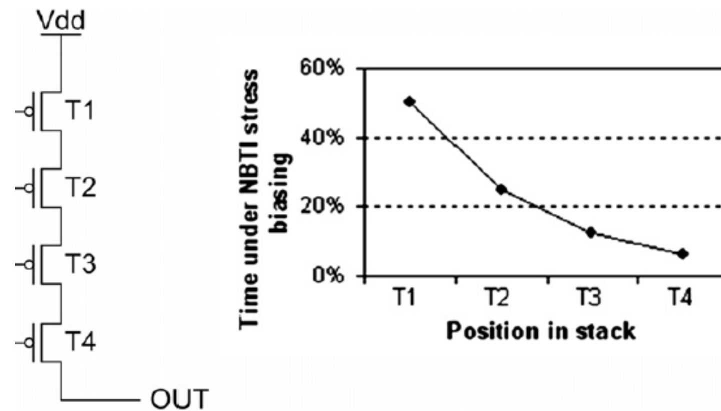
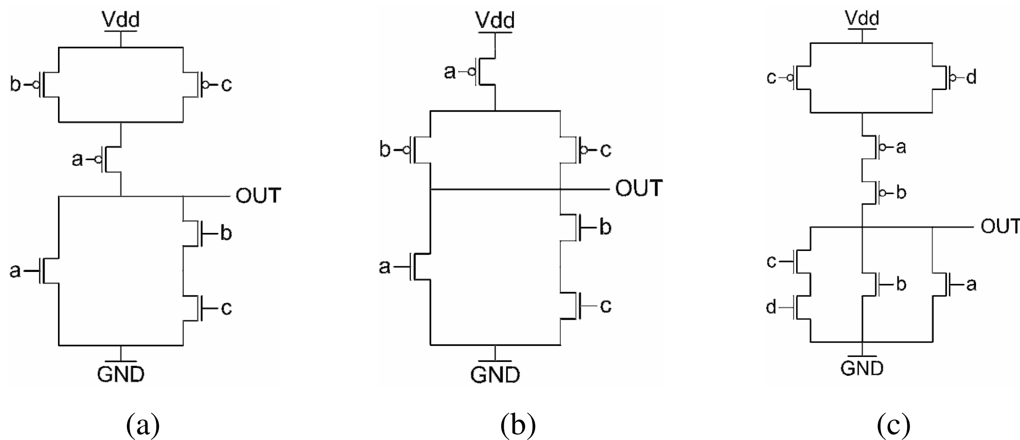
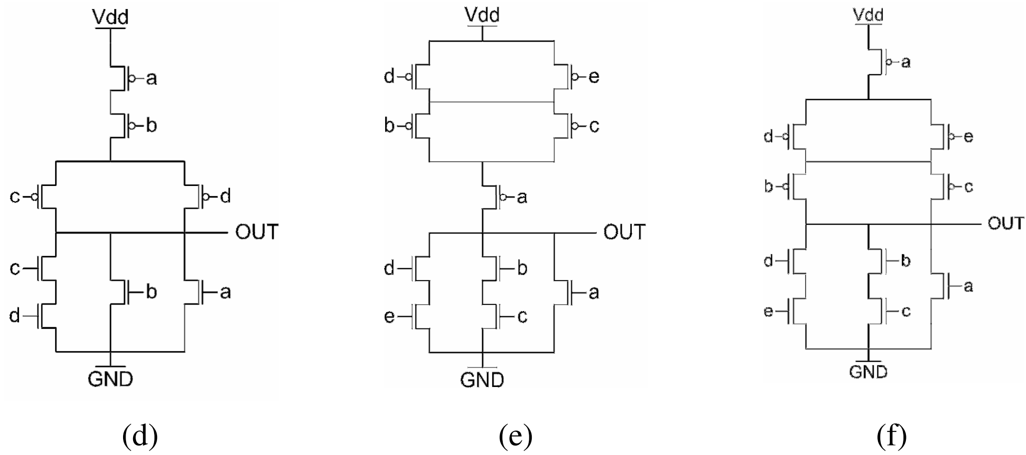


Figure 5.8: Time under stress biasing versus position in a four transistor stack. (BUTZEN, 2010b)

In the pull-up arrangement of the AOI21, AOI211, and AOI221 gates illustrated in Figure 5.9 (a), (c) and (e), respectively, two transistors are submitted to severe NBTI degradation since they are directly connected to V_{dd}. On the other hand, the topologies in Figure 5.9 (b), (d) and (f) present just one transistor connected to V_{dd} and consequently only this device suffers significant degradation. Figure 5.10 illustrates two versions of a typical circuit used in carry look-ahead adder unit, named here CLAunit. According to previous analysis, the gate depicted in Figure 5.10 (a) has more transistors close to V_{dd}, so suffers higher NBTI degradation than the one shown in Figure 5.10 (b).

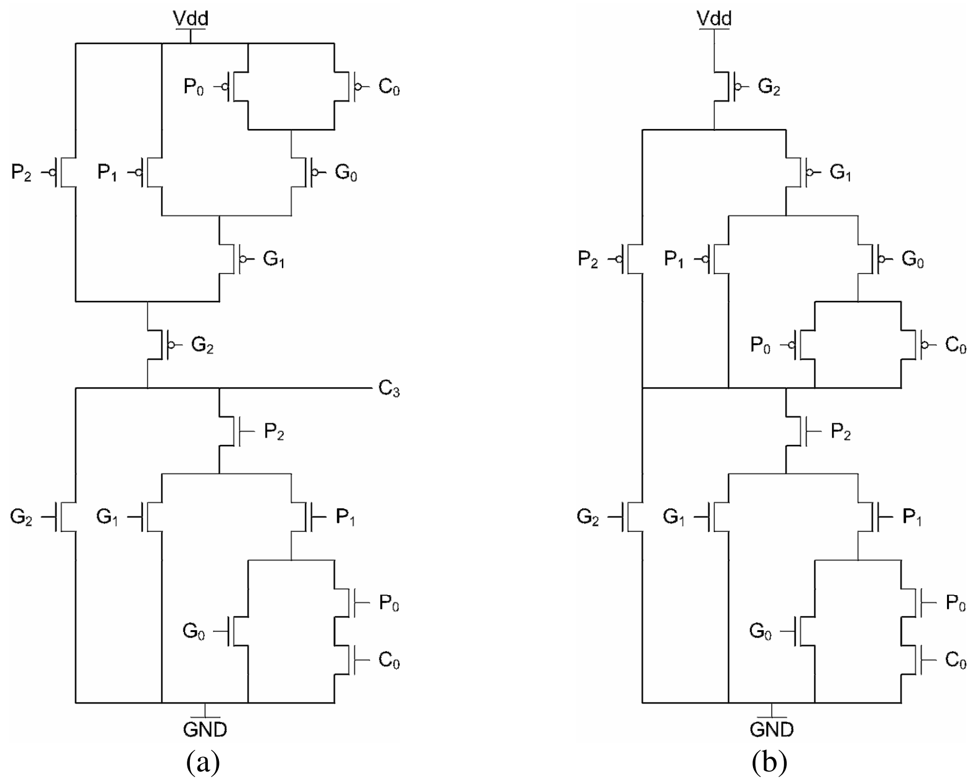


(a) (b) (c)



(d) (e) (f)

Figure 5.9: Logically equivalent CMOS gates. AOI21 in (a) and (b). AOI211 in (c) and (d). AOI221 in (e) and (f).



(a) (b)

Figure 5.10: Two logically equivalent ‘CLAunit’ gates.

Table 5.1 presents the degradation on the average rise propagation delay through gates depicted in Figure 5.9 and Figure 5.10 due to NBTI effect. The degradation recovered due to transistor arrangement restructuring is also presented. The results show that up to 15% of the NBTI timing performance degradation can be recovered by transistor arrangement restructuring.

Gate	Average Rise Delay Degradation (%)	Average Rise Degradation Avoided (%)
AOI21 (a)	8,69	10,74
AOI21 (b)	7,76	
AOI211 (a)	8,95	15,04
AOI211 (b)	7,60	
AOI221 (a)	8,66	5,61
AOI221 (b)	8,17	
CLAunit (a)	9,13	13,97
CLAunit (b)	7,85	

Table 5.1: Average rise delay degradation in gates depicted in Figure 5.9 and Figure 5.10. (BUTZEN, 2010b)

5.4.2.2 Single gate versus multiple stage circuit

Table 5.2 shows the average delay degradation of NAND3, NOR3, AOI21, AOI211, and AOI221 gates designed as a circuit decomposed into multiple stage compared to their single stage version. The chosen single stage versions are the ones that have presented less delay degradation in previous section. The decomposed version of NAND3 referred by Table 5.2 is composed by two NAND2 being the first followed by an inverter, and the decomposed version of NOR3 follows the same structure changing the NAND2 gates by NOR2 gates. The decomposed versions of AOI21, AOI211, and AOI221 are shown in Figure 5.11. In these figures, the difference between (b) and (c) versions is the input connections ordering on the PMOS transistor stack of the NOR3 gate in the last stage. The up connection in the NOR3 symbol represents the one connected to the PMOS transistor closer to V_{dd}.

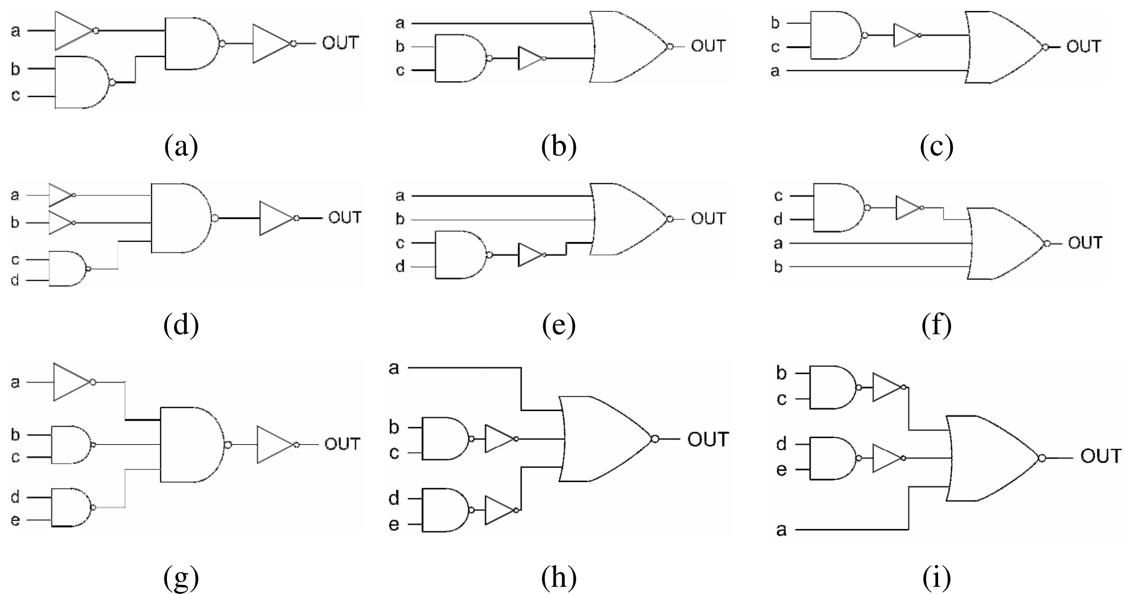


Figure 5.11: Decomposed versions. (a), (b) and (c) AOI21. (c), (d) and (f) AOI211. (g), (g) and (i) AOI221.

The ‘CLAunit’ circuit, depicted in Figure 5.10, is also evaluated and the results are also presented in Table 5.2. In this analysis, two decomposed versions are evaluated.

These versions are illustrated in Figure 5.12. A decomposed three gate level version is depicted in Figure 5.12 (a), Figure 5.12 (b) illustrates a decomposed seven gate level version that instantiates logic gates with just two inputs.

The NBTI effect just degrades the threshold voltage of PMOS transistors. Therefore, as verified in the previous subsection (5.4.2.1), the rise delay is increased in single stage design approaches. The results presented in Table 5.2 show that the decomposed versions present degradation in both rise and fall delay. In these multiple stage designs, the rise delay degradation may not be as severe as in single stages at the penalty of fall delay degradation. It can be explained since the fall output transition depends on at least one rise transition at an intermediate node, which is defined by a pull-up network composed by PMOS transistors.

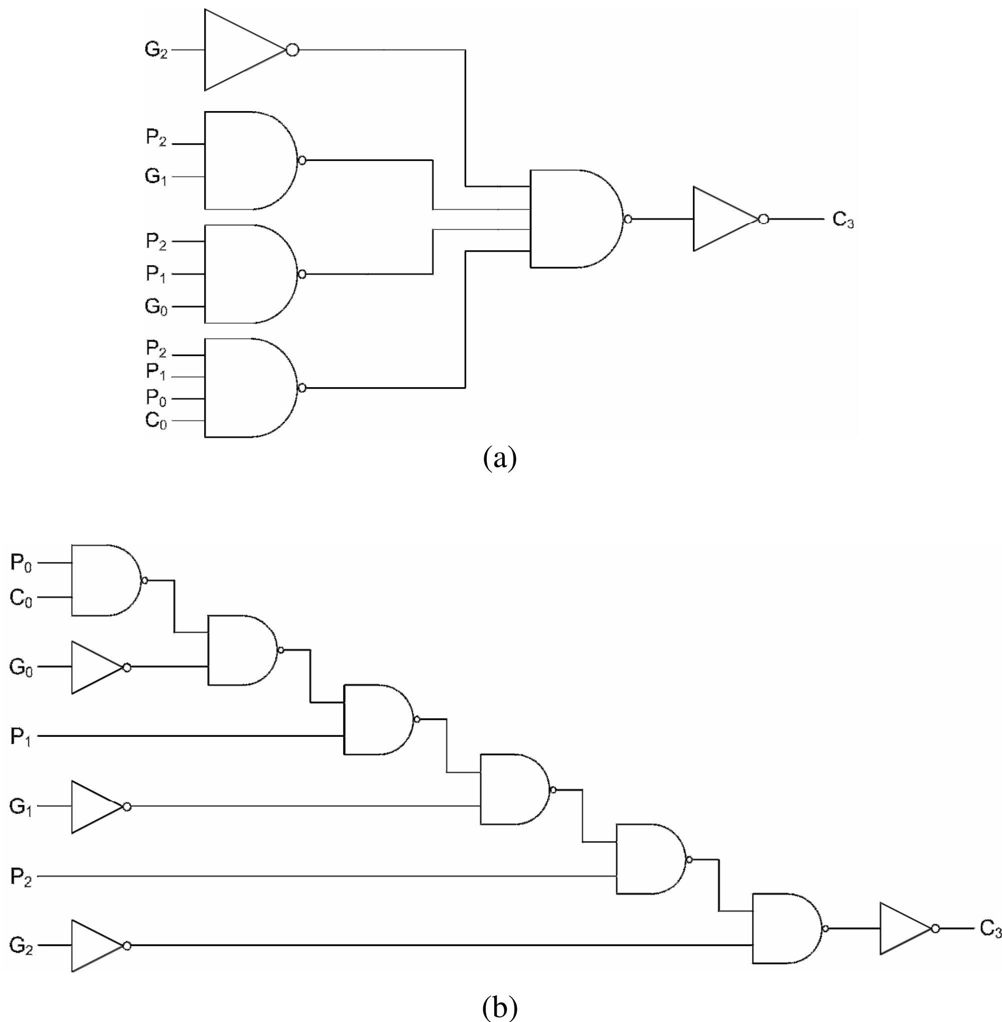


Figure 5.12: ‘CLAunit’ decomposed versions.

In single stage CMOS gates, the logic paths responsible for the fall output transition are composed solely by NMOS transistors and should not be affected by NBTI. However, this single stage designs may even present a small improvement in fall delay. It is caused by the weakening of PMOS transistors current, reducing the influence of the pull-up network during the output fall transition.

Logic Function		Rise delay degradation (%)	Fall delay degradation (%)
NAND3	Single gate	7,63	0,00
	Decomposed version	7,65	1,22
NOR3	Single gate	8,11	-0,18
	Decomposed version	6,28	1,35
AOI21	Single gate	7,76	-0,08
	Decomposed version (a) Decomposed version (b) Decomposed version (c)	6,23 7,76 7,90	2,12 1,38 1,10
AOI211	Single gate	7,60	-0,26
	Decomposed version (a) Decomposed version (b) Decomposed version (c)	5,33 8,08 8,48	2,81 0,76 0,59
AOI221	Single gate	8,17	-0,36
	Decomposed version (a) Decomposed version (b) Decomposed version (c)	5,39 8,10 8,59	2,60 1,13 1,02
CLAunit	Single gate	7,85	-0,31
	Decomposed version (a) Decomposed version (b)	5,59 5,98	2,35 2,89

Table 5.2: Average delay degradation of logic functions designed as a single CMOS gate and as a decomposed circuit in multiple stages of basic logic gates. (BUTZEN, 2010b)

Moreover, this set of results show that the transistor arrangement restructuring is a potential design solution to recover the delay degradation due to NBTI effect.

6 CONCLUSIONS

This thesis has discussed project challenges and reliability concerns of digital integrated circuits built in most recent technologies.

It has been provided an overview about nanometric regime physical effects, followed by the exploration of NBTI, which is considered the primary concern in devices lifetime reliability and has been a constant research subject.

A solid study about the related literature was accomplished, and summarized in this thesis, acting as project guidelines as well as technical background to future works and novel proposals.

One contribution of this work is in the NBTI evaluation topic, an electrical circuit equivalent to a chosen analytical NBTI R-D model has been proposed. Electrical simulations have demonstrated that it is suitable to predict CMOS cells degradation due to NBTI aging effect, evaluating individually each PMOS transistor at pull-up logic gate network. This approach also carries benefits like: no need of any previous computation about the stress probabilities, and topology transparency to the designer.

Another contribution of this work is in the robustness increasing against NBTI topic, an analysis about the several design solutions which can be used to represent a certain logic function has been done, considering the influence in terms of the NBTI timing performance degradation. The results show that the transistor arrangement restructuring is a potential design solution to prevent the delay degradation due to NBTI effect. This technique can be used combined with other ones already proposed in the literature to achieve better results. The use of logic functions decomposed into more than one stage can also be a solution to reduce the rise delay degradation at a cost of fall delay degradation.

Future works include the proposal of estimators to the explored effects, in order to evaluate different transistor networks behavior in this theme. Another future task is to expand all performed gate analysis to circuit-level, as well as explore different ways of attaching nanometric effects evaluation into available commercial flows.

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APENDIX

The bellow code is the final implementation (containing some optimizations) of the developed work described in section 4.4.

```
*Empirically determined parameter //According to [5]
.param Vbulk2Vth = 5.62

*Tech parameters
.param vddnom = 1.1
.param vssnom = 0

*.include /<INCLUDE THE TRANSISTOR MODELS PATH HERE>

*********************************************************************
* MODULAR NBTI CONTROL CIRCUIT
* Optimized version developed in 2009, September
*********************************************************************

.SUBCKT CONTROL_CIRCUIT source gate drain

*********************************************************************
* Time Modules
*********************************************************************
*   Vth = 0.165V //According to [3]

.param Vth = 0.165

*Source responsible for indicating when transistor is under stress
E_str in_stress 0 VOL='(-1*(v(gate)-v(source)))>Vth'

*The total time of simulation is the negative voltage in tot_time
I_tot_time     tot_time    0     0.01
C_tot_time     tot_time    0     0.01  IC=0

*The stress time is the negative voltage in str_time
I_str_time     str_time    0     0.01
C_str_time     str_time    0     0.01  IC=0
R_str_time     str_time    0     R='max(1E-5,v(in_stress)*1E99)'

*The recovery time is the negative voltage in rcv_time
I_rcv_time     rcv_time    0     0.01
C_rcv_time     rcv_time    0     0.01  IC=0
R_rcv_time     rcv_time    0     R='max(1E-5,(1-v(in_stress))*1E99)'

*********************************************************************
* Control Module
*********************************************************************
```

```
************************************************************
* STRESS MODULE
************************************************************

**********************************************
* "exp(Eox/E0)" equation section
**********************************************
*   Eox = (Vgs-Vth)/Tox   //According to [1]
*   Toxe = 1.85nm    //According to the utilized PMOS_VTL model
above
*   Toxe = 1.75nm    //According to [2]
*   E0 = 2 MV/cm = 200000000 V/m    //According to [1] and [2]

.param Toxe = 1.85E-9
.param E0 = 200000000

*   Tox*E0 is constant = 0.37
*   NO negative value for Vgs-Vth accepted (max function)
//arbitrary, because stress equation will only be active above Vth
*   Vgs replaced by Vsg in order to adjust the signal
*   Vth refreshed by last value of recovery deltaVth
*   This component roughly varies between 1V and 15V

*Verification source
*E_expEoxE0    expEoxE0    0     VOL='exp( max(0,(v(source)-v(gate)-
Vth-v(recoveryStable))) /0.37 )'

**********************************************
* "exp(-Ea/kT)" Kv section
**********************************************
*   Ea = 0.13 eV   //According to [1] and [2]
*   k = 8.617343E-5 eV/K (Boltzmann constant)
*   T = 373 Kelvin //arbitrary
*   exp(-Ea/kT) = exp(-5.028597246) = 0.006547989

**********************************************
* "sqrt(Cox*(Vgs-Vth))" Kv section
**********************************************
*   Cox = eox/Tox //According to [1] and [2]
*   eox = 3.9 e0 = 3.9*8.85*10E-14 //According to [4]

.param Cox = 1.86567567567E-4

*   NO negative value for Vgs-Vth accepted (max function)
//arbitrary, because stress equation will only be active above Vth
*   Vgs replaced by Vsg in order to adjust the signal
*   Vth refreshed by last value of recovery deltaVth
*   This component roughly varies between -10mV and 20mV, 0 and 20mv
with max function

*Verification source
*E_sqrtCoxVgsVth     sqrtCoxVgsVth     0     VOL='sqrt( Cox*
max(0,(v(source)-v(gate)-Vth-v(recoveryStable))) )'

**********************************************
* "1-Vds/alpha(Vgs-Vth)" Kv section
**********************************************
*   alplha = 1.3 //According to [1] and [2]
```

```
.param alpha = 1.3

*   Vgs replaced by nominal vdd since only the static (like
subthreshold leakage) matters and dynamic behavior of Vgs may
overload the division
*   Vds replaced by Vsd in order to adjust the signal
*   This component roughly varies between 0V and 1V

*Verification source
*E_VdsalphaVgsVth          VdsalphaVgsVth    0     VOL='1-
(v(source)-v(drain)) / (alpha*(vddnom-Vth-v(recoveryStable))) '

***********************************************
* "A*Tox" Kv section
***********************************************
*   A = 1.8 mV/nm/C**0.5 = 1800000 V/m/C**0.5 //According to [1] and
[2]
*   A*Tox is constant = 0.00333

***********************************************
* "K" equation section
***********************************************
*   A*Tox*exp(-Ea/kT) is constant = 0.00002180480337
*   This component roughly varies between 0V and 4uV

*Using verification sources
*E_Kv    Kv    0     VOL='0.00002180480337 * v(sqrtCoxVgsVth) *
v(VdsalphaVgsVth) * v(expEoxE0)'

*This equation might be included into the stress equation source, it
is separated only for simplicity
E_Kv     Kv    0     VOL='0.00002180480337 *
(sqrt(Cox*max(0,(v(source)-v(gate)-Vth-v(recoveryStable))))) * (1-
(v(source)-v(drain))/(alpha*(vddnom-Vth-v(recoveryStable)))) * exp(
max(0,(v(source)-v(gate)-Vth-v(recoveryStable)))/0.37)'

***********************************************
* Stress equation
***********************************************
*   sqrt (timeAdjust * Kv^2 * sqrt(t) + deltaVth^2) + deltav
*   deltav = 5mV //According to [1] and [2]
*   timeAdjust accelerates the aging process = 2592000 // arbitrary,
each second will be equivalent to 30 days

.param deltav = 0.005
.param timeAdjust = 2592000

*   An ideal diode was added to the ideal switch in order to avoid
|Vsg-Vth| fake recovery during Vsg down
*   Optimization made: v(in_stress) multiplies deltav in order to
remove 2 switches
*   DeltaVth caused by NBTI is the voltage in stressEquation node

R_stressModule stressEquation    stressStable
   R='max((v(stressStable)-v(stressEquation))*1E99, max(1E-5,(1-
v(in_stress))*1E99))'
E_stressModule stressEquation    0
   VOL='sqrt(timeAdjust*v(Kv)*v(Kv)*sqrt(-
1*v(str_time))+(v(recoveryStable)*v(recoveryStable)))+deltav*v(in_st
ress)'
```

```
C_stressModule  stressStable           0     C=0.1


************************************************************
* RECOVERY MODULE
************************************************************
*   n = 0.35 //According to [1] and [2]

.param n = 0.35

E_recoveryModule     recoveryEquation  0     VOL='max(0,
(v(stressStable)-deltav)*(1-sqrt(n*v(rcv_time)/v(tot_time))) )'
R_recoveryModule     recoveryEquation  recoveryStable    R='max(1E-
5,v(in_stress)*1E99)'
C_recoveryModule     recoveryStable    0     C=0.1

.ENDS


********************************************************************
* MODULAR PMOS TRANSISTOR WITH NBTI EFFECT
********************************************************************

.SUBCKT PMOS_NBTI_TRANSISTOR source gate drain bulk W=0.135000U
L=0.045000U AS=0.009112P AD=0.009112P PS=0.270000U PD=0.270000U
M_pmos_transistor    source      gate  drain bulk_nbti   PMOS_VTL
W='W' L='L' AS='AS' AD='AD' PS='PS' PD='PD'
x_control source      gate  drain CONTROL_CIRCUIT
Enbtia   bulk_nbti   bulk
   VOL='Vbulk2Vth*v(x_control.stressEquation)'
.IC v(bulk_nbti)=vddnom
.ends


.SUBCKT NMOS_NBTI_TRANSISTOR source gate drain bulk W=0.090000U
L=0.045000U AS=0.004050P AD=0.004050P PS=0.180000U PD=0.180000U
M_nmos_transistor    source      gate  drain bulk  NMOS_VTL W='W'
L='L' AS='AS' AD='AD' PS='PS' PD='PD'
.ends


********************************************************************
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********************************************************************
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