Analysis of the Negative-Bias-Temperature-Instability on Omega-Gate Silicon Nanowire SOI MOSFETs with different dimensions

Vanessa C. P. Silva[1], Gilson I. Wirth[2], João A. Martino[1], and Paula G. D. Agopian[1, 3]

[1] LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil
[2] UFRGS, Rio Grande do Sul Federal University, Porto Alegre, Brazil
[3] UNESP, Sao Paulo State University, Sao Joao da Boa Vista, Brazil
email:vcpsilva@usp.br

***Abstract*— This work presents an experimental analysis of the Negative-Bias-Temperature-Instability (NBTI) on omega-gate nanowire (NW) pMOSFETS transistors and the trends analysis from simulations, focusing on the influence of channel length and width, since it is an important reliability parameter for advanced technology nodes. 3D-numerical simulations were performed as guideline for a trend analysis. The results show a high NBTI in NW ($\Delta V_T \approx$200-300mV – for W_{NW}=10nm) due to a high defect density and high gate oxide electric field accelerating the NBTI effect providing a higher degradation.**

***Index Terms*—NBTI, NW, SOI, MOSFET.**

I. INTRODUCTION

The Negative-Bias-Instability-Temperature (NBTI) is one of the major reliability concerns for advanced technology nodes, due to the temperature increase that can lead to circuit failure and degrade its lifetime [1]. For pMOS devices the NBTI degradation is accelerated when submitted at elevated temperatures and with a negative bias at the gate (inversion mode) [1][2].

The degradation mechanisms are basically related to the interaction of channel inversion layer charge carriers with traps close to the Silicon (Si)/Silicon Oxide (SiO_2) [2][3]. This effect causes a shift in the threshold voltage to a higher value in module when increasing time, leading to a reduction in the drain current level [4].

The omega-gate nanowire transistors present a cylindrical structure providing a higher electric field when compared to planar devices. Furthermore, this cylindrical structure presents a higher defect density in the gate oxide due to processes fabrication, and this high stress level caused by the electric field and the defects in the oxide turns the device more susceptible to NBTI effects [5][6].

This effect was barely studied for nanowire transistors, and as it is an important reliability parameter for this promising technology, due to its susceptibility for scaling, in this work is presented an analysis of this effect in Omega-Gate nanowire SOI pMOSFETs. The NBTI effect was analyzed through experimental data varying the channel width (W_{NW}) and the channel length (L), and the simulations were used as a support for the presented behavior trends of NBTI for different dimensions.

II. DEVICES CHARACTERISTICS

The devices used in this work were the p-type Omega-gate silicon nanowire transistors fabricated at CEA-LETI, with the following characteristics: channel length (L) of 400 nm and 80 nm, channel width (W_{NW}) of 220 nm and 10 nm. The interfacial layer is composed by 0.8 nm of SiO_2 and 2.3 nm of HfSiON resulting in an effective oxide thickness (EOT) about 1.3 nm. The buried oxide thickness (t_{oxb}) is equal to 145 nm and the silicon thickness/fin height (h_{fin}) is 10 nm. These characteristics are represented in Fig. 1 where it is shown the device cross section for both studied W_{NW}, where t_{oxf} represents the gate oxide thickness.

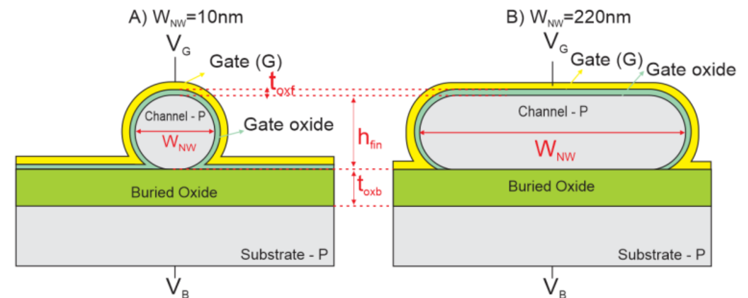

Fig. 1 – Cross section of Omega-Gate NW transistor with W_{NW}=10 nm (A) and W_{NW}=220 nm (B) [7].

III. MEASUREMENTS AND SIMULATIONS ADJUSTMENT

To measure the NBTI effect, the semiconductor analyzer B1500A from ©Keysight was used. In the stress phase, a stress gate voltage ($V_{GSstress}$) of -2.5 V was applied at a temperature of 125 °C, during 1000 s. The drain current level was kept constant after the stress time with VGS=-0.6 V and VDS=-0.1 V, when biased in this region before the stress phase, the current level should be about -1 µA.

The measurement of ten fresh (never measured) devices was performed to avoid erroneous analysis. The pre-stress biased region was with V_{GS} from -0.3 V to -0.9 V and V_{DS}=-0.1 V, this small range was chosen to avoid previously stress.

To extract the NBTI degradation, the Spot-Id Sense Measurement method was used [8].

Prior to stress, the I_{DS} x V_{GS} characteristics are measured, limiting V_{GS} to -0.9V. Stress (V_{GS} stress) is then applied, and after each stress time, the I_{DS} is measured at the fixed V_{GS} sense, right after the stress time, during the recovery time (~ 50 µs). This extracted I_{DS} is then interpolated in our reference curve (I_{DS} x V_{GS} with no stress), to obtain the correspondent V_{GS} value, which will give us the

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ΔV_T. Fig. 3 is presents the extraction procedure for ΔV_T [8]. These measurements steps were repeated seven times, for each stress time: 1, 10, 50, 100, 200, 500 and 1000 seconds, in order to obtain the threshold variation in each point.

Hence, the V_{GS} sense is a fixed voltage equal to -0.6 V which corresponds to a pre-stress current value of approximately -1 μA, for W_{NW}=10 nm with L=80 nm and W_{NW}=220 nm with L=400 nm. For the other device with W_{NW}=10 nm and L=400 nm the current level is lower (in module) due to its W_{NW}/L ratio. Fig. 2 presents the region in the experimental transfer curve for all measured devices where the I_{DS} was extracted.

The software Sentaurus TCAD developed by Synopsys® was used to perform the three-dimensional simulations. The simulated devices have the same characteristics from the experimental ones and the used models considered the majority and minority carrier mobility and its dependence with temperature besides impurity physics effects and electron-hole spreading, electrical field dependence of the mobility and the high electric field saturation.

The NBTI effect was simulated using the Two-Stage NBTI Degradation Model from Sentaurus, and it was used to analyze the trends of the NBTI in the device, not the effective values. This model refers to the generation of interface traps and positive oxide charges and it considers that the degradation occurs in two stages:

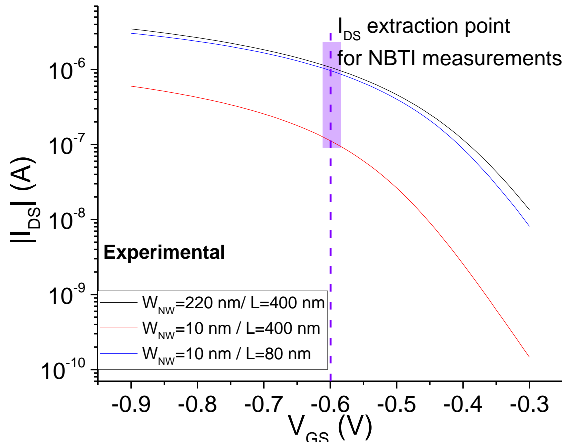


Fig. 2 – I_{DS} x V_{GS} characteristics measured before stress.

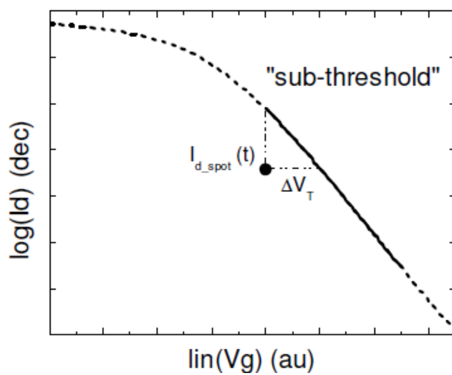


Fig. 3 – Extraction procedure of V_T for a given V_{GS}. [8]

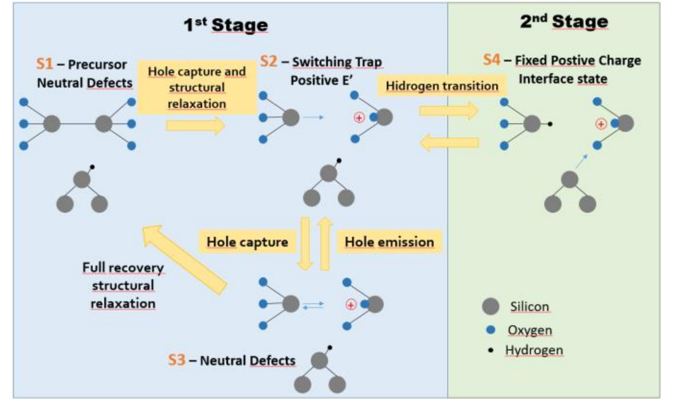


Fig. 4 – Representation of the Two-Stage NBTI degradation model. Adapted from [3].

1st stage: it is considered the creation of dangling bonds in amorphous oxide (E' centers) from their neutral oxygen vacancies precursors, the generation of positive and neutral E' centers as a result from the charging and discharging of these E' centers and it is also considered the total annealing of these E' centers to neutral oxygen vacancies.

2nd stage: it is considered that the trapped charge becomes a permanent defect, i.e. a dangling bond at Si-SiO_2 interfaces, called poorly Pb centers.

In Fig. 4 it is represented the two degradation stages, in this model it is considered that the trap has four internal states [3][9]:

- S1: represents the precursor state, i.e. the oxygen vacancy;
- S2: in this state the E' centers become positively charged;
- S3: represents the E' centers as a neutral defect;
- S4: represents the state when the positively charged E' centers become a fixed charged (permanent defect).

The evaluation of NBTI effect in the simulations is through the variation in the threshold voltage (ΔV_T), which is obtained by the current level variation just after stress time. There were three phases during the simulation:

1. Pre-stress time: the applied V_{GS} is -0.6 V and V_{DS}=-0.1 V;
2. Stress time: the stress time varies from 1 second up to 1000 seconds with V_{GS}=-2.5 V and V_{DS}=0 V;
3. Recovery time: this phase lasts for 50 s and the V_T is extracted in the very begging of this phase.

Fig. 5 represents these three phases with V_{GS} indicated in each phase.

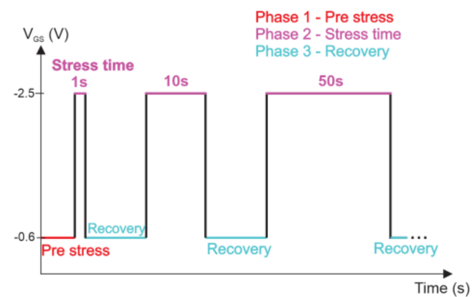


Fig. 5 – Representation of the three phases of simulated NBTI effect with V_{GS} as function of time [7].

IV. RESULTS AND DISCUSSION

The applied stress with high $|V_{GS}|$ causes a shift in V_T since it generates interface traps and oxide defects that can trap the holes and also the hole trapping in preexisting oxide defects contributes to ΔV_T [10].

The first analysis is the degradation effect in V_T and I_{DS} as a function of stress time, for L=400 nm and varying W_{NW}, as presented in Fig. 6, with the average values of the ten fresh measured devices and its respective standard deviation. The right-axis presents the percentage variation of degradation in I_{DS}, ($\Delta I_{DS}/I_{DS}$), where the divider corresponds to the drain current for V_{GS}=-0.6 V before stress.

For W_{NW}=220 nm (square symbol) the variation tendency is similar when comparing ΔV_T and ΔI_{DS}, while for W_{NW}=10 nm (circle symbol) the ΔV_T variation becomes more abrupt for t_{stress}>50 s than for the variation in ΔI_{DS}, which presents the smallest variation with time. This difference in degradation for V_T and I_{DS} is related to the fact that the extraction point of degradation was for a fixed V_{GS} of -0.6 V, close to V_T which presents a non-linear region, as presented in Fig. 2, explaining the non-linear relation between the degradation in V_T and I_{DS}.

The ΔV_T degradation for W_{NW}=10 nm is higher than for W_{NW}=220 nm, which would not be expected if considering a planar device, since ΔV_T can be given by ΔV_T=Ndef*dvt, where Ndef is the number of defects in the device and dvt is the average variation in V_T due to a single defect. Ndef for planar devices is proportional to its area, while dvt is inversely proportional and this compensation should not influence ΔV_T [11]. As W_{NW}=220 nm is very large it can be considered a quasi-planar device. But when considering that in the experimental device there is a higher defect density in the corners, it should led to an increase of NBTI when reducing W_{NW}, since it becomes more influent, as presented in the experimental data and reported in reference [12] where was simulated the NBTI with different charge concentration in lateral and top surface.

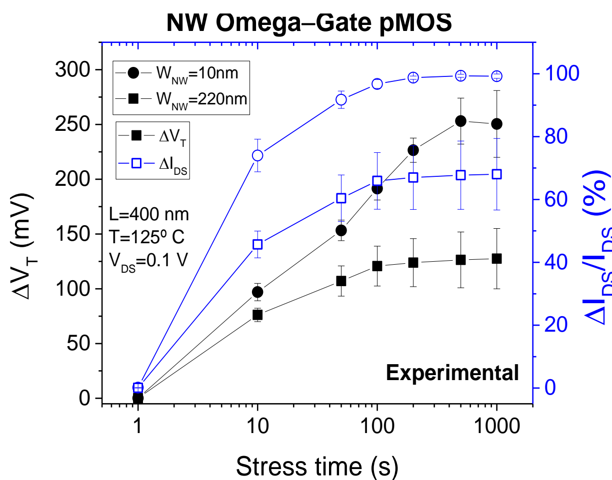


Fig. 6 – Experimental measurement of ΔV_T and $\Delta I_{DS}/I_{DS}$ as a function of stress time, for W_{NW}=220 and 10 nm and L=400 nm.

In Fig. 7 it is presented the degradation in V_T and I_{DS} as a function of time, varying the transistor channel length, with W_{NW}=10 nm. In this case, the device with L=400 nm still presents the highest variation in I_{DS} with stress time increase (as in Fig. 6), and the variation in ΔV_T is slightly higher for L=80 nm which is not significant whereas for longer stress time, the error bars from both devices overlap.

The influence of L in $\Delta I_{DS}/I_{DS}$ and in ΔV_T is not significant, especially for longer stress time, where the error bars overlaps, however considering the dependence on W_{NW} variation, there is a significant influence in both analyzed parameters.

The numerical simulations were performed to obtain the NBTI trend degradation. Firstly, the transfer curve (dc characteristics) was used to calibrate the simulations, to make it more realistic. To calibrate these characteristics with the experimental data, were done some adjustments at the mobility and work function parameters, at room temperature.

Although the calibration on the dc characteristics, when adding the NBTI model, to analyze this effect, i.e., transient analysis, the parameters that influence the dynamic characteristics were not adjusted. The proposal is to do a trend analysis of the precursor density defects on the variation in ΔV_T, presented in Table I.

The only simulation fit was in I_{DS} X V_{GS} curves at room temperature, where some parameters as mobility and work function were adjusted with the experimental data. To simulate the NBTI was added the Two-Stage NBTI model, and the precursor defects density (N_0) was the only fitted parameter, it is presented in all $Si\text{-}SiO_2$ interfaces and is kept constant along this entire interface, and the stress time was also set up. The devices dimensions, bias and temperature were the same from the experimental ones.

Table I presents the simulated values of N_0 and its respective obtained ΔV_T variation with stress time, from 0 s to 1000 s. From N_0=1.10^{12}cm^{-2} to 5.10^{12}cm^{-2} the ΔV_T increased approximately four times and from 5.10^{12}cm^{-2} to 1.10^{13}cm^{-2} increased approximately 1.6 time, demonstrating that the increase of defect density causes a greater variation in ΔV_T. Thus, the ΔV_T values that were closer to the experimental is the N_0=1x10^{13} cm^{-2}, being the considered defect density value for the next analysis.

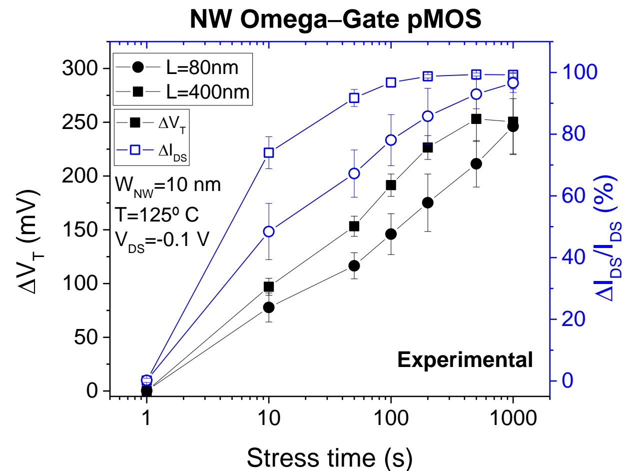


Fig. 7 - Experimental measurement of ΔV_T and $\Delta I_{DS}/I_{ds}$ as a function of stress time, for L=400 and 80 nm and W_{NW}=10 nm.

		ΔV_T variation(mV)
1x10[12]	29 – 30.4	1.4
5x10[12]	122 – 127.2	5.2
1x10[13]	178 – 185	7
Experimental	**0 – 250**	**250**

With simulation it was only done a qualitative analysis of the results, i.e. the trends analysis. The simulations for both channel widths were done with the same defect density, considered constant along the all gate oxide. The NBTI behavior along time was not calibrated with the experimental, it was kept the default parameters.

Fig. 8 presents the simulated NBTI effect for devices with W_{NW}=10 nm and L=80 nm and 400 nm and for W_{NW}=220 nm and L=400 nm. Comparing the influence of W_{NW}, it is observed the opposite behavior from the experimental, where the wider device presents a higher degradation. A possible explanation for this is the step to round the corners in the process fabrication, which generates more defects in the oxide. As the channel gets narrower these defects become more pronounced explaining the obtained experimental results in Fig. 6.

In simulations the charge density was considered the same for both W_{NW} and considered the same along the gate oxide even in the corners. The expected behavior in these conditions is the one presented in Fig. 8, where with the channel width scaling there is a reduction in ΔV_T. From table I the influence of the charge density is also presented, where it is noticed that the increase in charge density leads to an increase of ΔV_T, meaning that if a higher density is added in the corners for W_{NW}=10 nm the simulated results would present a higher degradation when compared to W_{NW}=220 nm, as reported in [12], where are presented simulations with higher charge density in the lateral surfaces. These simulations indicate that when increasing the charge density, the ΔV_T increases, and if a higher density is added in the corners it would get in agreement with the experimental data, which presents a higher degradation for the narrow device.

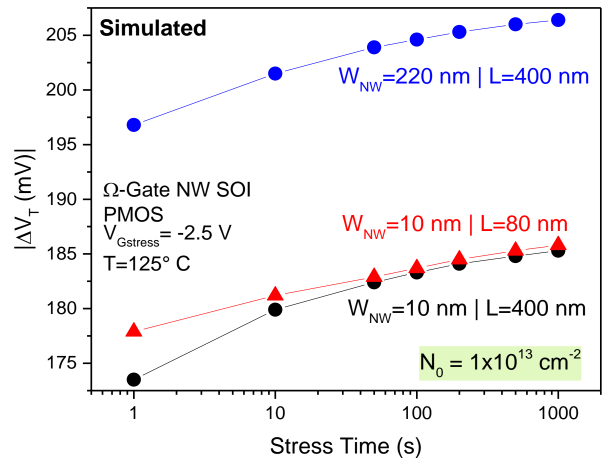
The NBTI can also be explained through the stress oxide electric field at the Si-SiO_2 interface (E_{ox}), which is expressed by equation (1) for NW [5] and equation (2) for planar device [13]:

$$E_{ox} = \frac{(V_{GSstress} - V_T)}{R\ln(1+\frac{EOT}{R})} \quad (1)$$

$$E_{ox} = \frac{(V_{GSstress} - V_T)}{EOT} \quad (2)$$

where R is the NW radius.

In Table II it is presented the calculated and simulated values of E_{ox}. The E_{ox} accelerates the NBTI effect, i.e., the increase of E_{ox} causes a higher degradation in ΔV_T. From the calculated values of E_{ox} we observe that W_{NW}=10 nm presents an E_{ox} of ~ 2MV/cm higher than for W_{NW}=220 nm explaining the higher degradation for the narrow device obtained experimentally.



Devices		Simulated
W_{NW}=220nm | L=400nm	15.692 *	14.493
W_{NW}=10nm | L=400nm	17.048 **	14.374
W_{NW}=10nm | L=80nm	17.740 **	14.377
W_{NW}=220nm | L=400nm	15.692 *	14.493

* equation (2); ** equation (1).

Analyzing the simulated E_{ox} for W_{NW}=220 nm and L=400 nm, it is slightly higher than the other devices, explaining the small difference obtained when comparing the influence of W_{NW} on ΔV_T. The E_{ox} values also explain the small difference presented when analyzing the channel length, as the E_{ox} values for both L are very close, no influence on ΔV_T is observed.

V. Conclusions

This work presented an experimental analysis of the NBTI degradation in nanowire omega-gate p-type MOSFET, focusing in the influence of channel length and channel width and the simulations were performed to present the NBTI trend behavior, since they were not calibrated.

When W_{NW} is reduced the experimental data presented a higher NBTI degradation, which may be a result from the higher defects density in the corners of the device, resulted from the process fabrication to obtain the cylindrical structure, which becomes more pronounced for narrow devices.

The influence of channel length was also analyzed, and no significant influence was noted in the experimental devices since the gate oxide is continuous along the entire device's width (source-channel-drain) and the results obtained in simulations presented the same trend, no significant L influence.

The evaluation of the oxide electric field also supported these analyses, where when reducing W_{NW}, the electric field increases accelerating the degradation, i.e. increasing ΔV_T, being confirmed through calculation for the experimental devices and numerical simulations.

The NBTI degradation tends to be more severe in nanowire transistors than in planar devices, when considering the W_{NW}=220 nm (quasi-planar) due to acceleration of these effects because of the oxide electric field and the defect density in the corners for narrow devices, that becomes more pronounced.

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REFERENCES

[1] V. King, S. Wong, H. S. Ng, and F. Sim, "Influence of Measurement System on Negative Bias Temperature Instability Characterization : Fast BTI vs Conventional BTI vs Fast Wafer Level Reliability," vol. 10, no. 12, pp. 1460–1463, 2016.

[2] R. Russin, M. Muhamad, S. Shahabuddin, N. Soin, and M. F. Bukhori, "A Study using Two Stage NBTI Model for 32 nm high-k PMOSFET," pp. 2–3, 2013.

[3] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel, "A Two-Stage Model for Negative Bias Temperature Instability," 2009 IEEE Int. Reliab. Phys. Symp., pp. 33–44, 2009.

[4] S. Mahapatra, N. Parihar, S. Mishra, B. Fernandez, and A. Chaudhary, "A BTI analysis tool (BAT) to simulate p-MOSFET ageing under diverse experimental conditions," 2017 IEEE Electron Devices Technol. Manuf. Conf. EDTM 2017 - Proc., vol. 3, no. c, pp. 111–113, 2017.

[5] O. Prakash, S. Beniwal, S. Maheshwaram, A. Bulusu, N. Singh, and S. K. Manhas, "Compact NBTI reliability modeling in Si nanowire MOSFETs and effect in circuits," IEEE Trans. Device Mater. Reliab., vol. 17, no. 2, pp. 404–413, 2017.

[6] A. Laurent et al., "Performance & reliability of 3D architectures (πfet, Finfet, Ωfet)," IEEE Int. Reliab. Phys. Symp. Proc., vol. 2018–March, no. c, p. 6F.31-6F.36, 2018.

[7] V. C. P. Silva, G. I. Wirth, J. A. Martino, and P. G. D. Agopian, "A negative-bias-temperature-instability study on omega-gate silicon nanowire SOI pMOSFETs," in SBMicro 2019 - 34th Symposium on Microelectronics Technology and Devices, 2019.

[8] T. Grasser, Bias Temperature Instability for Devices and Circuits. New York, NY: Springer New York, 2014.

[9] Synopsys, "Sentaurus Device User Guide," Synopsys, Inc, vol. 3. Synopsys, Inc, Mountain View, CA, 2013.

[10] A. E. Islam, S. Mahapatra, S. Deora, V. D. Maheta, and M. A. Alam, "Essential aspects of Negative Bias Temperature Instability (NBTI)," in ECS Transactions, 2011, vol. 35, pp. 145–174.

[11] S. F. W. M. Hatta et al., "Negative bias temperature instability characterization and lifetime evaluations of submicron pMOSFET," ISCAIE 2017 - 2017 IEEE Symp. Comput. Appl. Ind. Electron., pp. 206–211, 2017.

[12] X. Garros et al., "New insight on the geometry dependence of BTI in 3D technologies based on experiments and modeling," Dig. Tech. Pap. - Symp. VLSI Technol., pp. T134–T135, 2017.

[13] S. Mahapatra, N. Goel, A. Chaudhary, K. Joshi, and S. Mukhopadhyay, "Characterization Methods for BTI Degradation and Associated Gate Insulator Defects," 2016, pp. 43–92.