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Study and Application of Direct RF Power Injection Methodology and Mitigation of Electromagnetic Interference in ADCs

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Orientador: Prof. Dr. Tiago R. Balen

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“Even if you have already taken a long walk, there is always a way to go.”

— Saint Augustine

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ABSTRACT

There are many publications available in literature regarding the DPI (Direct Power Injection) technique for electronic systems, but few works specifically addressed for mixed-signal converters, which are components existent in almost all electronic devices. IEC 62132-4(International Electrotechnical Commission, 2006) and 62132-1(International Electrotechnical Commission, 2006) standards describe a method for measuring immunity of integrated circuits (IC) in the presence of conducted RF disturbances. This method ensures a high degree of repeatability and correlation of immunity measurements. Knowledge of the electromagnetic immunity of an IC allows the designer to decide if the system will need external protection, and how much effort should be directed to this solution. In this context, the purpose of this work is the study and application of the DPI methodology for injection of EMI in a mixed-signal programmable device, evaluating mitigation possibilities, with special focus on the analog-to-digital converters (ADCs). The main objective is to evaluate the impact of electromagnetic interference (EMI) on different converters (two Successive Approximation Register ADCs, operating with distinct sampling rate and a Sigma-Delta ADC) of the Cypress Semiconductor Programmable SoC (System-on-Chip), PSoC 5LP. Additionally a previously proposed fault tolerance methodology, based on triplication with hardware and time diversity is tested. Results show distinct behaviors of each converter to conducted EMI. Finally, the tested tolerance technique showed to be suitable to reduce error rate of such data acquisition system operating under EMI disturbance.

Keywords: DPI – Direct Power Injection. IEC 62132-4.Programmable System-on-Chip (PSoC). Analog-to-digital converters. Electromagnetic Interference.

RESUMO

Existem muitas publicações disponíveis na literatura sobre a técnica de DPI (Direct Power Injection ou injeção direta de energia) para sistemas eletrônicos, mas poucos trabalhos direcionados para conversores de sinais mistos, que são componentes existentes em quase todos os dispositivos eletrônicos. As normas IEC 62132-4 (IEC, 2006) e 62132-1 (IEC, 2006) descrevem um método para medir a imunidade de circuitos integrados (CI) na presença de distúrbios de RF conduzidos. Este método garante um alto grau de repetibilidade e correlação das medições da imunidade. O conhecimento da imunidade eletromagnética de um CI permite que o projetista decida se o sistema precisará de proteção externa e quanto esforço deve ser direcionado para esta solução. Nesse contexto, o objetivo deste trabalho é o estudo e aplicação da metodologia DPI para injeção de interferência eletromagnética em um dispositivo programável de sinal misto, avaliando as possibilidades de mitigação, com foco especial em conversores analógico-digitais (ADCs). O principal objetivo é avaliar o impacto da interferência eletromagnética em diferentes conversores (dois ADCs baseados em aproximação sucessiva, operando com taxa de amostragem distintas e um ADC do tipo Sigma-Delta) do SoC(System-on-Chip) programável da Cypress Semiconductor, PSoC 5LP. Além disso, é testada uma metodologia de tolerância a falhas proposta anteriormente, baseada em triplicação com diversidade de hardware e temporal. Os resultados mostram comportamentos distintos de cada conversor para a interferência eletromagnética conduzida. Finalmente, a técnica de tolerância testada mostrou-se adequada para reduzir a taxa de erros desse sistema de aquisição de dados operando sob perturbação eletromagnética.

Keywords: DPI - Injeção direta de potência. IEC 62132-4. Sistema em Chip Programável (PSoC). Conversores analógico-digital. Interferência Eletromagnética.

LIST OF FIGURES

LIST OF TABLE

LIST OF ABBREVIATIONS AND ACRONYMS

ADC	Analog to Digital Converter
ABS	Antilock Brake System
AE	Auxiliary Equipment
CAGR	Compound Annual Growth Rate
CIC	Cascaded Integrator-Comb
CMOS	Complementary Metal-Oxide-Semiconductor
DAS	Data acquisition system
DAC	Digital to Analog Converter
DMA	Direct Memory Access
dB	Decibel
DNL	Differential Non-Linearity
DPI	Direct Power Injection
DSP	Digital Signal Processing (DSP)
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ENOB	Effective Number of Bits
HIS	Hospital Information System
HF	High Frequency
IC	Integrated Circuit
IEC	International Electrotechnical Commission
INL	Integral Non-Linearity
IoT	Internet of Things
ISM	Industrial, Scientific and Medical Band
LPWAN	Low Power Wide Area Networks
LSB	Least Significant Bit
MS-DTMR	Mixed-Signal DiversityTriple Modular Redundancy
MSB	Most Significant Bit
NAD	Noise and Distortion
OSR	Oversampling Ratio
PCB	Printed Circuit Board

PLD	Programmable Logic Devices
PSoC	Programmable System-on-Chip
RMS	Root Mean Square
RF	Radio Frequency
SAR	Successive Approximations Register
SFDR	Spurious Free Dynamic Range
SHA	Sample-and-Hold
SINAD	Signal Noise and Distortion
SNR	Signal-to-Noise-Ratio
SoC	System-on-Chip
THD	Total Harmonic Distortion
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
UDB	Universal Digital Blocks
VDDA	Analog Power
VREF	Reference Voltage
ΣΔ ADC	Sigma-Delta Analog to Digital Converter

CONTENTS

1. INTRODUCTION

The electromagnetic interference (EMI) in electronic equipment has become more notable as technology evolves. People see with enthusiasm the evolution of electronic devices, mainly the wireless devices, but, unfortunately, the consequences of the pollution of frequency spectrum to the environment we live are not always considered.

The increasing use of electronic products leads this market to be fierce in terms of competitiveness, mainly for price and time-to-market constraints. This pressure often reflects in the work of system designers who are daily challenged to create innovative products that must cost less than the competitors, often within a tight schedule. However, for low cost products it is common some stages of the project to be skipped, such as functional tests that could recreate the actual use of the product in the field.

Along with the increasing demand for innovative electronic systems, a concern, that until then had not been considered so important, raised. However, it attracted more attention after the occurrence of a series of situations that brought risk of accidents to society as a whole. For example, during the early years of Antilock Brake System (ABS), Mercedes-Benz automobiles equipped with ABS had severe braking problems along a certain stretch of the German autobahn. The brakes where affected by a nearby radio transmitter as drivers applied them on the curved section of highway. The near term solution was to BUILD a mesh screen along the roadway to attenuate the EMI. This enabled the brakes to function properly when drivers applied them (NASA, 1995).

Thus, electromagnetic interference (EMI), which is a disturbance of electromagnetic origin that may cause performance degradation or affect the normal operation of a component, device and electronic systems, is being considered more often nowadays. EMI considers all the problems concerning the transfer of electromagnetic energy.

The interference may be intentional or accidental and may be of natural or artificial origin. According to Waes (2017), the earth's magnetic field is of natural origin and can cause interference in power systems by the influence of its force. Atmospheric discharges and winds are examples of natural causes of EMI.

The cost of maintaining an engineering area capable of dealing with electromagnetic interference issues is very high to some companies. This deficiency often causes unknown problems in products developed and commercialized by the company. This way, EMI may be

not properly treated due to the difficulties of solving the problem. As in many situations, especially in underdeveloped countries, electromagnetic interference is usually only dealt with when it arises and causes some damage, making the system more complex and more costly than if it had been planned at the beginning of the project. Nowadays a big challenge consist in to improve design methodologies and develop modeling techniques capable of providing simulations of circuit performance under EMI (JOVIC, 2010).

Another concept which will be addressed is Electromagnetic Compatibility (EMC), which is the ability of electronic equipment to function properly while immersed in an electromagnetic environment (IEC, 2016). The main topics of electromagnetic interference subject are: causes, effects and mitigation. The compatibility between electronic circuits should be achieved. Thus, an electronic system must work without impairing the operation of other devices, nor should it stop operating when installed/exposed to electromagnetic environments.

The motivation for study and research on EMI / EMC topicsis due to the limited knowledge and application of this topic in Brazil, the complexity of EMI understanding and, mainly, the demand for knowledge in this area.

In Brazil, there is no imposition for compliance with EMC standards for general-purpose electronic products, although the recommendations presented by the International Electro technical Commission (IEC) serve as a reference. Nowadays, there is no comprehensive EMC / EMI standardization, the correct operation of electronic systems is very vulnerable to problems of electromagnetic interference due to the system topology itself, its interconnection cables and the configuration of the grounding system. Thus, the correct functioning of electrical and electronic products is compromised by the installation of new equipment in the vicinity, by the appearance of accidental connections, by the degradation of existing installations, among other factors. However, the National Telecommunications Agency (ANATEL), through Resolution No. 715 - Regulations for Conformity Assessment and Homologation of Telecommunications Products (ANATEL, 2019) now requires all national telecommunication equipment manufacturers to be compliant with specific EMC requirements - which reflect the technical specifications of the 2014/30/EU EMC Directive (COUNCIL OF EUROPEAN UNION, 2014). EMC requirements for biomedical equipment are also being adopted in Brazil, which (also) reflect the technical specifications of the EMC Directive.

The miniaturization of the electronic components is directly connected with technological innovation. Undoubtedly, electronic circuits became smaller while the systems

became more reliable. In this way, some areas such as medical equipment, automotive, and aerospace, for example, have taken advantage of this. One can imagine a cell phone in the 2000s and compare it to a mobile phone these days, the difference in size, functionality and cost is considerable. In this case, the processors have become faster, smaller and cheaper. This had been possible by the evolution in the microelectronics manufacturing process that allowed the transistors to become smaller and faster.

Reducing the size of the transistors increases the variability and consequently the probability of defects in nanoelectronic devices that, consequently, are more susceptible to environmental phenomena (CHENET, 2015). Thus, characterization of the susceptibility of integrated circuits (ICs) for electromagnetic disturbances is receiving special attention. This trend leads to the need for standardized measurement procedures that allow a comparative evaluation and analysis between different devices. The increasing technical development, on the other hand, has the consequence of increasing the complexity of the design of such systems, thus raising concerns regarding its reliability, performance and safety, especially with regard to its electromagnetic compatibility. It has become vital to prevent critical systems from malfunctioning because the consequences of these can be catastrophic. A possible way to overcome this problem is to use fault tolerance techniques in the design of such systems PRESTES, 2010).

The current study considers a previously proposed (by Chenet (2015))fault tolerance technique which is based on Triple Modular Redundancy (TMR) with diversity (DTMR) implementing a data acquisition system (DAS), prototyped in a PSoC. The objectives are, firstly, to evaluate the behavior of different architectures of data converters in the face of direct radio frequency (RF) power injection in their reference voltage and supply pins, and then to evaluate the effectiveness of the studied DTRM technique to mitigate EMI effects in this system.

Another important point considered for this study is that, today, most of the signal processing performed in electronic systems is digital, and the performance of the analog-to-digital converters (ADCs) present at the borders of the digital domain become very important (RAPUANO, 2005). To benefit from the Digital Signal Processing (DSP) advantages, an analog signal must be converted to a digital format, a task that is performed by an Analog-to-Digital Converter (A/D converter or ADC). The reverse procedure, that is, conversion from digital to analog domains, is performed by a Digital-to-Analog Converter (D/A Converter or DAC) (DORNELAS, 2018). Analog-to-Digital Converters (ADCs) are used in electronic

systems applied in large-scale to control, instrumentation and communication tasks that comprise mixed-signal interfaces.

In this work the Triple Modular Redundancy (TMR), a system-level fault tolerance technique, is considered. TMR and diversity are mainly used in critical applications where an error can result in harm for life or loss of high investment (CHENET, 2015).Throughout this textthe results of the impact of electromagnetic interference (EMI) on the three different converters of the Cypress Programmable SoC PSoC 5LP (CYPRESS SEMICONDUCTOR, 2013) is presented along with a discussion regarding the application of the methodology of redundancy with hardware diversity and its effectiveness to mitigate this type of interference in mixed-signal systems. Mainly, the standards IECs 62132-4(IEC, 2006) and 62132-1(IEC, 2006b) were followed to apply the Direct Power Injection (DPI) test to the PSoC device.

Therefore, this work contributes to the evaluation of the tolerance level and reliability of the converters and the voting system by injecting fault directly into the data converters. The main results show that the ΣΔ ADC is more susceptible, in part due to its complex working principle and topology. Additionally, the applied tolerance technique is suitable to reduce the error rate of the overall system, as demonstrated in the rest of this text.

2. ELECTROMAGNETIC INTERFERENCE IN ELECTRONIC SYSTEMS

At this moment, it is essential to understand some concepts about electromagnetic interference and how it happens. For the development of this research, it is also important a brief knowledge about the history of electromagnetic disturbances, as well as where the studies in this area are directed to. First of all, in order to better exemplify the possible effects, some interesting cases involving EMI will be presented.

2.1 Basic concepts

Electromagnetic Interference is degradation in the performance of equipment or transmission channel or a system caused by an electromagnetic disturbance. It can be generated by spark-ignition in motor brushes, power circuit switching, inductive and resistive charge drives, relay drives, switches, circuit breakers, fluorescent lamps, heaters, automotive ignitions, atmospheric discharges and even electrostatic discharges between people and equipment, microwave equipment and mobile communication equipment. All of them can result in overvoltage, under voltage, surges, transients and other types of noise and interference (LAVARDA et al 2015).

The growing need for equipment to operate with different communication protocols, along with inadequate installations, allows the generation and emission of electromagnetic interference.

The occurrence of these disturbances is very common in industries and factories, where EMI is very frequent due to the greater use of machines and motors that generate transients in the electrical network. The biggest problem caused by EMI is the sporadic situations that gradually degrade the equipment and its components. According to Hanada et al. (2018), several problems can be generated by EMI, for example - in electronic equipment - we may have failures in communication between devices of network and/or computers, alarms generated without explanation, acting in relays that do not follow a logic and without command for this and, burnout of components and electronic circuits, among other effects. The presence of noise in the power supply is very common due to design errors in determining equipment and board grounding (FRÉMONT et al, 2012).

In general, at high frequencies, wires and PCB (Printed Circuit Board)paths are even closer to the behavior of an antenna, which helps us to understand why EMI emission

problems are aggravating in networks that operate at high speeds (PRESTES, 2010). Any electronic circuit is capable of generating some kind of magnetic field around it and its effect will depend on its amplitude and duration. Another typical example of how EMI can affect the behavior of an electronic component is a capacitor that is subject to a voltage peak higher than its specified nominal voltage (MANDRUCCOLO et al. 2010). It can cause the dielectric degradation (the thickness of the dielectric is limited by the capacitor's operating voltage, which must produce a potential gradient higher than the dielectric strength of the material), causing a malfunction and, in some cases, the burnout of the capacitor. Static electricity is an electrical charge in equilibrium that is generated primarily by the imbalance of electrons located under a surface or in the air of the environment. This imbalance of electrons thus generates an electric field that is capable of influencing other objects that are within a given distance. The charge level is affected by the type of material, contact speed and separation of the devices. When a not grounded object is electrostatically charged, an electric field associated with this charge is created around it and if an electronic device gets exposed to this field, electrostatic induction may occur. This can cause transfer of charges between the devices, which may result in a reduction of lifetime of the equipment, or even instantaneously damage it(CHENET et al. 2015).

2.2 EMI/EMC history, trends and mitigation

Michael Faraday, near1843, demonstrated a zero electric field inside an electrified conductive surface. According to this experiment, the charges distribute homogeneously on the outside of this surface. This effect received the name of Faraday's Cage (MARCO, 2018). The German mathematician Carl Friedrich Gauss established the relation between the flows of the electric field through a closed surface with the electric charge that exists within the volume bounded by this surface, this is the principle of the electrostatic machine that was invented by the engineer Robert Jemison van de Graaff, around 1929 (MARCO, 2018). The knowledge of these effects has brought the possibility of preventing many problems caused by electromagnetic interference in several areas. In the case of vehicular applications, for example the meshes in electrical cables are responsible for shielding the transmission of important signals for the operation of the car.

The first known cases of electromagnetic interference occurred around 1930 in electric motors and electric railroads (PAUL, 2006). By 1950, the problem intensified with the emergence of the bipolar transistor, worsening between the 1960s and 1980s with the

invention of the integrated circuit and the microprocessor (PAUL, 2006). Thus, between 1960 and 1980, the main way to deal with EMI and power line transients issues was through grounding. In the 1970's, studies started to address PCB layout issues, in order to mitigate the effects of EMI in electronic equipment. However, the advances in this area were still very fast and even when a problem was solved, new equipment appeared in the market showing increased susceptibility to electromagnetic interference. Thus, in 1990 the studies began at the level of integrated circuit (MARDIGUIAN, 2004).

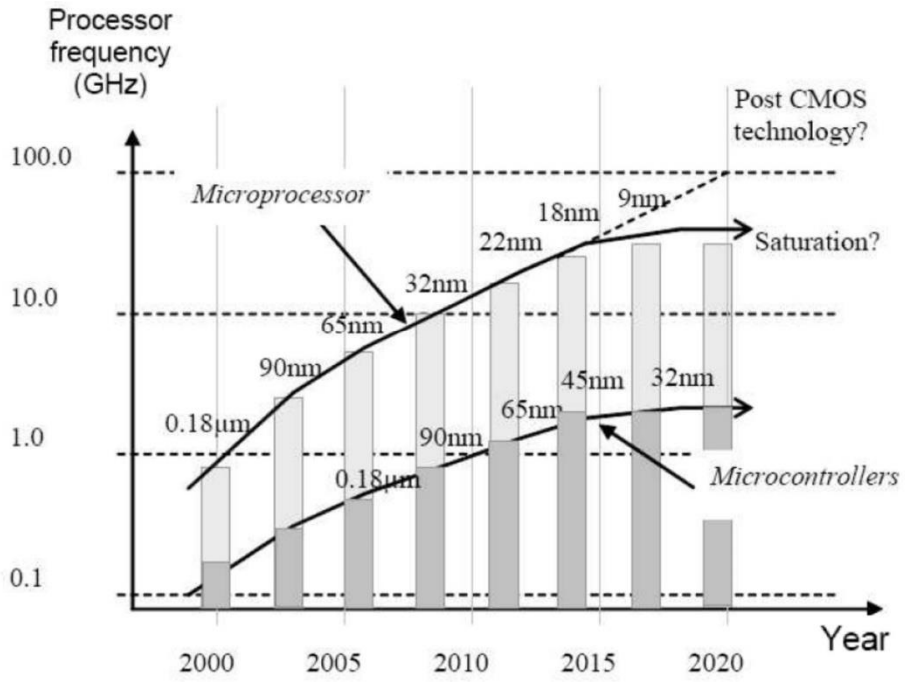
Some companies are highly concerned with EMI, as, for example, the automotive industry. With the arrival of autonomous vehicles, smart cities and as cars become more connected, sensors and other devices that emit EM signals will become increasingly present.

In the 2012 edition of IEEE International Symposium on Electromagnetic Compatibility the main theme was "trends in EMC engineering". Among the most discussed topic was the automotive industry, loss and absorbing materials, nanotechnology, high data rates and EMC rule checker software.

For Kruczkowski (2012), the automotive industry is in a period of aggressive innovation, adding modern features like Wi-Fi and radar. All of these emitters, combined with external interferers like cell towers, hot spots, and other vehicles, are potential sources of EMI to the processor-based systems that control all aspects of vehicle operation. In respect to materials science breakthroughs and how such advances can affect their area of expertise, composite materials with nanoparticles, nanotubes, or nanofiber for gaskets and shielding screens have already shown promissory. Nanowires have the potential to someday replace copper in high-density, high-speed interconnects; however, suitable approaches to signal integrity simulation and modeling are a necessity to avoid EMI when using such materials. Signal integrity has become a major concern for engineers because the demand for high-speed data transmission is greater.

Miniaturization of transistors is very important for processor size reduction. This is why manufacturers are in a growing race to reduce the manufacturing size of their components. As already discussed, this miniaturization can have implications for EMC, mainly because the power supply reduction and frequency increase usually occur together with feature size reduction in technology scaling of integrated circuits. According to Jovic (2010), the time line of ICs performance is consistently rising, as can see observed in Figure 2.1.

Figure 2.1–Microprocessor evolution



Source: JOVIC (2010, p. 01).

The EMC industry is increasing relying on software simulation. With the speed in which new technologies emerge, the demand for EMI robust systems has increased very fast. The creation of standards, development of measurement and monitoring equipment and qualification of people has not accompanied the increasing diversity of characteristics in this area. Thus, development and use of software for simulation of EMI/EMC, is becoming an effective alternative to deal with this problem.

In relation to integrated circuits, it is important to consider that, internally, they have a thin layer of metal. In this frame are attached the semiconductor in the package process. Even though the lead frame is the largest component in an integrated circuit, at frequencies below 1 GHz, its presence is not considered as an antenna for receiving unwanted RF signals.

It is the cable harness and/or the traces of a printed circuit board which constitute efficient antennas. Thus, an IC receives the unwanted RF energy through the pins connected to the wires of such cables. Because of this, the electromagnetic immunity of an IC can be characterized by conducted RF disturbances (i.e. RF forward power) instead of field parameters as is usually the case in module and/or system testing (IEC 62132-4, 2006).

2.2.1 Market Forecast concerning EMC

Due to the importance and complexity of the subject, there are studies presenting detailed forecasts on investments that should be made in the area of EMC for the coming years. According to Global Market Insights(2017) EMI shielding materials market size should grow at a moderate rate from 2017 to 2024. The factors that are driving the EMI industry are increasing telecommunications infrastructure worldwide, increasing use of electronic devices in automobiles and tremendous growth of mobile wireless communications that is resulting in the need to shielding electronic equipment from interference by unwanted radio frequencies.

New generations of integrated electronic circuits with stacked & multi-chip package structures are more susceptible to interference that, besides affect performance of circuits, may also lead to data loss(JOVIC, 2010). The shielding market must be boosted by the EMI regulations. The area of defense/military has been important for the development of research of new technologies and, this should continue to happen in the coming years due to growing political and economic instability in many regions of the world. The aerospace industry is expected to continue growing and this includes space exploration. There is a forecast that 30,000 new passenger aircrafts will be needed in the next 20 years. Based on a survey conducted by the website Research and Market (2015), electromagnetic compatibility shielding market was valued at USD 3.51 billion in 2014 and estimated to grow at a CAGR (Compound Annual Growth Rate) of 6.09% during the forecast period of 2015-2020.

This shielding market can be divided according to the application: aerospace, automotive, defense and electronics. Different applications require distinct material. The main type of material includes aluminum, brass, nickel, silver, stainless steel, conductive carbon/graphite composites, metalized plastics and others.

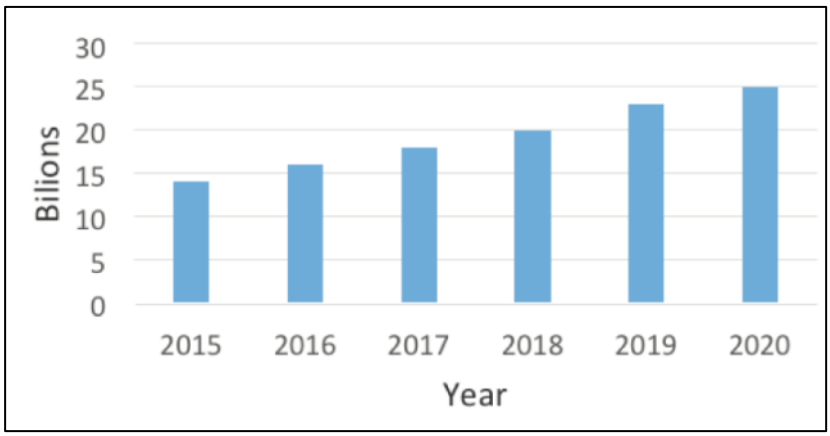
The automotive market must be one of the main propellant for EMC concern. With the advent of self-driven cars, several new devices must be released, as well many other communication and safety standards.

2.2.2EMI on IoT systems

The interconnecting of physical devices embedded with electronics, sensors and network connectivity is called Internet of Things (IoT). According to Wiklundh (2017) and Stenumgaard (2017) the wireless part of global Internet traffic is expected to grow from approximately 50% today, to about 75% in 2020, and the first 5G products are expected to be

available in 2020. By 2025, the Internet of Things is projected to have an $11 trillion impact on companies all around the world (WAES, VANKEIRSBILCK, PISSOORT and BOYDENS, 2017).

Figure 2.2– Global number of connected devices



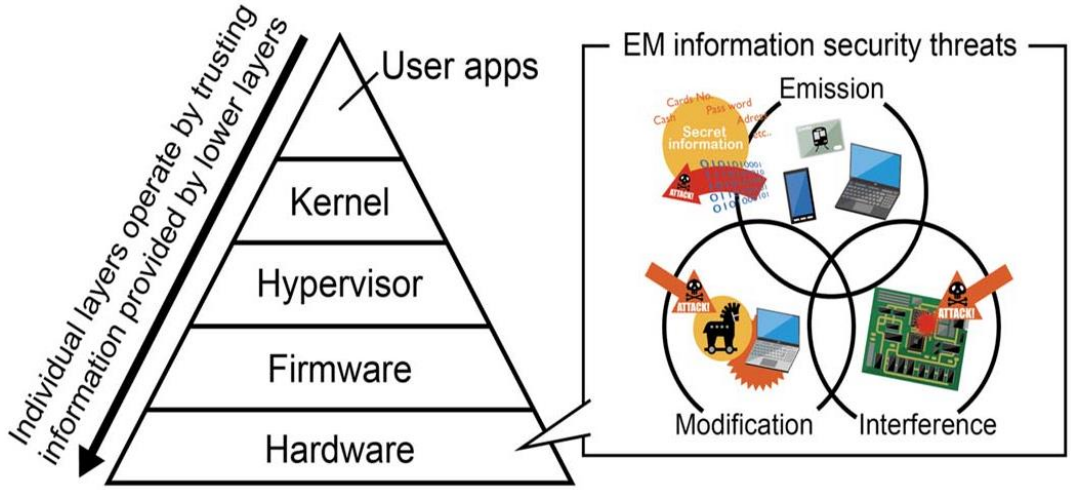
Source: WIKLUNDH and STENUMGAARD (2017, p 01).

New services are being created, and using data gathered using devices like smart meters and surveillance cameras. These data are uploaded to servers through communication networks.

Another important area to be considered include medical field. For example, the medical telemetry systems used in hospitals can continuously acquire vital signs and transmit them to a staff station or administrative area. At a terminal in a staff station, staff members can observe multiple patients at the same time. A medical telemetry system connected to a hospital information system (HIS) is an example of critical IoT system (HANADA AND KUDOU, 2018).

For Hayashi, Verbauwhede and Radasky (2018), IoT systems, may be divided in, at least, two layers. The upper layer – software – and lower layer – hardware. Thereby, to ensure reliability in IoT services it is very important to ensure that the hardware has a correct operation, because, in this layer, the data are gathered and transmitted. Figure 2.3 shows a system where each layer consists of terminals that operate by trusting the information coming from the layer below them. According to Waes et al. (2017), effects of EMI are observed in both hardware and software. In hardware, the effects of EMI can result in noise accumulating on traces and leading to false readings on inputs or distortion on outputs. As a result, software effects, such as jumps in the program execution and data corruption can be witnessed.

Figure 2.3 – Trust model and EM information security threats



Source: HAYASHI, VERBAUWHEDE and HADASKY (2018, p 01).

As already mentioned, automotive applications are continuously increasing complexity. Until 2025 it is expected that each car has more than one hundred microcontrollers with different functions.

More and more, those microcontrollers are used in a safety-critical environment, where a failure might result in injury, and in the worst case, even human deaths (WAES, VANKEIRSBILCK, PISSOORT and BOYDENS, 2017).

According to Fuqaha (2015, apud Dornelas 2018), the overall concept of the IoT is a network in which every domain-specific application is interacting with domain-independent services, whereas in each domain, sensors and actuators communicate directly with each other. In figure 2.4, some examples of this interconnectivity are depicted.

Figure 2.4 – Examples of applications on the IoT market

Source: AL-FUQAHA et al., (2015, apud DORNELAS, 2018, p 16).

Sources of Electromagnetic Interference in IoT Environment: Even though electronic products designed to operate in IoT environment are planned to comply with lower bands of the electromagnetic spectrum, the operating frequency, in some cases, may be particularly high. Some applications may operate up to 30 GHz (outdoor) and up to 90 GHz (indoor) WIKLUNDH et al. 2017. Nowadays, the majority EMI susceptibility tests are considering the frequencies up to 18 GHz. Therefore, it is possible to infer that, in the future, devices may suffer EMI from sources which are not considered in current compliance tests. Thus, for a wide range of new frequencies, both emission and immunity properties will be unknown. Furthermore, instruments and equipment for EMC testing will have to be further developed and modified to cope with the large extension of frequency bands (WIKLUNDH and STENUMGAARD, 2017).

The trend is that low power devices and components will dominate in IoT applications. For Wiklundh and Stenumgaard (2017), low power devices usually show lower signal-to-noise ratio (SNR) for the wireless connections. This means larger sensitivity to electromagnetic interference.

For medical applications, caution with distortions in electrical signals should be even greater as devices work by collecting and analyzing low amplitude signals. Considering the accuracy of medical application, some structural care should be observed, such as equipment installation location and the communication standards in which they operate. Wiklundh and Stenumgaard (2017) expose a great example: microwave therapy equipment and some heaters emit electromagnetic noise in the same frequency band as the ISM (Industry, Scientific and Medical) band, which is often used in the communication infrastructure of IoT. Although not specifically a medical device, microwave ovens are often installed in hospital wards. Careful planning of the location of the microwave equipment and careful installation of the IoT system can minimize the electromagnetic effect. In addition, IoT communication utilizes a wide variety of communication standards that must be taking in to account as a potential polluter of the EM spectrum. Currently, standards such as ZigBee, Bluetooth, IEEE802.11 series, and wireless LAN are used in the same environment. This all greatly increases the probability of EMC problems affecting the functioning of medical devices.

According to Hayashi, Verbauwhede and Radasky (2018) in IoT systems the electromagnetic vulnerability maybe divided in three categories:

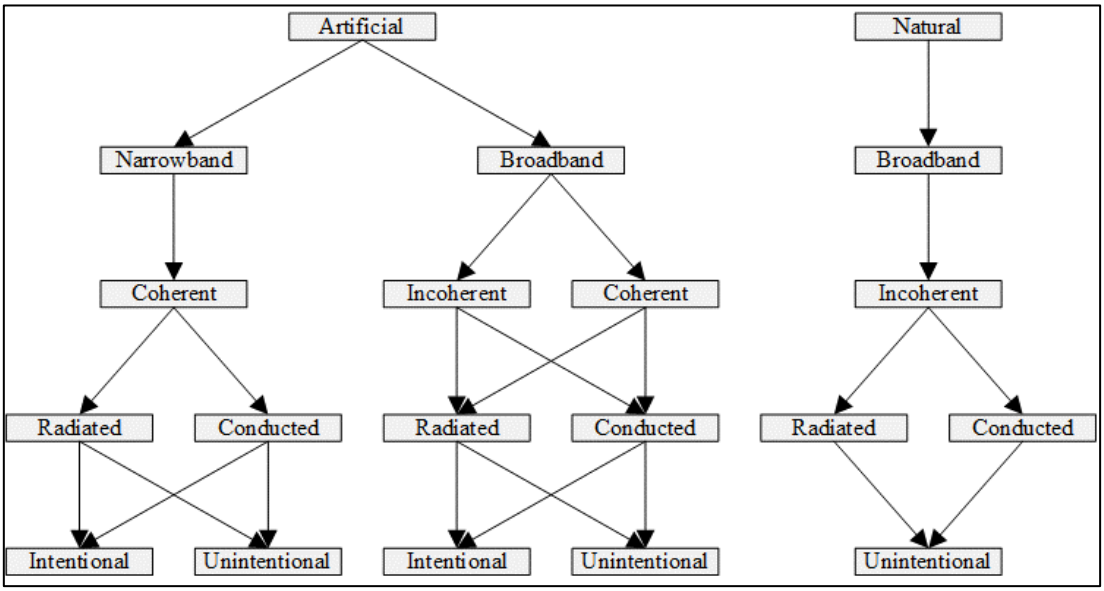
Electromagnetic interference induced from devices operation– non intentional: It happens when the electronic devices are processing data, in normal operation. Electromagnetic interference is attributed to the radiated electromagnetic waves that vary with time according to data.

Intentional electromagnetic interference: Intentional electromagnetic interference is a threat that disables information and communication equipment by stopping functionality. This threat was usually carried out by military organizations. However, as time goes by, access to ordinary citizens is becoming possible.

Intentional Modification of electronic circuits: There are a lot of reasons that brings some manufacturers to make modifications on products. Amongst them is the cost reduction, which may bring loss of quality, potentially, turning the electronic devices more susceptible to EMI.

In the same way, Waes et al. (2017) classifies the electromagnetic interference in five categories according to the sources. The classification is shown in the figure 2.5.

Figure 2.5 – EMI Source Classification



Source: WAES, VANKEIRSBILCK, PISSORT AND BOYDENS (2018, p 02).

Artificial EMI is originating from manmade devices and infrastructure. Lightning on the other hand, is an example of natural EMI. Another classification considers the bandwidth of interfering signal: narrowband or broadband EMI. Broadband disruptions have a greater frequency range than the bandwidth of the device subjected to EMI. Electromagnetic disturbs can be also classified as coherent or incoherent: coherent EMI is defined as signals with a well-defined relationship between amplitude, frequency and phase. Regarding the propagating media, EMI can be considered as conducted or radiated: conducted EMI propagates through electrical conducting paths such as grounding planes or wires. All non-conductive EMI is classified as radiated. Finally, the last category considers whether or not the device is transmitting intentionally. Intentional radiating devices are emitting devices whose primary function is dependent on radiated emitters, such as communication, navigation and radar systems. Natural EMI events are by definition classified as unintentional. Restricted radiating devices only access the electromagnetic spectrum for a limited time, such as garages opening systems and wireless microphones.

2.3 EMI in Data Converters

Previous research has been conducted into determining the susceptibility of analog voltage comparators (FIORI, 2012) and flash ADCs (KENNEDY, 2018) to EMI. According to Fiori (2012) when the input signals contain EMI and can cause false switching of the

output. It was observed that this effect was due to rectification of the EMI signal performed by non-linear devices causing unwanted perturbation of operating points of the transistors. This reflects in erroneous decision of bits during comparison leading to bit errors at the converter output.

MUSUMECI (2009) discusses if RFI can affect the ΣΔ ADC operation, once the anti-aliasing filter could mitigate it. However, it is concluded that the ΣΔ ADC operation can also be affected by substrate interference, which derives from digital core switching.

Kennedy (2018) presents some information about previous tests carried out on the internal structure of ADCs. For example, tests carried out on the analog voltage comparator showed that this block may be susceptible to EMI. The sample and hold phase uses a capacitor and a switche at the ADC inputs to sample and maintain the input voltage. Because of that, distortion caused by MOS switches due to the injected EMI has been investigated. Kennedy (2018) also comments about bulk CMOS processes suffering from substrate noise coupling due to the common substrate connection across the die. Undesirable responses in the circuit can be caused from EMI injected into the IC and propagated by the substrate.

Fiori (2012) addresses the topic of susceptibility of CMOS voltage comparators for radio frequency interference, in which some studies and tests were carried out on false commutations induced by the disturbances superimposed onto the nominal input signals. Fiori concluded that the RFI distortion occurs mainly at the comparator input stage, causing the comparator limit to change. Probably with this, the result of an AD conversion can be affected.

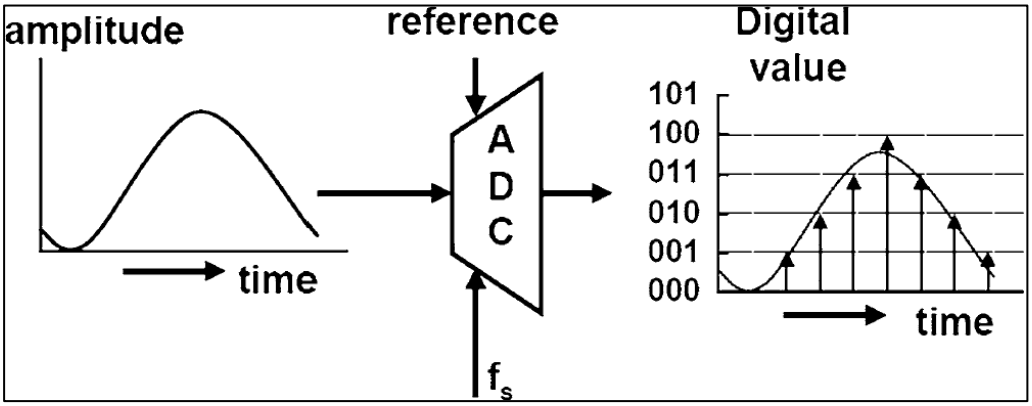
Kennedy (2018) focused his studies to verify the susceptibility of flash ADCs to electromagnetic interference concluding that supply port is immune to interference but the analog input and reference voltage input ports are susceptible to injected EMI.

3. ANALOG-TO-DIGITAL CONVERTERS

An analog signal is continuous in time, with continuous variations of its amplitude. The physical quantities such as velocity, pressure, temperature, electric current and voltage, are examples where analog variations occur. The analog-to-digital (ADC) conversion of signals is applied in control, instrumentation and communication systems, including those used in critical applications. AD and DA converters, depending on the needs of the system, perform the interface between the analog and digital world (AGUILERA, 2018).

Several errors may be introduced by sampling and quantization process that occurs in the task of converting an input analog signal. Additionally, the quantized and sampled signal is only meaningful when a relationship exists between the digital number range considered and a physical reference value (DORNELAS, 2018). Figure 3.1 shows the function involved in the conversion process, where an A / D converter transforms an analog signal, continuous in time, into a sampled signal, discrete in time, quantized within a finite number of integer values, determined by the characteristic resolution of the converter in bits.

Figure 3.1 – Functions of the A/D Converter: sampling in time, quantizing in amplitude and linking to a reference



Source: PELGROM (2010, p. 02).

Next subsections present the important characteristics and terminologies regarding ADCs, which are the main devices studied in this work.

3.1 ADC Parameters and Characteristics

Some parameters are responsible for determine the performance and output accuracy of the ADC. Characteristics such as Signal-to-Noise-Ratio (SNR), Total Harmonic Distortion (THD), Signal to Noise and Distortion (SINAD), and Effective Number of Bits (ENOB) are explained below.

Reference Voltage (VREF): It is a standard voltage provided through external supply or generated from de ADC module. VREF is used such an indicator for Analog Input Voltage. The range of VREF varies among different devices and the respective device datasheet must be referred to know the exact or allowed values (ATMEL, 2016).

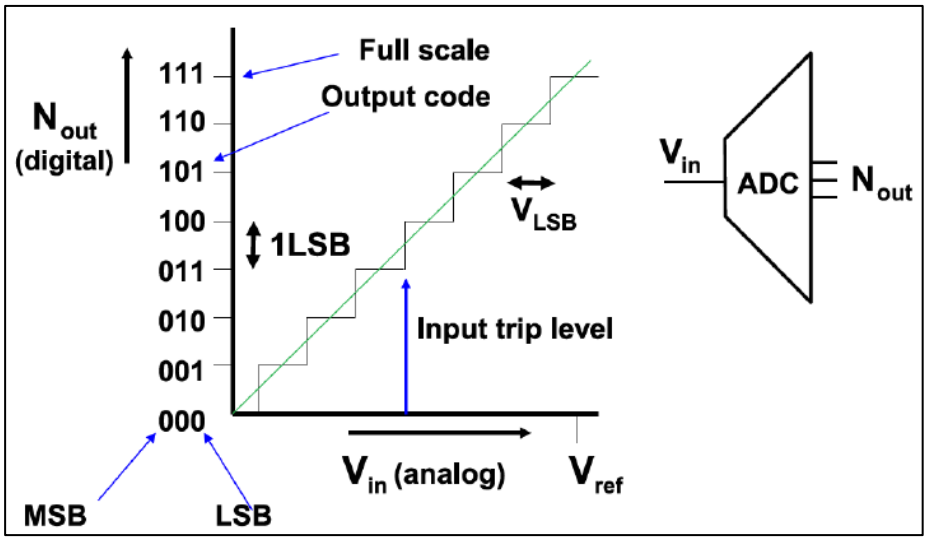
Resolution: it is the number of bits per conversion cycle that the converter is capable of processing. The resolution of an A/D converter (ADC) is specified in bits and determines how many distinct output codes (2^n) the converter is capable of producing. Analog equivalent resolution is the smallest voltage increment corresponding to a 1 LSB (Least Significant Bit)change. This ADC specification determines the smallest analog input signal an ADC can resolve.

Sampling Rate and Bandwidth: The converter input receives the analog signal in continuous time and the ADC module needs to convert it to discrete digital values. These digital values are sampled from the analog signal. Sampling rate is defined as the number of samples acquired in one second (ATMEL, 2016). The maximum frequency supplied to the ADC of the input analog signal is the bandwidth. Nyquist theorem guides sampling rate and bandwidth parameters. According to this theorem, the sampling rate must be at least twice the bandwidth of the input signal (ATMEL, 2016).

Quantization: In A/D Converters, the quantization process is performed after sampling and is also known as rounding (DORNELAS, 2018). Quantization is the process where the sampled analog input voltage will be replaced with an approximation from a finite set of discrete values (ATMEL, 2016). The converter dynamic range is divided into (ideally) equally-spaced quantized levels, each represented by analog amplitude (DORNELAS, 2018). The digital representation is done in binary numbers. The quantization level is a power of 2, $2^{N.}$ The letter N represents the number of bits or resolution of the converter. Figure 3.2 shows

the most significant bit (MSB) and the least significant bit (LSB) in a quantization process. According to Pelgrom (2010), the Full Scale (FS) of the converter corresponds to the available analog dynamic range, Vrefp − Vrefn (typically Vrefn = 0).

Figure 3.2– Quantization process – MSB and LSB.



Source: PELGROM (2010, p. 175).

3.2 Dynamic and Static Parameters

The basic purpose of an ADC is to transform an analog signal into an equivalent digital value. Characterization techniques of an analog–to-digital converter intend to achieve static and dynamic behavior of converters (FLORES, 2003; IEEE, 2010). Below, the main parameters for static and dynamic characterization of converters are detailed.

Static Parameters: Static errors are evaluated from the characteristic curve of the converter. This curve depends on its response to a ramp that goes through its entire scale (FLORES, 2003). The transfer function of the ADC is given by an N-bit line, and its actual characteristic curve will be formed by a uniform 2^N levels.

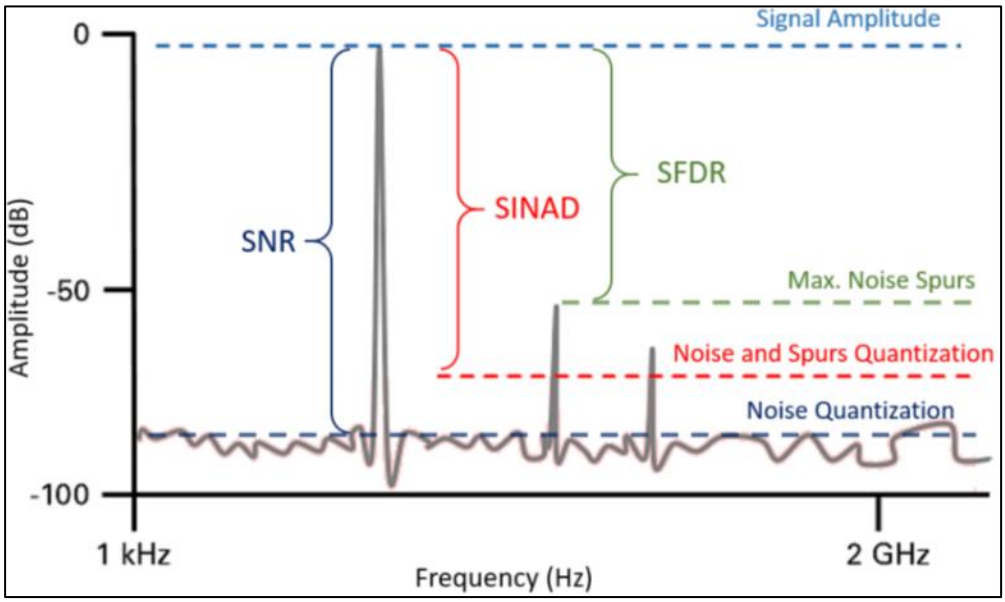
Differential Non-Linearity (DNL): This parameter describes the deviation between two analog values corresponding to digital input values. A DNL error specification less or equal than 1 LSB ensures a monotonic transfer function without missing codes (AGUILERA,

2018). Non-linearity produces quantization steps with varying widths. For the case of a perfect ADC, the step width must be 1LSB. However, an ADC with DNL shows step widths which are not exactly 1LSB (ATMEL, 2016).

Integral Non-Linearity (INL): Integral non-linearity (INL) is defined as the maximum vertical difference between the actual and the ideal curve. It indicates the amount of deviation of the actual curve from the ideal transfer curve (ATMEL, 2016). INL can be interpreted as a sum of DNLs.

Dynamic Parameters: Dynamic errors are errors that occur when the signal is varying (RAPUNO, 2005) and may be associated to the above mentioned non-linearities. Dynamic parameters are used for ADC characterization and can be obtained with a sine excitation with known amplitude and phase, and evaluated the obtained spectrum of the converted signal (FLORES, 2003). In figure 3.3, some of the dynamic parameters ADCs may be observed. The following text will detail the dynamic parameters, such as Signal-to-Noise-Ratio (SNR), Total Harmonic Distortion (THD), Signal Noise and Distortion Ratio (SINAD), and Effective Number of Bits (ENOB).

Figure 3.3 – Common dynamic metrics: SNR, SINAD and SFDR.



Source: DORNELAS (2018, p. 32).

Signal to Noise Ratio (SNR): SNR is defined as the ratio of the output signal voltage level to the output noise level (ATMEL, 2016). It is possible to calculate SNR (dB) using this formula:

$$SNR(dB) = 20\log\left(\frac{V_{RMS(Signal)}}{V_{RMS(Noise)}}\right) \quad (3.1)$$

In an ideal analog-to-digital converter the quantization error is distributed between −1/2 LSB and +1/2 LSB, and the Signal-to-quantization-noise ratio (SQNR) is calculated using this formula:

$$SNR=6.02N+1.76dB \quad (3.2)$$

The higher the value of SNR (dB), the better will be the performance of ADC.

Signal-to-Noise and Distortion Ratio (SINAD): Signal to noise and distortion (SINAD) is a combination of SNR and THD parameters (ATMEL, 2016). For Maloberti (2010, apud Aguilera 2018), SINAD is the relationship between the fundamental frequency and the frequency integration of all harmonic content obtained by spectral analysis of the converted signal, excluding the fundamental itself and the DC level. SINAD can be calculated with SNR and THD by:

$$SINAD = 10\log 10\left[10^{\frac{SNR}{10}} + 10^{\frac{THD}{10}}\right] \quad (3.3)$$

The higher the value of SINAD, the better will be the performance of ADC.

Total Harmonic Distortion (THD): When a sine wave is applied to a nonlinear ADC, the digitized output will contain harmonics of the input signal. The total harmonic distortion (THD) is the ratio, in percent or decibel, of the Root Mean Square (RMS) value of the harmonics to the RMS value of the component of the output signal at the input signal frequency (RAPUNO, 2005), considering a pure sine wave as input. The THD is a good metric for evaluating the correct functionality of data converters. This parameter is also correlated with DNL and INL. The THD is calculated in dB or as a percentage value (MALOBERTI, 2007; IEEE, 2010):

$$THD_{\%=}\left(\frac{\sqrt{V_2^2+V_3^2+\cdots V_N^2}}{V1}\right) X\ 100\% \quad (3.4)$$

To achieve better performance, the THD value of an ADC should be as low as possible (ATMEL, 2016)

Effective Number of Bits (ENOB): The effective number of bits (ENOB) is a measure of accuracy and expresses the total of noise and distortion(NAD) relative to the full scale of the ADC. ENOB is another way of representing the signal to noise ratio and distortion (SINAD), in units of bits, and can be derived from the following formula (ATMEL, 2016):

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (3.5)$$

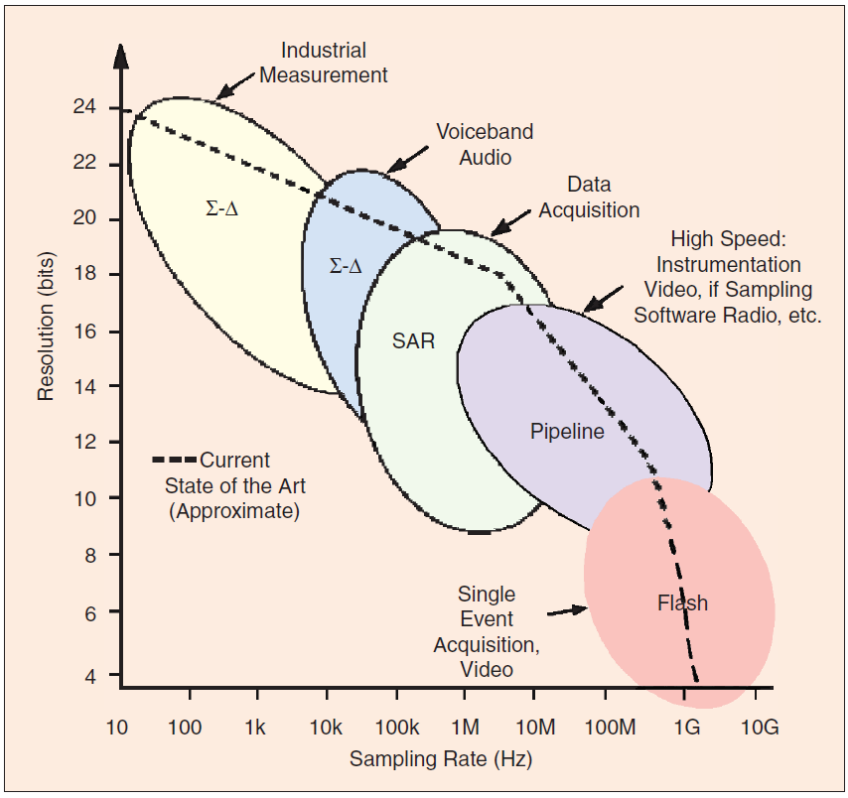
Ideally, the ENOB value should be as close as possible to the resolution of the ADC.

Spurious Free Dynamic Range (SFDR): is the ratio of the root-mean-square signal amplitude to the root-mean-square value of the highest spurious spectral component in the first Nyquist zone (MALOBERTI, 2007). The SFDR is important for communication systems.

3.3 ADC Architectures

For Rapuano *et al* (2005), the ADC application can be characterized by five main market requirements - data acquisition, precision industrial measurement, voice band and audio, high speed and communication systems. Figure 3.4 shows the performance (resolution and sampling rate) related to different ADC architectures demanded for different applications.

Figure 3.4– ADC architectures, applications, resolution and sampling rates.



Source: RAPUANO *et al* (2005, p. 02).

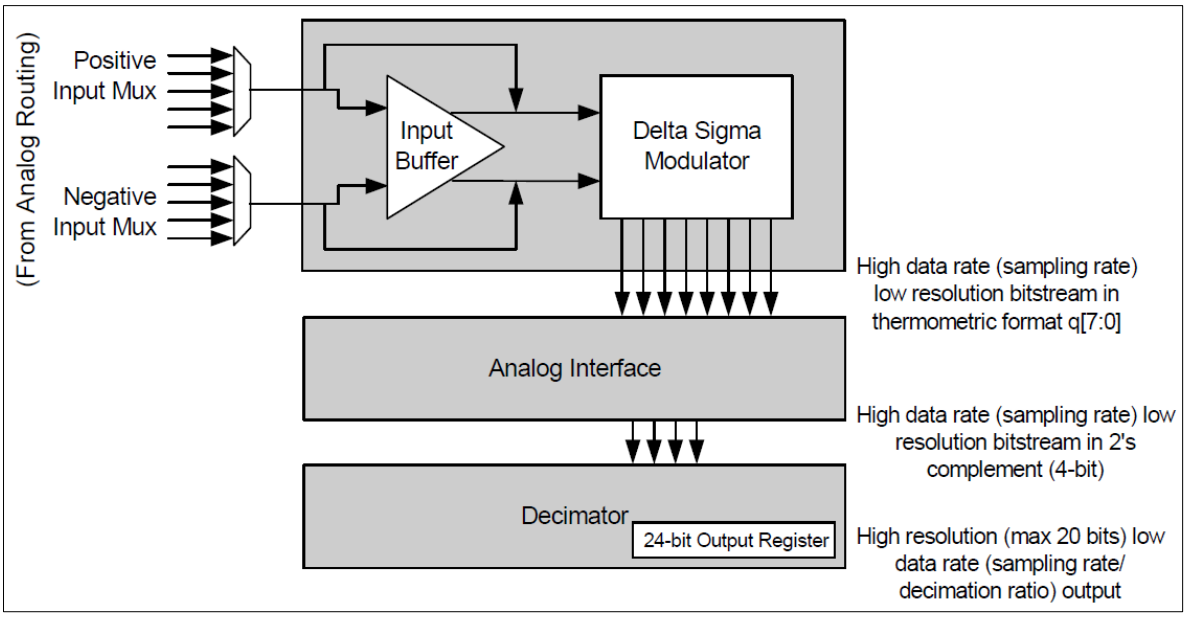
The experimental part of this work considers the ADCs embedded in the Cypress Semiconductor Programmable SoC (System-on-Chip), PSoC 5LP, (CYPRESS SEMICONDUCTOR, 2013). Such PSoC comprises two architectures of ADCS – SAR and ΣΔ for this reason, both architectures are detailed below.

3.4 Sigma-Delta Analog-to-Digital Converter (ΣΔ ADC)

This converter has the following technical characteristics: 100 μV offset, a gain error of ±0.1%, integral nonlinearity (INL) of 1 LSB, differential nonlinearity (DNL) of 0.5 LSB, and signal-to-noise ratio (SNR) of 90 dB (ΣΔ ADC) in 16-bit mode (PSoC 5LP Architecture TRM, 2017). It is possible to program this AD to work between 8 - to 20-bit resolution. It offers Internal and external reference options, differential/single ended inputs and the sample rate can be adjusted between up to 384 ksps. While the maximum clock that can be applied to the modulator is 6.144 MHz The ΣΔ ADC from PSoC 5 uses the internal 1.024-V reference (default), but an external reference is allowed.

This ΣΔ ADC is composed of three blocks: an input amplifier, a third order ΣΔ modulator, and a decimator. The input amplifier provides a high impedance input and a user selectable input gain. The decimator block contains a 4 stage Cascaded Integrator Comb (CIC) decimation filter and a post processing unit. The CIC filter operates on the data samples directly from the modulator. The post-processing unit optionally performs gain, offset, and simple filter functions on the output of the CIC decimator filter (PSoC 5LP Delta Sigma Analog to Digital Converter, 2017). Figure 3.5 shows the PSoC5 ΣΔ ADC macro block diagram.

Figure 3.5 – ΣΔ ADC Block Diagram.



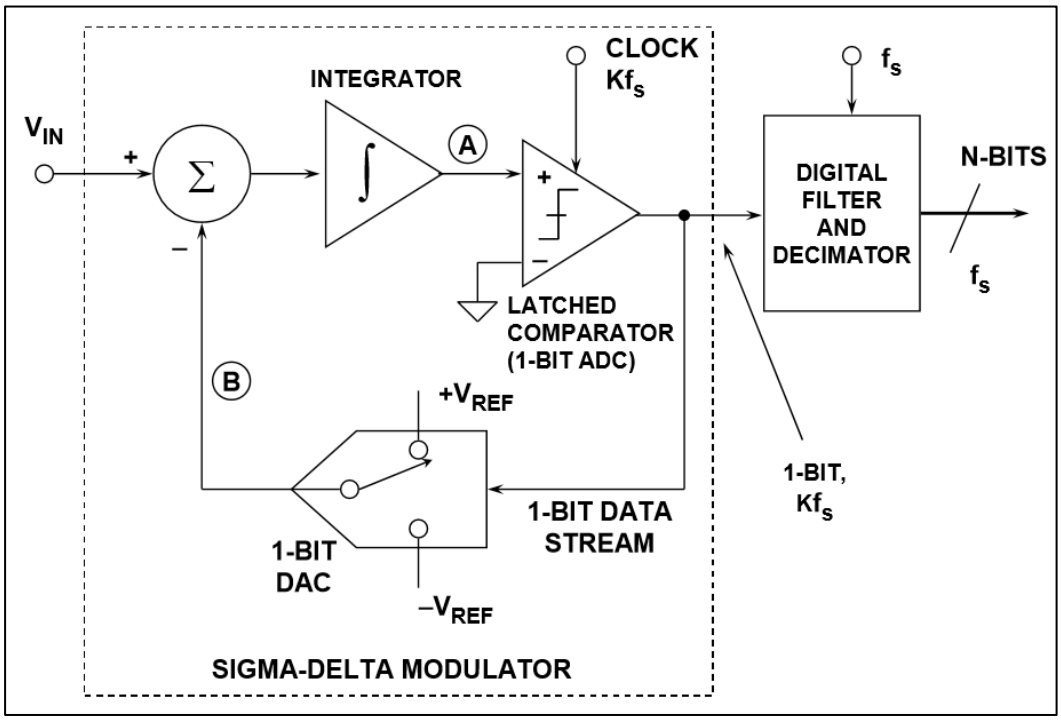
Source: PSoC 5LP Architecture TRM (2017, p. 377).

A conceptual1st order ADC modulator is shown in figure 3.6. The modulator consists in a closed loop system that constantly compares and samples the present analog input signal at the comparator positive side with the integrator voltage (KUMAR *et al*, 2016).

The ADC operates as follows: assume a dc input at VIN; the integrator is constantly ramping up or down at node A; the output of the comparator is fed back through an 1-bit DAC to the summing input at node B; the negative feedback loop from the comparator output, passing through the 1-bit DAC, back to the summing point, will force the average dc voltage at node B to be equal to VIN. This implies that the average DAC output voltage must be equal the input voltage VIN. The average DAC output voltage is controlled by the ones-density in the 1-bit data stream from the comparator output. As the input signal increases towards $+V_{REF}$,

the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. Similarly, as the signal goes negative towards $-V_{REF}$, the number of "ones" in the serial bit stream decreases, and the number of "zeros" increases. From a very simplistic standpoint, this analysis shows that the average value of the input voltage is contained in the serial bit stream produced by the comparator output. The digital filter and decimator process the serial bit stream and produce the final output data (KESTER, 2009).

Figure 3.6 – Conceptual ΣΔ ADC Modulator.



Source: KESTER (2009, p. 06).

To better understand the ΣΔ ADC, fundamentals concepts of oversampling and noise shaping need to be known. These techniques bring improvement to ADC speed and resolution. According to Maloberti (2007), the advantage of oversampling is that the signal band occupies a small fraction of the Nyquist interval making it possible to use digital cancellation ontherelativelylargefractionofthequantizationnoisethatisoutsidetheband of interest. The use an ideal digital filter after the A/D conversion removes the noise from fB to fs/2 and significantly reduces the quantization noise power by a factor of fs/(2fB) leading to:

$$V^2_{n,B} = \frac{\Delta^2}{12} \cdot \frac{2fB}{fs} = \frac{V^2_{ref}}{12.2^{2n}} \cdot \frac{1}{OSR} \quad (3.6)$$

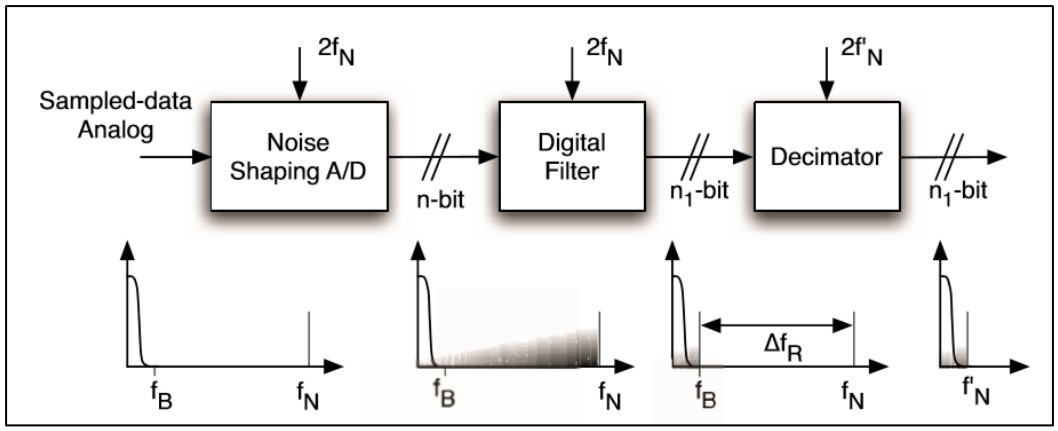
where Vref is the reference voltage and n is the number of bitsof the quantizer. The definition of the equivalent number of bits shows that an oversampling by OSR potentially improves the number of bits from n to:

$$ENOB = n + 0.5.log_2.(OSR) \quad (3.7)$$

Showing that every increase of the OSR by a factor four potentially improves the converter resolution by1-bit. For example, for gaining 5-bit resolution, it is necessary to use OSR = 1024, a high oversampling. Nevertheless, when oversampling is used to relax the anti-aliasing specifications, the additional benefit of obtaining extra bits is positive.

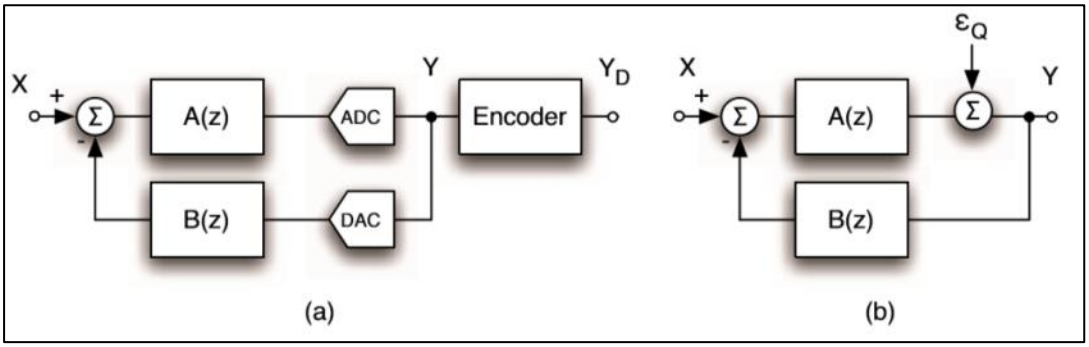
The oversampling method becomes more effective if the noise spectrum is lowered in the signal band, possibly at the expenses of an increase of the out-of-bandportion,thereby changing the white spectrum of the quantization noise into a shaped spectrum. Having more noise in high frequency regions is not problematic as the digital filter used after the ADC (Fig. 3.7) removes it. Incorporating the quantizer in a feedback loop as shownin Figure 3.8 gives rise to the desired in-band noise reduction, also called noise shaping.

Figure 3.7– Out-of-band noise rejection and decimation of a noise shaped signal.



Source: MALOBERTI (2007, p. 256).

Figure 3.8 – Incorporating the quantizer in a feedback loop obtains noise shaping



Source: MALOBERTI (2007, p. 257).

The scheme has a sampled data input that, after the processing block A(z), is converted into digital. For closing the loop it is necessary to generate the analog representation of the converted signal as done by the DAC. A second processing block A(z) is used before the subtracting element. The linear model of figure 3.8 (b) represents the quantization error with the additive noise ε_Q that is a second input of the circuit.

3.5 Successive Approximation Register (SAR)

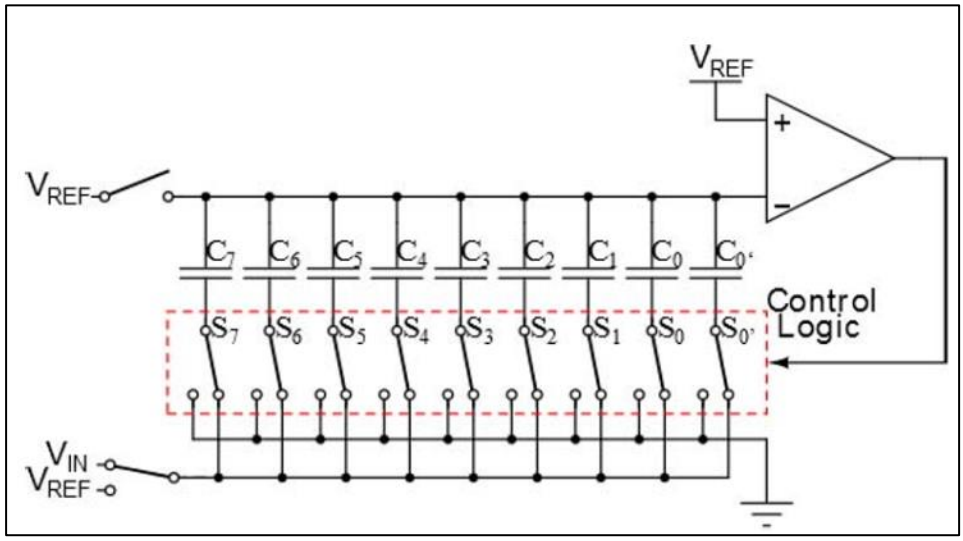
The PSoC 5LP device has two successive approximation register analog-to-digital converters (SAR ADCs) in addition to the ΣΔ ADC. The SAR ADC is designed for applications that require medium resolution and medium to high data rate. The ADC Successive Approximation Register (ADC_SAR) component provides medium-speed (maximum 1-msps sampling) and medium-resolution (12 bits maximum) (PSoC 5LP ADC Successive Approximation Register, 2015). Other relevant features are an SNR about 70 dB and rail-to-rail input (0V to Vdda) (PSoC 5LP Architecture TRM, 2017).

This SAR ADC requires a low RMS jitter clock source. The maximum frequency of the clock source is 18 MHz. The maximum jitter on the sampling clock for 12-bit resolution is 32 ps RMS. The maximum input clock that can be applied to the SAR is 18 MHz and 1 MSPS sample rate (PSoC 5LP Architecture TRM, 2017).

The SAR ADC requires a stable reference voltage between 1 V and Vdda (maximum 5.5 V). This can be set either as an internal or an external reference. The internal reference can be Vdda/2, 1.024V, 1.2V or the PSoC DAC's output voltage (PSoC 5LP Architecture TRM, 2017).

Figure 3.9 illustrates a simplified schematic of an 8-bit charge redistribution SAR ADC. This circuit consists of four main blocks: a capacitor array, a comparator, a set of switches, and the digital control logic for the switches. The capacitor array consists of N +1 binary-weighted capacitors, where N is the number of bits of the converter. Each bit is associated with one capacitor. The conversion is performed by a sequence of comparisons of the input signal with quantization levels generated by the reference voltage through the capacitive dividers formed by the switching scheme, converging to an equivalent digital representation. The code register, belonging to the digital control part of the converter, which also controls the state of the switches, will hold the final converted word after the charge redistribution phase (GONZÁLES, 2018).

Figure 3.9 – Simplified Schematic of an 8-bit SAR ADC.

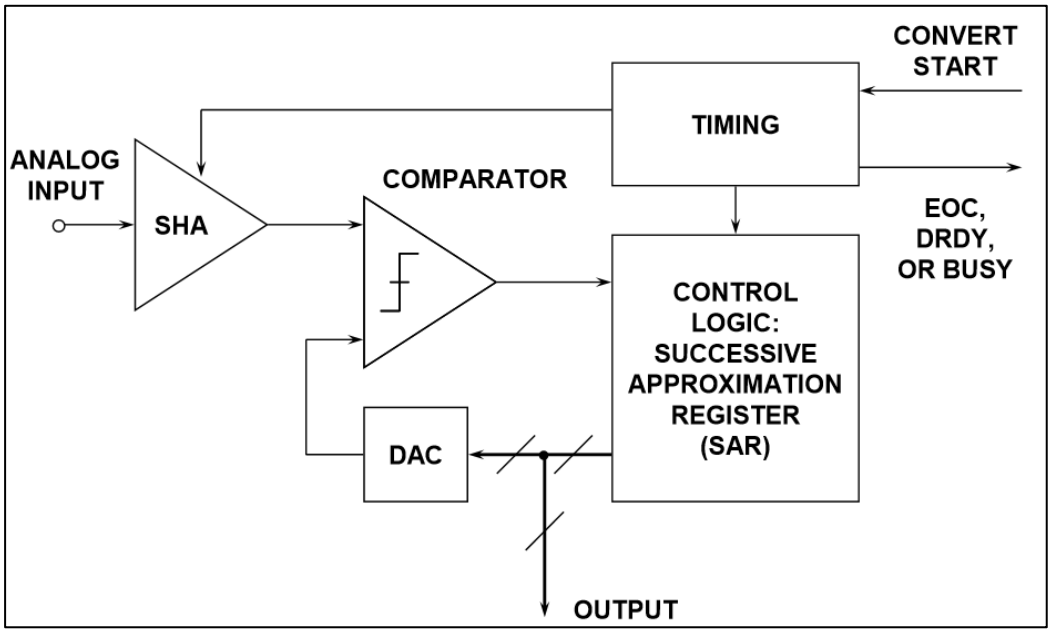


Source: GONZÁLES (2018, p. 06).

Figure 3.10 shows the SAR basic working. On the assertion of the CONVERT START command, the sample-and-hold (S&H) is placed in the hold mode, and the internal DAC is set to midscale. The comparator determines whether the S&H output is above or below the DAC output, and the result (bit 1, the most significant bit of the conversion) is stored in the successive approximation register (SAR). The DAC is then set either to ¼ scale or ¾ scale (depending on the value of bit 1), and the comparator makes the decision for bit 2 of the conversion. The result is stored in the register, and the process continues until all of the bit values have been determined. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the digital value of the analog input, and the conversion is complete (KULARATNA, 2008). Note that the acronym "SAR" actually stands for

Successive Approximation Register (the logic block that controls the conversion process), but is universally accepted as the acronym for the architecture itself (KESTER, 2009).

Figure 3.10– Basic Successive Approximation ADC



Source: KESTER (2009, p. 01).

4. DEVICE AND DESIGN UNDER TEST (DUT)

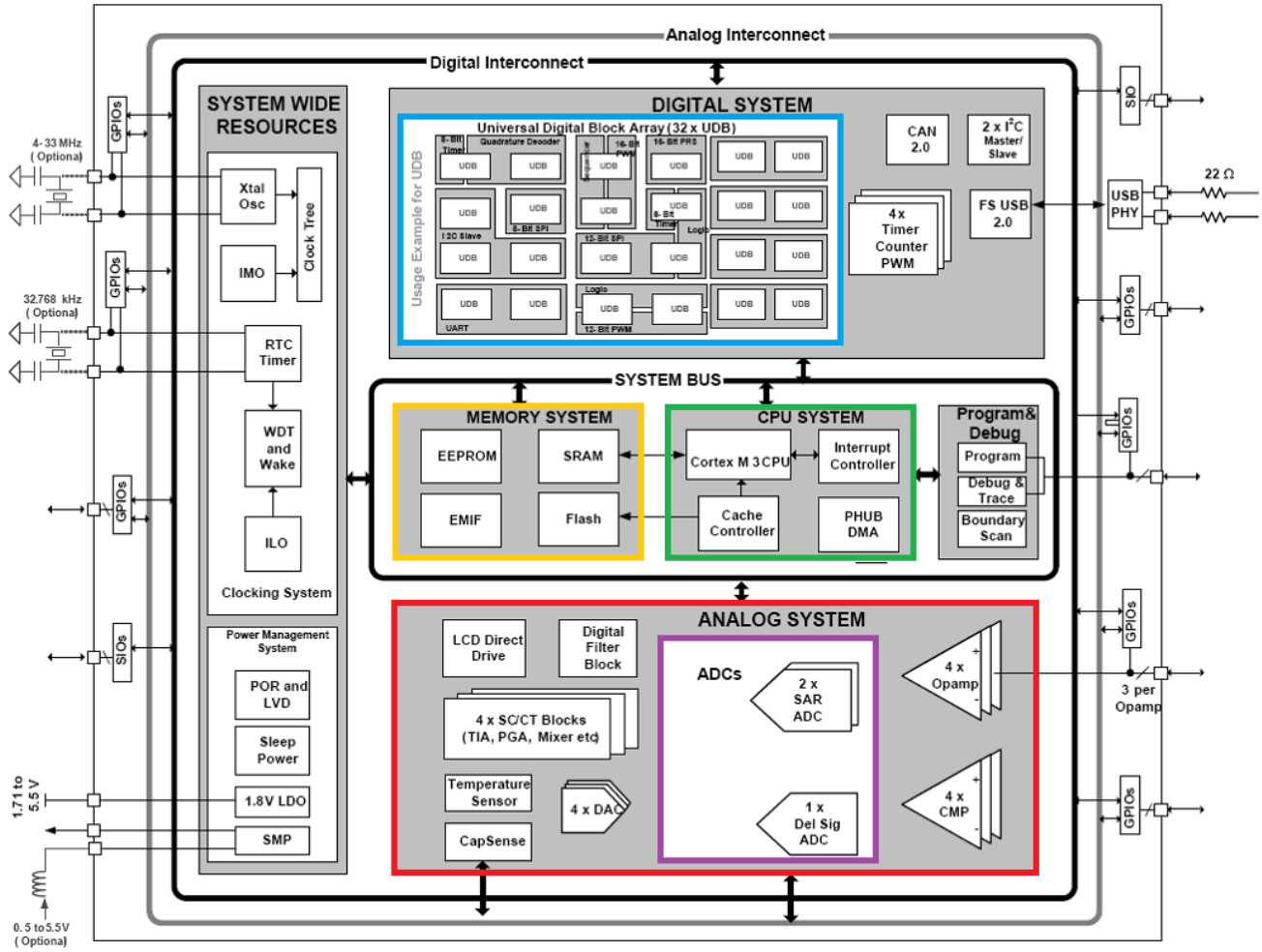
In this chapter, the device and the design on which tests were performed are presented. The DUT consists of a Data Acquisition System (DAS) programmed into a PSoC. The PSoC 5LP is a device that integrates configurable analog and digital peripherals, memory and microprocessor on a single chip (CYPRESS SEMICONDUCTOR, 2015). Besides that, the PSoC 5LP includes two Successive Approximation Register (SAR) ADCs and one ΣΔ ADC which, in this work, reevaluated when exposed to electromagnetic interference (EMI).

Section 4.1 describes the main features of the PsoC 5LP, while section 4.2 addresses issues related to the implemented DAS.

4.1 Programmable SoC (PSoC 5LP) Technical Features

The DAS was implemented in a commercial, programmable, mixed-signal SoC called PSoC 5LP (CYPRESS SEMICONDUCTOR, 2013a), from Cypress Semiconductor. The architecture block diagram of this integrated circuit is shown in figure 4.1. The PSoC 5LP part number used is CY8C5588AXI-060. The device is manufactured in 130 nm CMOS technology and consists of a Cortex ARM CPU32-bit M3 (up to80 MHz clock), 256 KB Flash Memory, 64 KB SRAM Memory, 2 KB EEPROM, 24 channels of Direct Memory Access (DMA),digital peripherals as communication interfaces and, additionally, UDB-based(Universal Digital Blocks), Programmable Logic Devices (PLDs),which provide the implementation of various functions such as timers, counters and others.

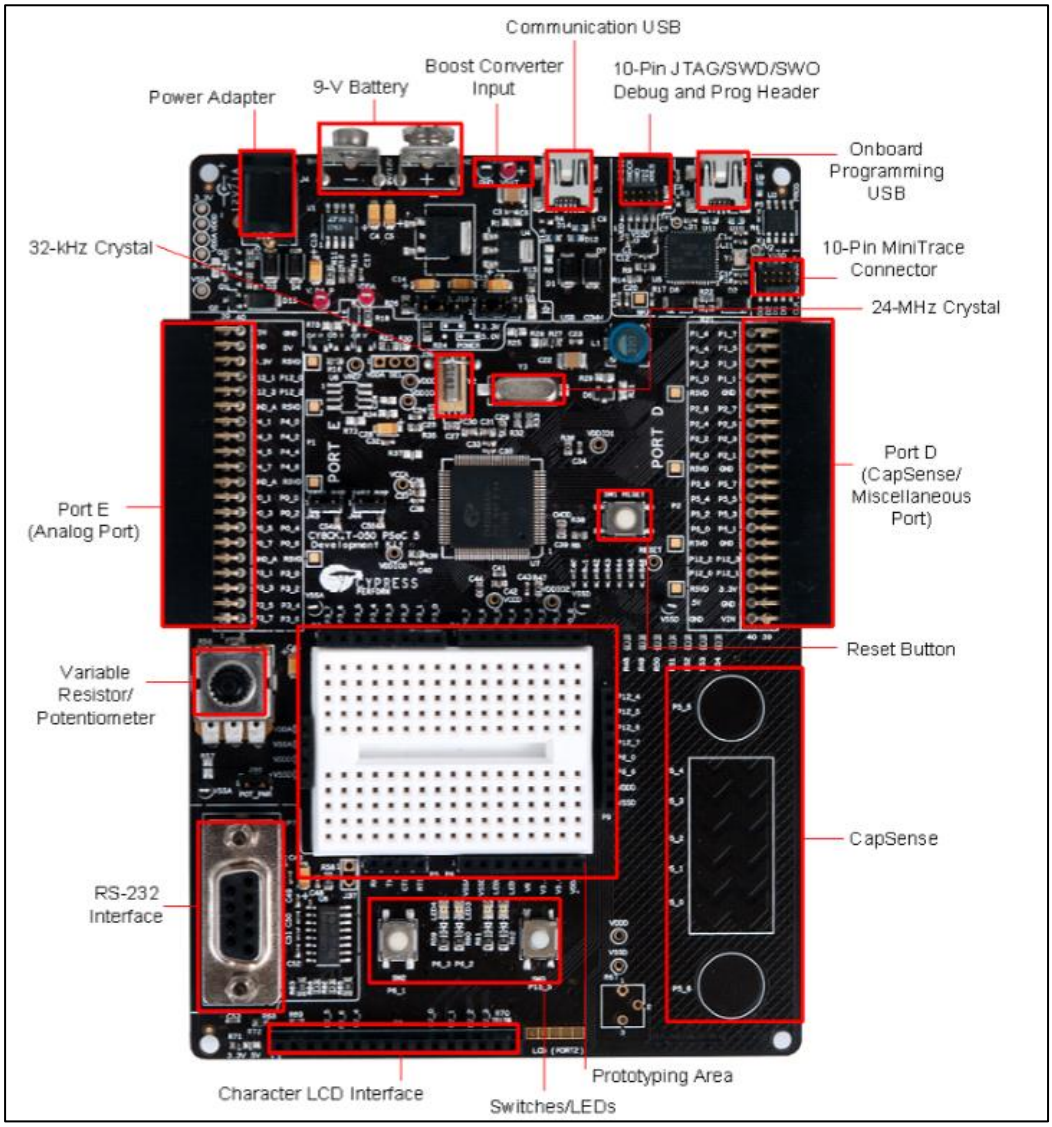
Figure 4.1 – PSoC overall block diagram



Source: CYPRESS SEMICONDUCTOR(2018, p. 04).

Fig. 4.2 shows PSoC 5LP development kit general details. The main technical features will be better detailed as follows.

Figure 4.2 – PSoC 5LP Development KIT general view

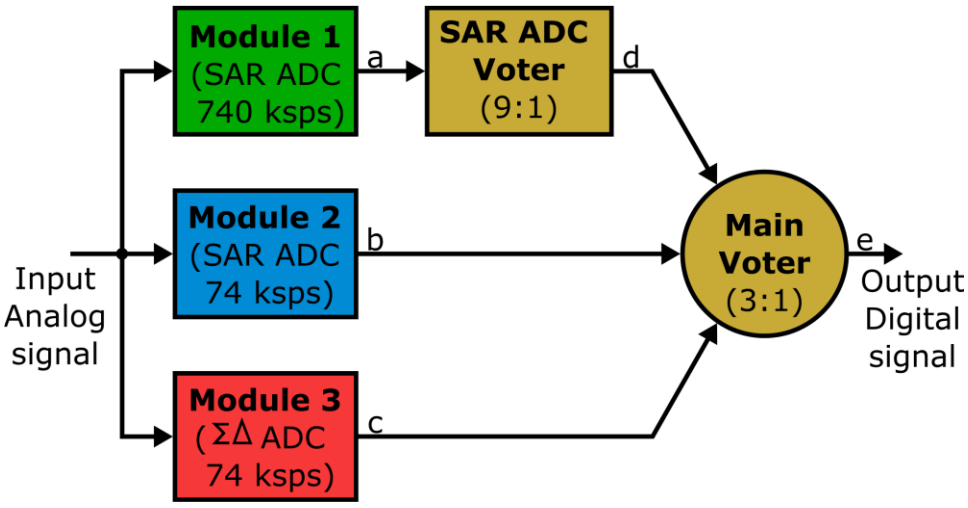


Source: CYPRESS SEMICONDUCTOR (2013, p. 15).

4.2 Data Acquisition System

The current study considers a previously proposed System (CHENET et al. 2015) which is based on TMR with design diversity (DTMR) implementing a fault tolerant data acquisition system (DAS), prototyped in a PSoC. The objectives are, firstly, to evaluate the behavior of different architectures of data converters under direct radio frequency (RF) power injection in their reference voltage and supply pins, and then to evaluate the effectiveness of the studied DTRM technique to mitigate EMI effects in this system. The fault tolerant DASsimplified block diagram is shown in Figure4.3.

Figure 4.3 – DAS scheme based on TMR and diversity



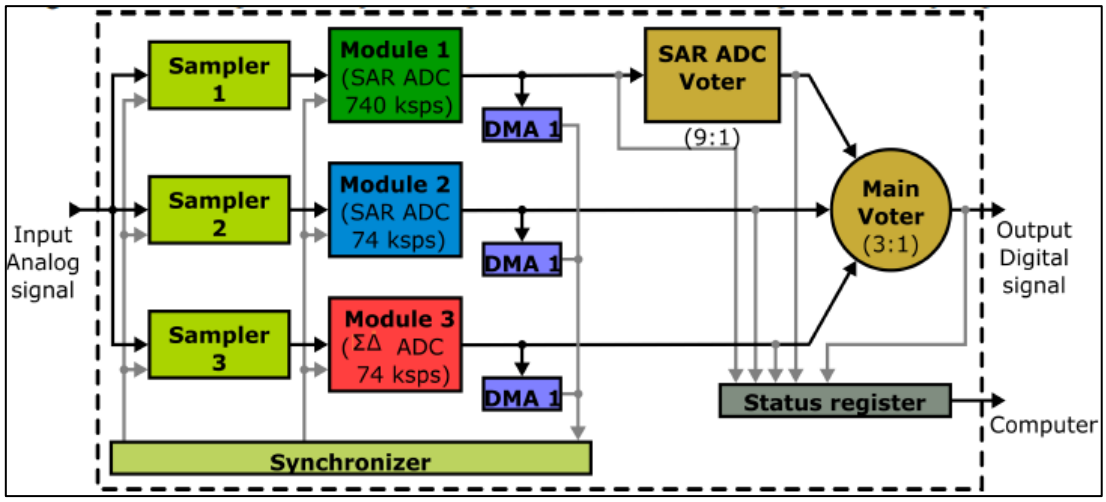
Source: CHENET (2015, p. 61).

The system is composed of three parallel converters: two Successive Approximation Register (SAR) ADCs and one ΣΔ ADC architecture. These converters operate in different working frequencies; the first SARADC operates with a sampling rate of 740 ksps (kilo samples per second) and the other two converters (SAR – module 2 – and ΣΔ ADC) work with a sampling rate of 74 ksps. This way a triple modular redundancy (TMR) approach is achieved. The use of different converter architectures constitutes the spatial (or hardware) diversity, and the different sampling rates constitute the temporal diversity (CHENET, 2015). Within the implementation of the system, it is necessary to build a voting structure: a temporal SAR ADC voter to vote upon the oversampled words generated by the SAR operating at 740 ksps and a main voter who conducts the voting between the SAR ADC voter output and the other two converters. The ADC SAR voting is done bit-by-bit considering 9-out-of-10 samples generated by the ADC (one is discarded to have an odd number); performing also the

coarse synchronization of the system (its output throughput is then 74 ksps). In the end, after the voting, the digital output of the system is obtained. The whole voting system is implemented in software.

Figure 4.4 shows in detail the full implementation of DAS on PSoC 5LP. Beyond analog-to-digital converters and voters initially planned, the implementation demands samplers (sample-and-hold blocks), direct memory access (DMA) units and a fine-synchronizer, to cope with the different latencies of the converters.

Figure 4.4 – Detailed implementation of DAS into the PSoC 5LP



Source: AGUILERA (2018, p. 41).

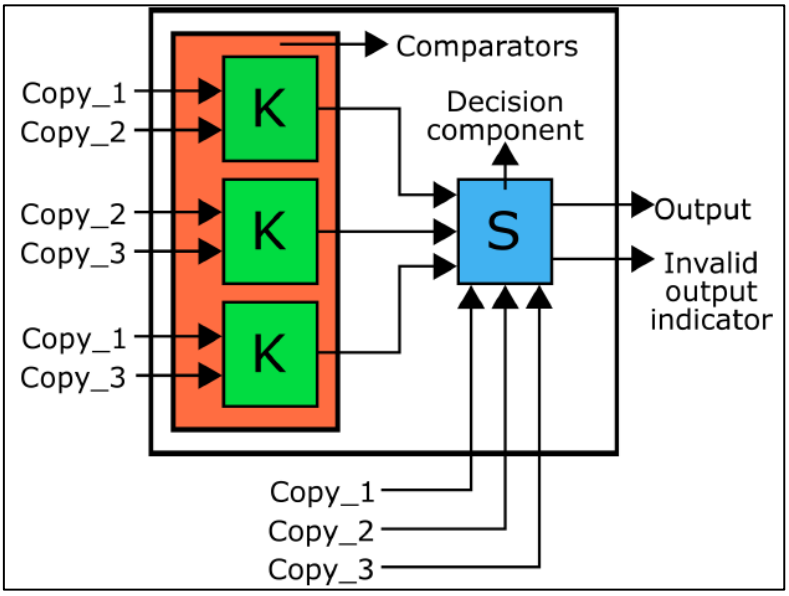
The adopted scheme consists in one individual sample-and-hold for each ADC, triggered by a synchronizer circuit, as shown in figure 4.4. The first advantage of this scheme is that it provides an extra redundancy, as using a single sampler could generate an incorrect response of the system in the case of an error affecting this block. The second advantage of the is that the impedance seen by the sampler output is higher than in a scheme with three ADCs connected in a single block. This way the samplers can maintain the sampled data for a higher period of time. The ADCs were implemented with prebuilt components of the PSoC 5LP. They were set to 8-bit resolution, internal clock source, internal reference voltage, and analog input in common and in the range 0 to 2,048 V.

The basic voting concept adopted in the implementation of the main voter and the ADC SAR voter was the majority voting. The majority voting has the disadvantage of loss in accuracy when applied to mixed-signal systems due to the need of a threshold for the

construction of a tolerance window, which allows the majority to be determined when the data to be voted on is approximate, but not exactly the same as in most digital systems.

The implementation of majority voting in the digital domain can be done by following the bit-by-bit voting or word voting concepts (CHENET, 2015). The word voter adopted in this system, as illustrated in figure 4.5, consists of three comparators and one decision element. The comparators perform mutual subtractions between the outputs of the three redundant copies (comprising all possible combinations), producing three error signals. Based on these error signals, the decision element selects the correct value for the voter's output.

Figure 4.5 – Representation of word voting scheme



Source: CHENET (2018, p. 05).

The software (C language code) used to program this voter is shown in figure 4.6. The tolerance window has been set to 4 decimal units and an indication (main_voter_error_det) is generated in the case an error is detected.

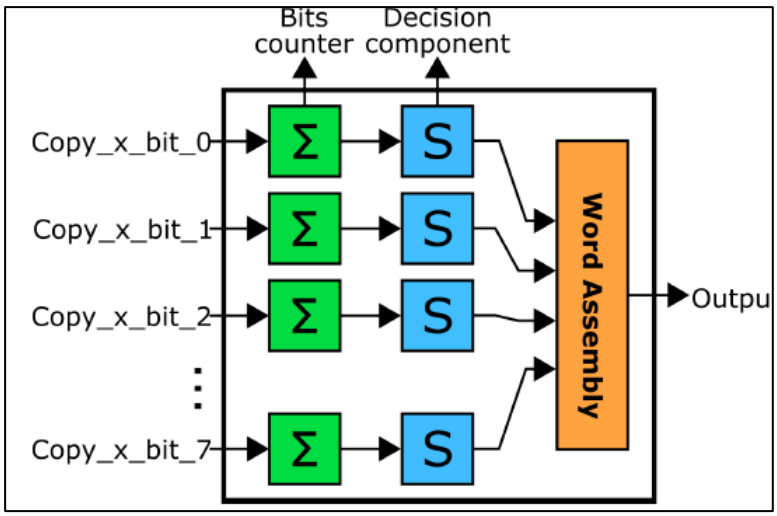
Figure 4.6 – Software code generated to implement the main word voter algorithm

```
1     void main_voter()
2     {
3         error1 = abs (SAR_ADC_voter_data - module2Data[1]);
4         error2 = abs (module2Data[1] - module3Data[1]);
5         error3 = abs (module3Data[1] - SAR_ADC_voter_data);
6
7         if (error1 <= 4)
8             system_output = SAR_ADC_voter_data;
9         else if (error2 <= 4)
10            system_output = module2Data[1];
11        else if (error3 <= 4)
12            system_output = module3Data[1];
13        else
14            system_output = 0;
15
16        if ((error1 > 4) ||  (error2 > 4) || (error3 > 4))
17            main_voter_error_det = 1;
18    }
```

Source: CHENET (2015, p. 66).

As illustrated in figure 4.7, bit-by-bit voting consists of a counter and a decision element for each bit position, as well as a word assembler. The number of ‘ones’ of each bit position between all words is counted and this information is taken to the decision element, which votes (if the bit is zero or one)based on the number of counted ‘ones’. Subsequently, each of these voted bits is submitted to the word assembler, whose generates the output word. The advantage of bit-by-bit voter is that it is easier to implement in the case of many voting inputs (as is the case of this block: 9 inputs).

Figure 4.7 – Representation of bit-by-bit voting scheme



Source: AGUILERA (2018, p. 43).

The software (C language code) used to program this voter is shown in figure4.8. If at any bit position different logical states are detected between words, an indication (SAR_ADC_voter_error_det) is generated.

Figure 4.8 – Software code generated to implemented the main bit-by-bit voter algorithm

```
1     void SAR_ADC_voter()
2     {
3         bits = 0;
4         SAR_ADC_voter_data = 0;
5         for (i = 0; i < 8; i++)
6             bit_counter[i] = 0;
7
8         for (i = 0; i < 8; i++)
9         {
10            for (j = 1; j < 10; j++)
11            {
12                bits = (module1Data[j] & mask[i]) != 0;
13                if (bits == 1)
14                    bit_counter[i] = bit_counter[i] + 1;
15            }
16        }
17
18        for (i = 0; i < 8; i++)
19        {
20            if (bit_counter[i] > 4)
21                SAR_ADC_voter_data = SAR_ADC_voter_data + mask[i];
22        }
23
24        bigger = module1Data[1];
25        smaller = module1Data[1];
26        for (pointer = 2; pointer < 10; pointer++)
27        {
28            if (bigger < module1Data[pointer])
29                bigger = module1Data[pointer];
30            if (smaller > module1Data[pointer])
31                smaller = module1Data[pointer];
32        }
33        error = bigger - smaller;
34        if (error > 4)
35            SAR_ADC_voter_error_det = 1;
36    }
```

Source: CHENET (2015, p. 67).

5. TEST SETUP

The main objective of this study is to evaluate the impact of conducted electromagnetic interference (EMI) on the three different converters of the Cypress Semiconductor Programmable SoC (System-on-Chip) system (PSoC 5LP) PSoC (CYPRESS SEMICONDUCTOR, 2013) and discuss whether the methodology of redundancy with hardware diversity is effective for this type of interference.

To make it possible, a study of the IEC standards 62132-4 (IEC, 2006) and 62132-1 (IEC, 2006) was done, together with a study of the PSoC 5LP device. These standards describe a method for measuring immunity of integrated circuits (IC) in the presence of conducted RF disturbances. This method ensures a high degree of repeatability and correlation of immunity measurements. Besides that, it establishes a common base for the evaluation of semiconductor devices used in equipment functioning in an environment subject to unwanted radio frequency electromagnetic waves.

A major challenge that eventually became one of the main contributions of this work was to propose a setup of tests that were both real and feasible using the available laboratory infrastructure at UFRGS.

Throughout the text of this chapter there will be notes specifying some points that could not be followed as the norm, but it is important to emphasize that the results can be used in a comparative way, since they were obtained with this same setup.

5.1 Requirements of IEC 62132-4

This part of IEC 62132 describes a method to measure the immunity of integrated circuits (IC) in the presence of conducted RF disturbances, e.g. resulting from radiated RF disturbances.

The minimum electromagnetic immunity level required for an IC depends on the maximum permitted level of RF disturbance to which an electronic system can be submitted. The value of the immunity level is dependent on system and application specific parameters. To determine the immunity performance of an IC, a simple measurement procedure, and a measurement setup in which resonances are avoided, is required to guarantee a high degree of repeatability (IEC 62132-4, 2006).

To characterize the immunity of an IC, the forward power needed to cause malfunction is measured. The malfunction may be classified from A to D according to the performance classes defined in IEC 62132-1:

Class A: all functions of the IC perform as designed during and after exposure to a disturbance.

Class B: all functions of the IC perform as designed during exposure; however, one or more of them may go beyond the specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain in class A.

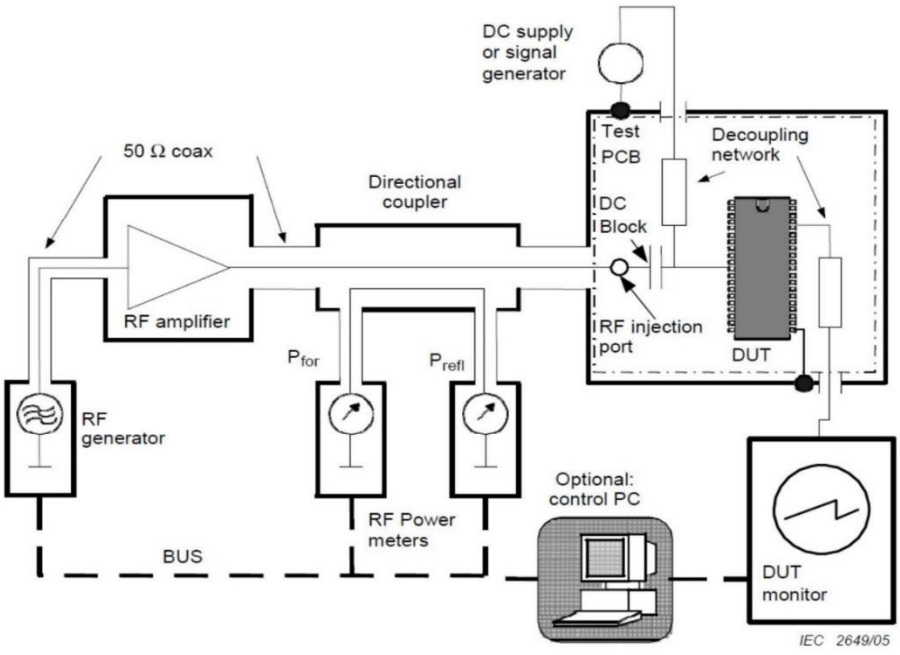
Class C: a function of the IC doesn't perform as designed during exposure but returns automatically to normal operation after exposure is removed.

Class D: a function of the IC doesn't perform as designed during exposure and doesn't return to normal operation until exposure is removed and the IC is reset by simple operator action (e.g. switch off supply).

Class E: one or more functions of an integrated circuit does not perform as designed during and after exposure and cannot be returned to proper operation.

Fig. 5.1 shows the main hardware setup to perform the test, according to the IEC standard. The RF generator provides the RF disturbance that is amplified by the connected RF amplifiers, when necessary. The directional coupler and the RF power meters are used to measure the actual forward power injected into the device under test (DUT). At the RF injection port the RF power is delivered to the test PCB. The RF amplifier is decoupled by a DC block to avoid supplying DC into the amplifier output. The DC supply (or signal generator) is prevented from getting RF power by a decoupling network that has a high RF impedance on the side that is connected to the RF injection path. A PC may be used to control the instruments and monitor de DUT. Besides that the test setup demands coaxial cables, connectors and adapters.

Figure 5.1 – Arrangement of a direct injection test set-up



Source: IEC 62132-4 (2006, p. 15).

Basically, this injection set-up has a mismatched termination. A high percentage of the power delivered to the DUT may be reflected due to the fact that an IC is not a 50 Ω termination. Matching the impedance of the DUT using a dissipative network would lead to measuring the power dissipation of matching network rather than the power delivered to the DUT. Power reflected by the DUT should not be reflected to the DUT again by an impedance discontinuity somewhere else in the power injection setup. Therefore, the power injection setup which is not on the test board shall be a 50 Ω system. This leads to a set of recommended parameters for the test board, the test setup and the components belonging to the test setup according to IEC 62132-4.

For practical tests, directional decoupling was not used and the reflected power was not measured, so it is not possible to guarantee what was the power absorbed by the DUT in relation to the power provided by the generator. Although the tests were done in this condition, the comparison between the results is reliable.

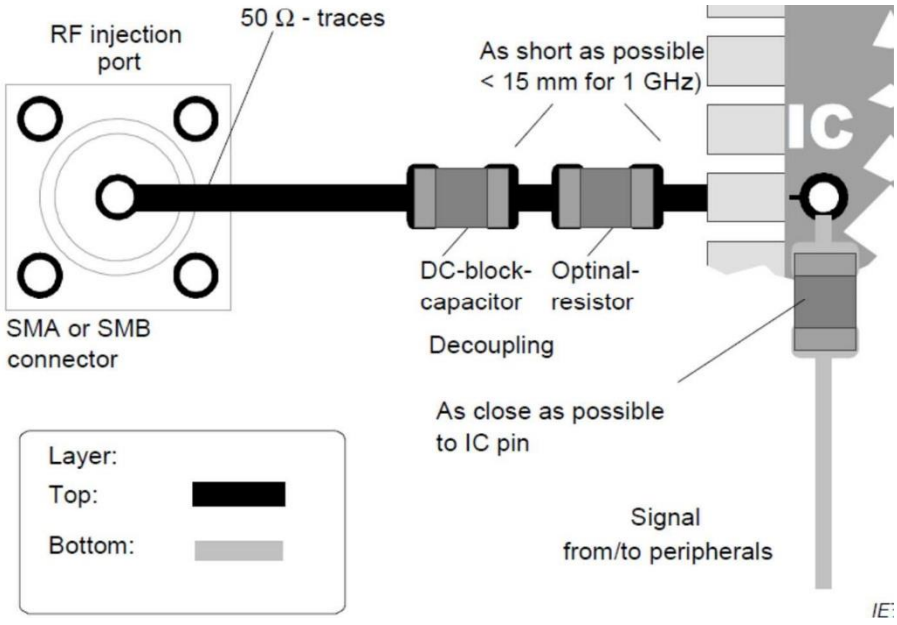
The use of a printed circuit board with a common RF ground plane for immunity testing of ICs is recommended. The DUT should be placed on the test board without sockets

because most sockets have a significant inductance that will affect the test (for instance 10 nH at 1 GHz makes de inductive reactance, XL = 63 Ω).

The main purpose of this standard is to test only the immunity of the DUT. Therefore, all external protection components of the DUT shall be removed unless it is absolutely mandatory to have these external components in order to achieve proper function on the IC (blocking capacitors, timer capacitors, etc.). Mandatory blocking means that it cannot be removed without jeopardizing proper function of the IC. Such mandatory blocking shall be placed directly on the IC and be regarded as if it would be part of it. All blocking components that are mandatory for the application shall be grounded on the same ground plane. Return paths from mandatory blocking components to the DUT or the shield of a transmission line should not have slits.

The trace from RF injection port connector to the DC blocking capacitor shall be a 50 Ω transmission line as shown in Fig. 5.2. The end of the transmission line to the pin of the DUT should be as short as possible. A trace length equal to 1/20 of the shortest wavelength applied is a reasonable target. Shorter trace lengths are advantageous. The ground plane shall not have slits in the return paths of RF carrying traces exceeding 1/20 of the shortest wavelength. To have a reliable ground reference, the impedance between the DUT ground pin(s) and the shield of any transmission line providing the RF signal shall be as low as possible. Therefore, using a ground plane on the PCB to minimize the impedance of ground connections is recommended. The RF decoupling should be as close as possible to the pin with RF power injection.

Figure 5.2 – Example of the routing from the injection port to a pin of the DUT



Source: IEC 62132-4 (2006, p. 25)

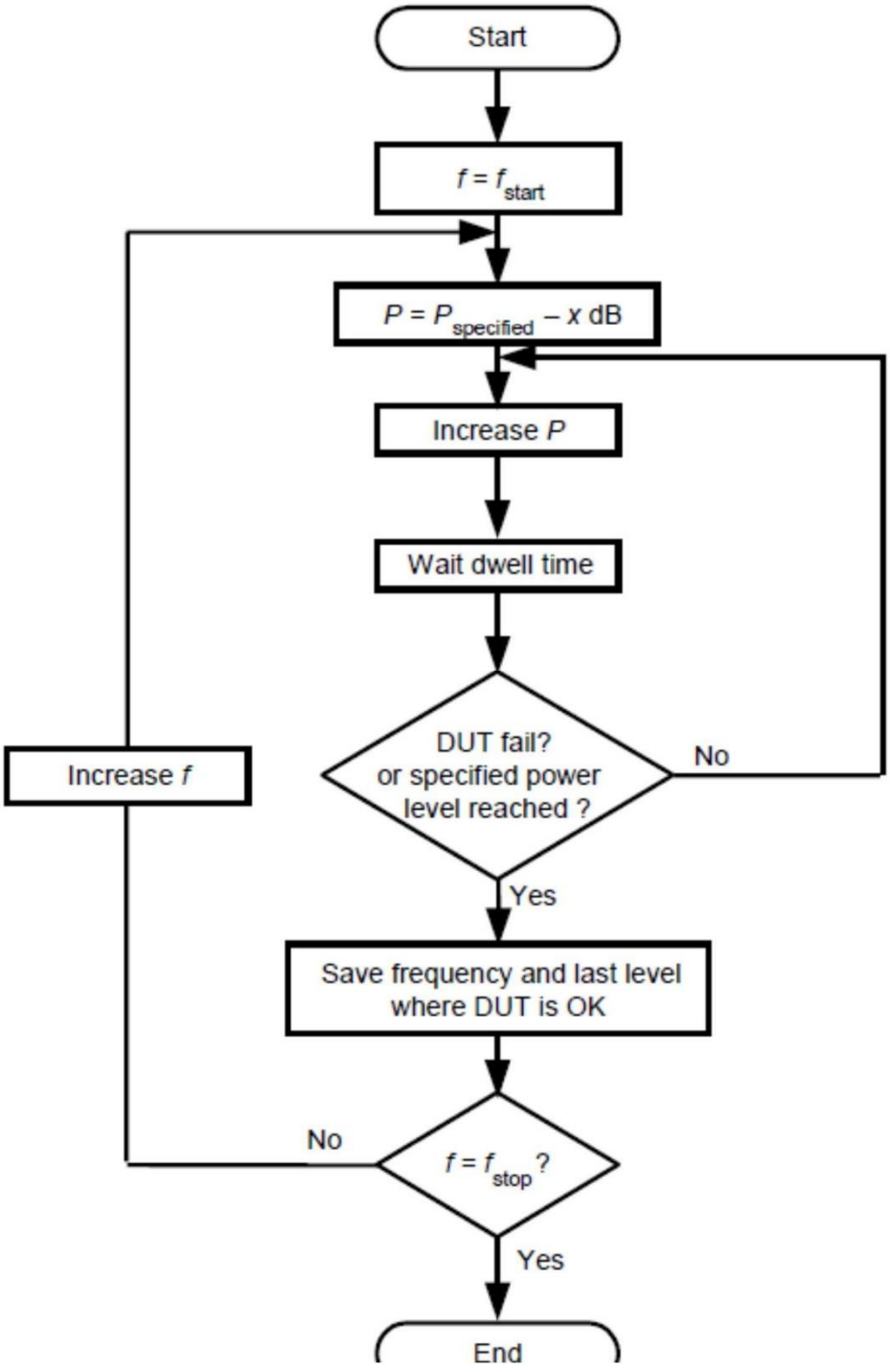
5.2 Test Procedure

In this test procedure, the DUT is tested in a sequence of frequency steps and test level steps. Fig. 5.3 shows the flowchart of an example of the specific RF power injection sequence.

At each frequency of interest, the forward power delivered to the DUT will start from low levels, e.g. 20 dB below the forward power level specified for the test. The level can then be increased in steps until a malfunction is observed, or the specified forward power level is reached. Each power level shall be kept long enough (dwell time) to allow the IC to react (e.g. if timer functions are included in the DUT). The recommended default power level step can be 0.5 dB. Default frequency steps and the dwell time are defined in IEC 62132-1. The dwell time for each frequency step and modulation shall be typically 1s or at least the time necessary for the DUT to respond, i.e., the measurement system to record.

In addition, the power leveling can be started at a specified forward power level, decreasing the level in steps until proper function or a minimum forward power level is reached. This procedure reduces the total duration of a test run mainly for a highly immune DUT according IEC 63132-4.

Figure 5.3 – Flowchart of a test procedure



Source: IEC 62132-4 (2006, p. 29).

The frequency range of these measurements is generally from 150 kHz to 1 GHz. In practice the tested frequency range depends on the cut-off frequencies of the injection network and test setup, e.g. IC decoupling. Frequency step size shall be selected according to table 5.1. However, to perform the tests, the power increase did not follow exactly what is indicated by

the standard. The tests were focused on certain powers, such as 10 and 17dBm, and on these powers the frequency increments were performed as indicated in table 5.1.

The time defined for each frequency step in this work took into acount that the minimal disturbance injection time must be at least equal to the time of a conversion cycle. In the tested DAS system, the conversion period of the slower converters is 13.5μs. In this work, the time chosen for each frequency step is 3 and 6 seconds, depending on the frequency range (as detailed below). Therefore, in each step we have a significant number of conversions.

Table 5.1 - Frequency step size versus frequency range

Frequency range	MHz	0,15 – 1	1 – 100	100 – 1000
Linear steps	MHz	δ0,1	δ1	δ10
Logarithmic steps		δ5 % increment		

Source: IEC 62132-1 (2006, p. 29).

The disturbance signal used is in accordance with the requirements of the test method chosen: sine wave, amplitude modulated (modulation deep of 80%) by a 1 kHz sine wave.

The necessary test power level depends on the application of the integrated circuit and the pin of the IC, which is to be tested. Depending on the possible filtering and decoupling from the disturbance signal, a different test level should be used. These circumstances could be described as protective zones and power levels related to the zones. The table 5.2 shows the power level of the signals.

Table 5.2 - Immunity level ranges and power levels

Zone	Power dBm	Power W	Device externally protected by	Example for devices
1	30…37	1…5	Nothing or only a small capacitor as filter	High side switches, power supply circuits, bus-transceiver for driving wire harness (e.g. CAN, LIN)
2	20…27	0,1…0,5	L-,R-,C-low pass filter	Signal conditioning devices, ABS sensor circuit, communication line driver
3	10…17	0,01…0,05	No direct connection to the environment, decoupling by placing	Microcontroller, memories

Source: IEC 62132-4 (2006, p. 31).

During the test, the DUT can be checked on various parameters or responses. Examples includes: DC output voltage, Supply current, Jitter, Spikes and glitches, System

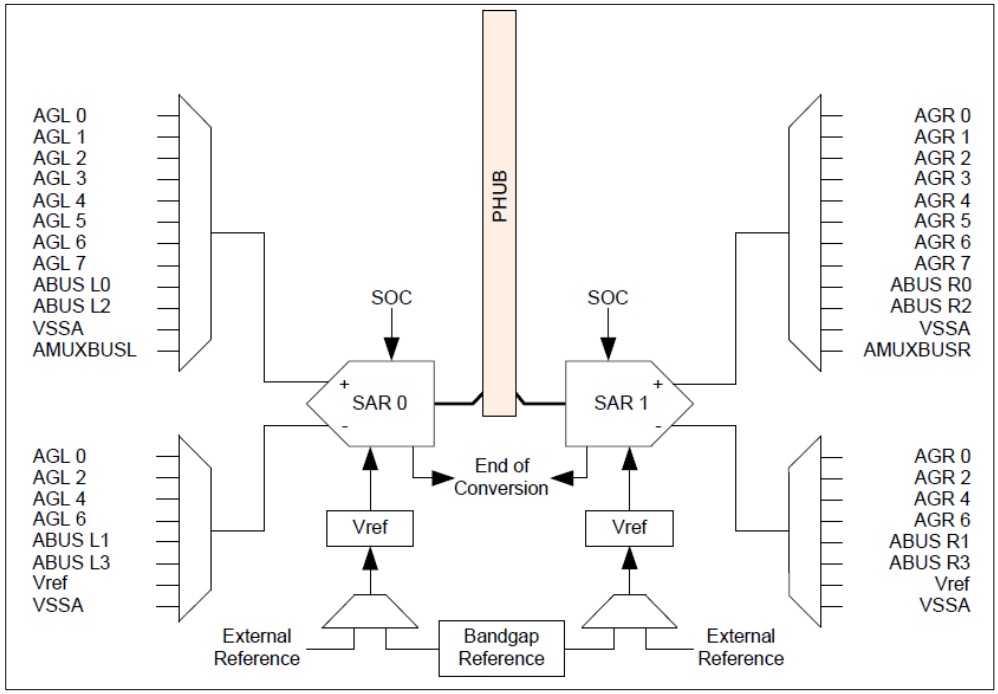
reset, System hang-ups and Latch-up. In this work, taking advantage of the system voters the converted words of the three converters are compared, in order to identify conversion errors during the EMI tests.

After studying the standard IEC 62132-4 and the Programmable SoC (System-onChip) technical characteristics, it is possible suggest a PVT (Plan Test Valuation) and the infrastructure required (appendix A) focused on injection and mitigation of EMI in mixed signal converters.

The test was conducted at Laboratories of the Graduate Program in Microelectronics at Federal University of Rio Grande do Sul in Porto Alegre.

The selected injection point share the reference voltage (VREF) of each converter and the analog supply voltage VSSA of the system. The signal was generated by an Agilent N9310A RF signal generator. Figure 5.4 shows that it is possible to select an external voltage reference to the SAR ADC through programmable muxes, so the EMI disturbance may be injected using these ports.

Figure 5.4– SAR ADC Block Diagram

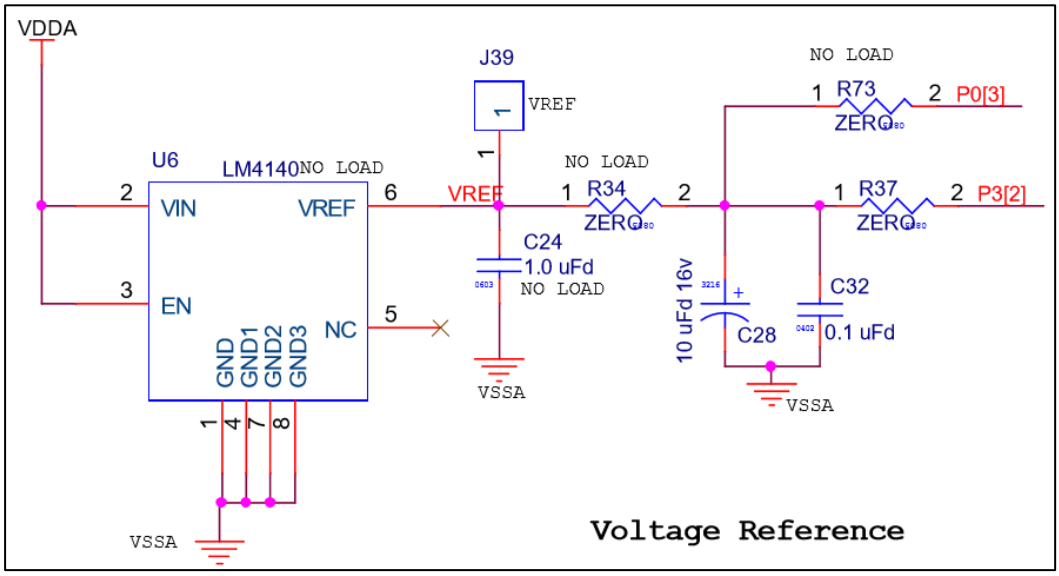


Source: PSoC 5LP Architecture TRM (CYPRESS, 2017, p. 397).

In the first test setup, while injecting the EMI signal at the VREF pin, a fixed signal with different DC voltage levels was applied at the system input: GND, 25%, 50%, 75% and 100% of the reference voltage of each converter (1,024 V).

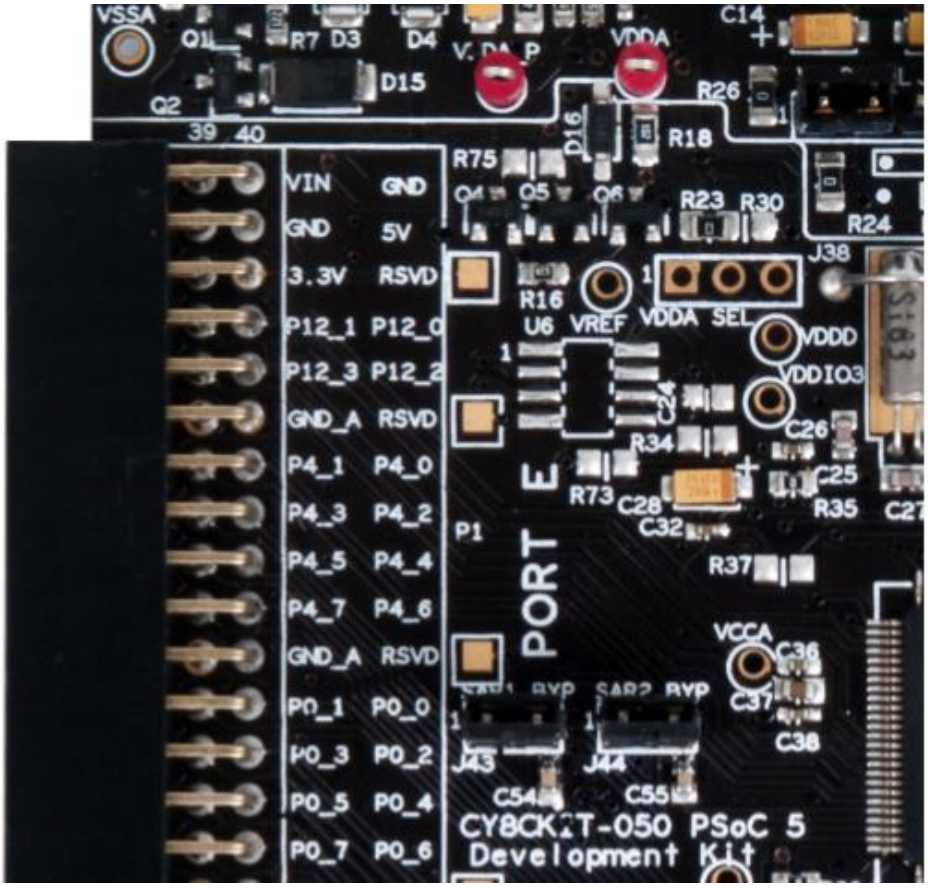
The reference voltage shall be provided from an external source. For this, the test point the jumper J39 of the development board was used as shown in the figures 5.5 and 5.6.

Figure 5.5 – PSoC 5LP Voltage reference circuit schematic



Source: PSoC 5LP development kit guide (CYPRESS, 2013, p. 43).

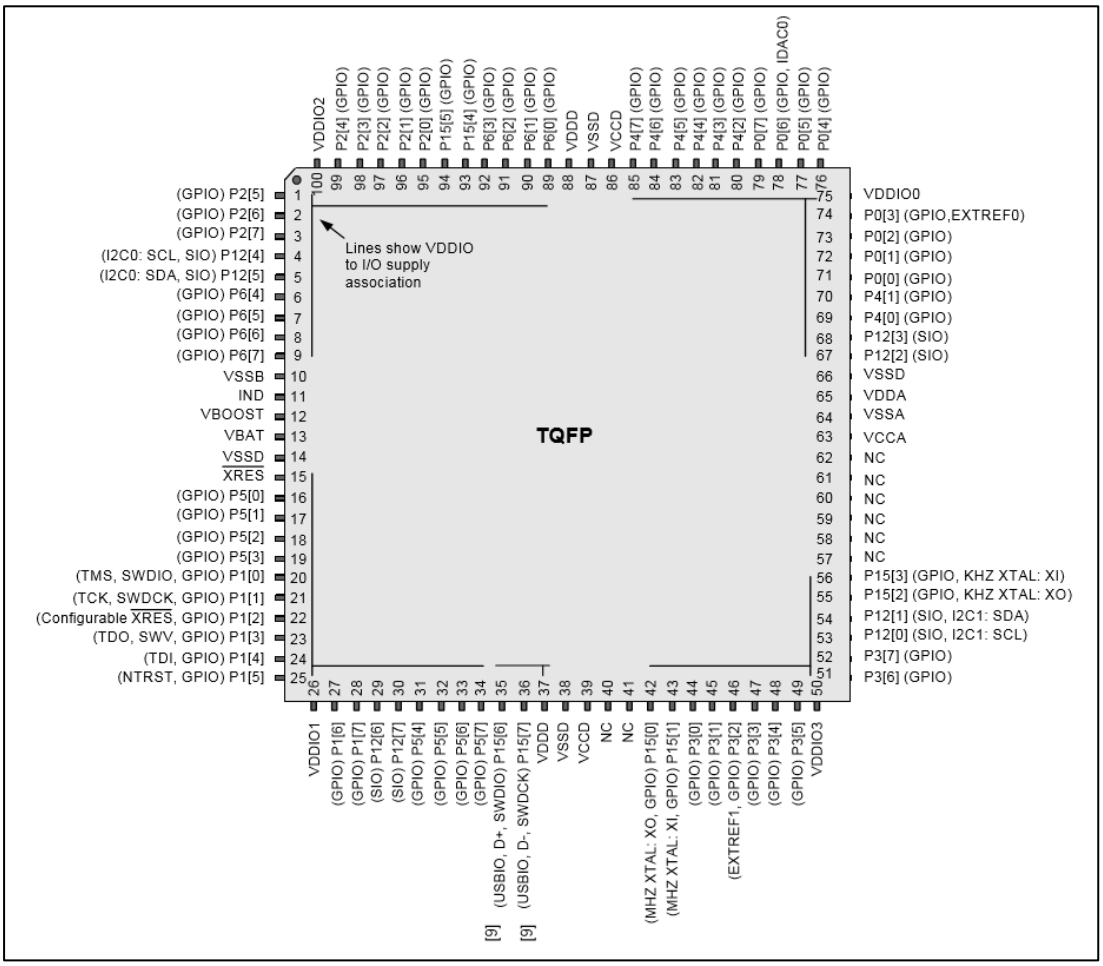
Figure 5.6– PSoC 5LP voltage reference circuit



Source: PSoC 5LP development kit guide (CYPRESS, 2013, p. 25).

This test point (J39) is also used to apply the DPI technique. Thus, using this test procedure, the noise injection is performed directly on the reference voltage. In Figure 5.7,it is possible to see the 100-pin TQFP Part Pin out. The pins P0[3] and P3[2] are GPIO (general purpose IO) and Ext Vref (external V_{REF}) and both are connected with J39 (test point).

Figure 5.7– 100-pin TQFP Part Pinout



Source: PSoC 5LP datasheet (CYPRESS, 2013, p. 08).

Tests were also performed using a sine wave as input of the system: a 120 Hz frequency, DC level of 0.96 V and peak-peak amplitude 1.88 V. The entire input amplitude range of the converters has not been used due to different nonlinearities between SAR converters and Sigma-Delta. For receiving the DUT status log and report generation a host computer with the TeraTerm software (TERA TERM, 2014) was used, recording the serial data by means of an USB port.

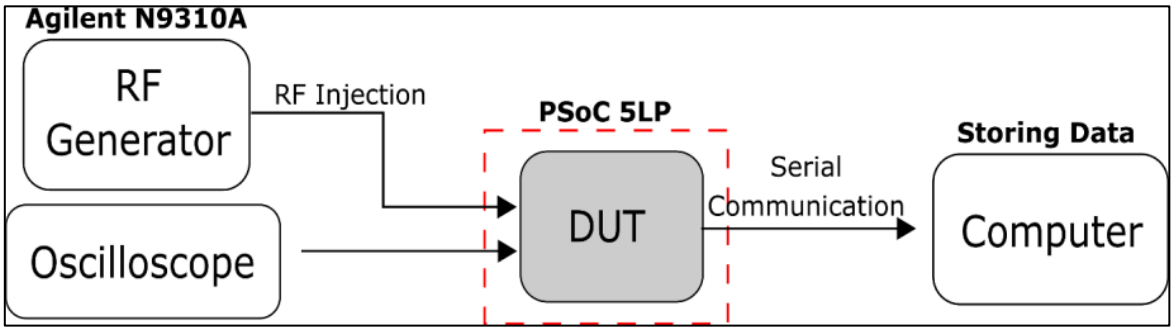
Disturbance injections were performed as suggested by IEC 62132-1 and IEC62132-4. The standard requires for signal injections between 150 kHz up to 1 GHz, with 10 to 17dBm power for microcontrollers and memories, and with 20 to 27 dBm power for ABS sensor and others devices, as is shown in table 5.1. Experiments were performed at frequencies of 150,

300, 600 kHz and 1.2 MHz with 10, 17, 20 and 27 dBm for each frequency, based on the frequency steps according table 5.1. From the frequency of 150 kHz to 1MHz, the increment was 100 kHz every 6 seconds. From the frequency 1 MHz to 100 MHz, the increment was 1 MHz every 3 seconds and from the frequency 100 MHz to 1 GHz, the increment was 10 MHz every 3 seconds to complete the scan of the entire standard from 150 to 1 GHz.

At each failure occurrence, the system sends a log with error information to the computer via the UART-RS232 interface, which sends a log to obtain digital signal information of 10 wordsof the 740 ksps SAR converter, and the value of the 74 ksps SAR and ΣΔ ADC, plus the temporal voter value and the main voter value(system output).The program developed by González (2018), sends an “alive” message showing the system status every 60 seconds if no error is reported.

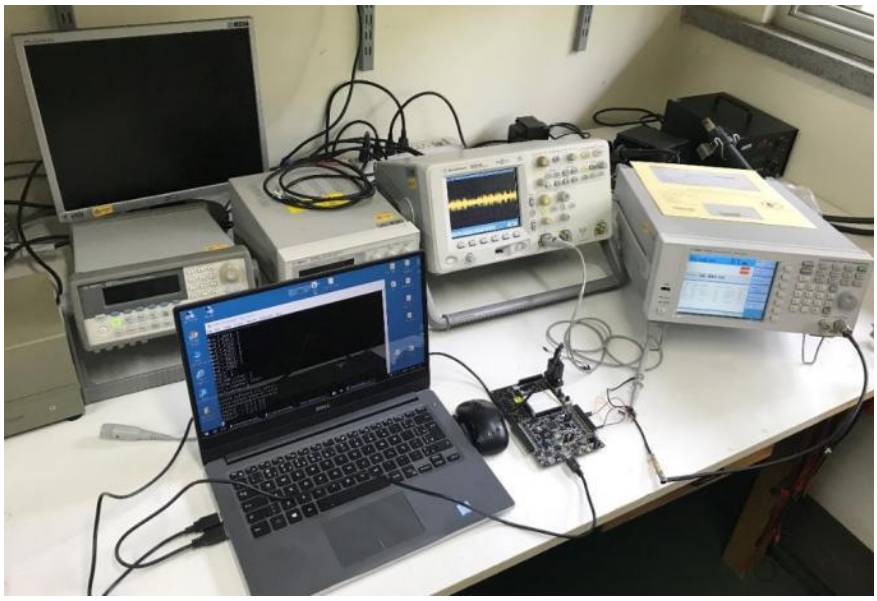
Figure 5.8 depicts the test setup for direct power injection, while Figure 5.9 shows the actual test setup at the lab.

Figure 5.8 – Block diagram of test setup



Source: own authorship, 2018.

Figure 5.9 – Test setup and equipment



Source: Own Authorship (2019)

6. RESULTS AND DISCUSSIONS

In this section, the aim is to present the impact of electromagnetic interference (EMI) on the three different converters of the Cypress Semiconductor Programmable SoC (System-on-Chip) system (PSoC 5LP) PSoC (CYPRESS SEMICONDUCTOR, 2013), and discuss the effectiveness of the adopted methodology, which has been based in TMR and diversity.

In the first performed test, the converters input were connected to the GND, as depicted in Figure 6.1, to verify the behavior of the converters and the voters while no EMI signal is injected. This test showed that the system was working properly so the EMI injection phase could start.

6.1 Injecting disturbance in VREF

For the continuation of the tests, the following parameters were used, as shown in figure 6.1:

- Converter inputs have been connected to GND.

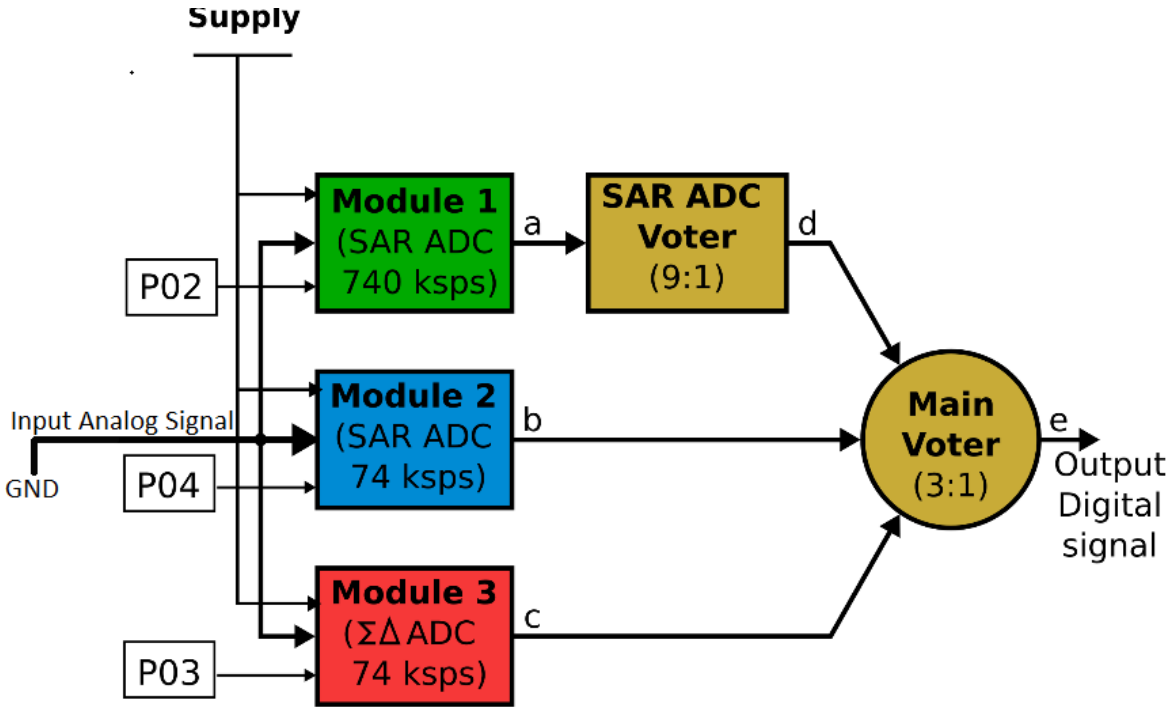
-It was used internal generated VREF - 1.024 V and injected the disturbance into this VREF, by means of the external access pin.

-For SAR MOD_01 it was used P0[2] to inject the disturbance.

-For SAR MOD_02 it was used P0[4] to inject the disturbance.

-For the SIGMA DELTA MOD_03 it was used P0[3] to inject the disturbance.

Figure 6.1 – Parameters and pins used to disturbance injection



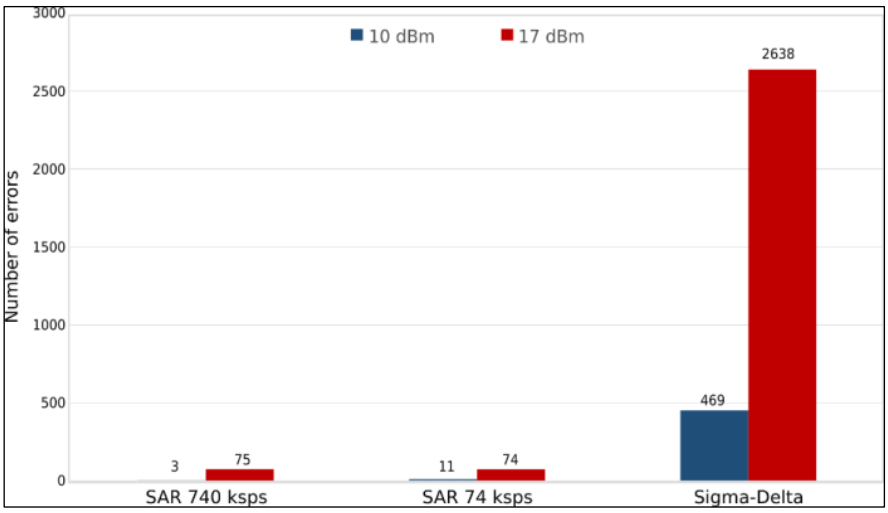
Source: Own Authorship (2019)

The obtained results were tabulated and shown in Appendix B. Figure 6.2 shows the number of conversion errors in each converter, considering the injected power of 10 and 17 dBm in the frequency range 150 kHz to 1 GHz. One can see that the Sigma-Delta is the most sensitive converter, in this case, and several errors occur for the signal power of 17dBm.

Studying the PSoC manual one can interpret why the SAR converter presented less errors that the ΣΔ ADC. Both the SAR ADC and the ΣΔ ADC have internal reference voltages, which can be filtered or not. A bypass capacitor is a capacitor that shorts AC signals to ground (in this case, at board level). In this way, AC noises that may be present on a DC signal are reduced, resulting in a cleaner DC signal.

Since the test was conducted with the default (on-chip and on-board) configurations of the PSoC, we opted to perform the tests with the condition in which the SAR ADC presents an internal reference voltage with an external bypass capacitor. The ΣΔ, on the other hand, uses an internal reference voltage (generated on-chip) that is buffered, but unfiltered. This also allows reproducing a condition in which, due to board design issues, a given converter is made more susceptible and, in this case the DTMR system may be able to mitigate.

Figure 6.2 – Conversion errors for EMI injected at VREF and input = 0 V.



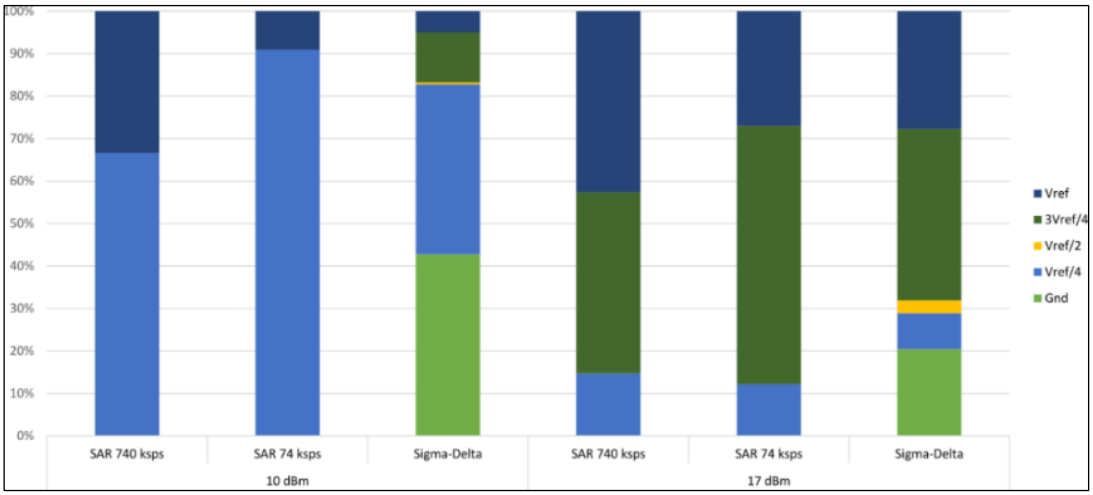
Source: Own Authorship (2019)

The next part of the tests consisted of connecting the converter inputs to the voltages Vin = VREF, Vin = ¾ VREF, Vin = ½ VREF and Vin = ¼ VREF and injecting RF into the reference voltage of these converters.

In figure 6.3, it is possible to see the errors percentage of each converter for the two power levels and different DC values of the analog input. The vulnerability of the Sigma delta converter is great when its analog input is GND for both 10dbm and 17dbm power.

For the 17dBm power, a more constant distribution of the occurrence of errors can be observed among the different levels of input signal.

Figure 6.3 – Conversion errors percent as function of input DC level

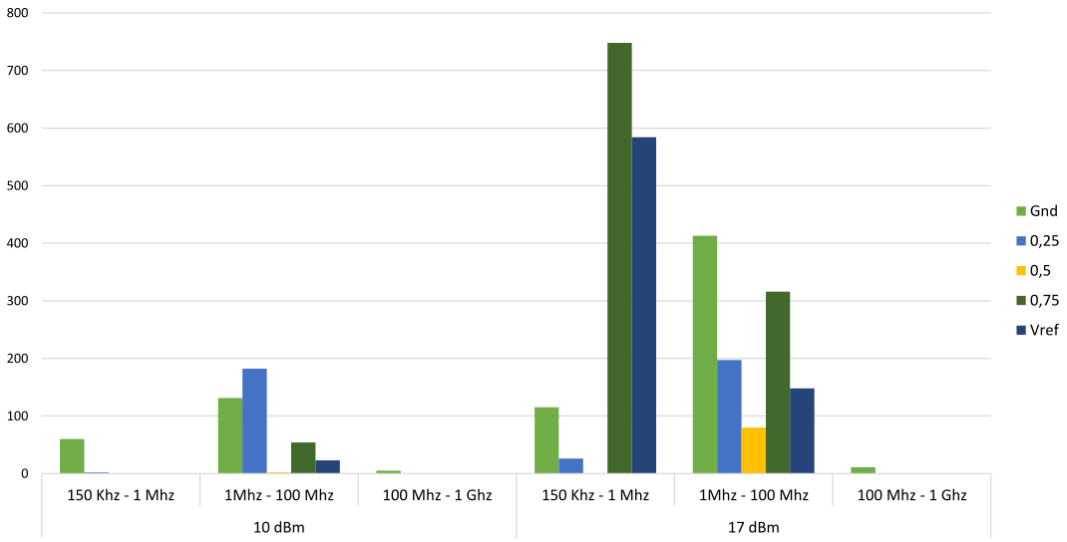


Source: Own Authorship (2019)

The ΣΔ ADC was more susceptible and that is why its results are detailed and highlighted in the figures below.

Considering that ΣΔ ADC presented a higher percentage of conversion errors. This figure 6.4 aims to present these events in detail. The graph clearly shows an accentuated amount of errors in the condition of 17 dBm compared to 10 dBm. Another analysis that this graph intends to show is that the frequency range which is most affected by errors is between 150 khz and 100 Mhz.

Figure 6.4 – ΣΔ ADC conversion errors number as function of input DC level in different frequencies range

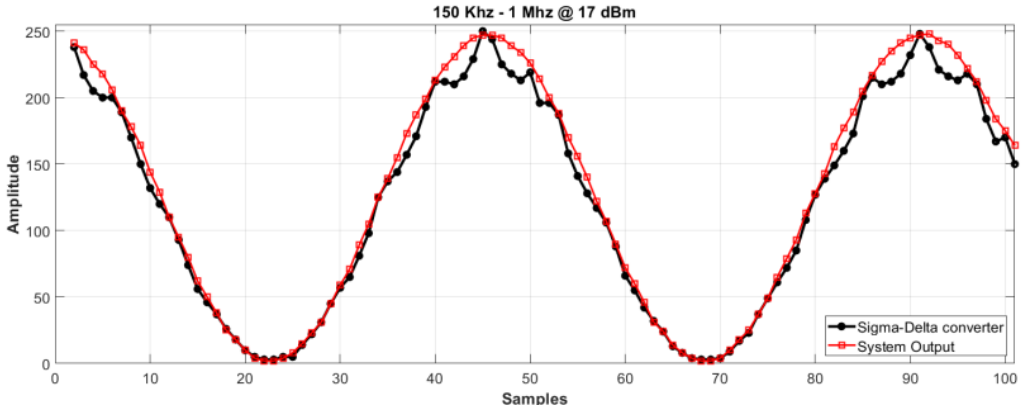


Source: Own Authorship (2019)

For the frequency ranges in which the converter showed increased sensitivity the sine wave test signal was used as input, in order to generate samples within most of the full scale range of the converter.

Figure 6.5, shows the result for the frequency range of 150 kHz to 1 MHz @ 17dBm of input power. This figure shows an example of a sine wave conversion. It is possible to see the degraded signal of the ΣΔ converter (with higher linearity loss at higher values – corroborating the data of Figure 6.4). It is also possible to see that, in this case, as the other converters perform well, the system output is able to deliver a good signal. This is thanking to the diversity redundancy scheme.

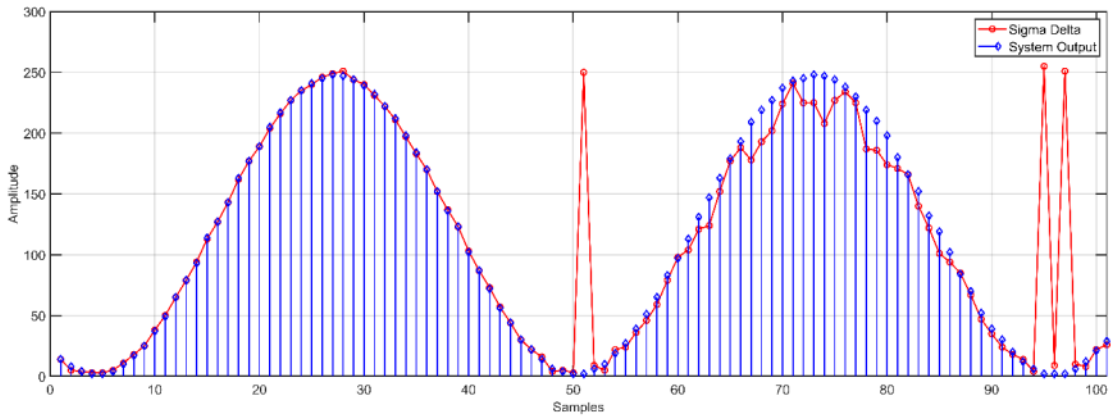
Figure 6.5 – ΣΔ conversion errors and healthy signal at system output.



Source: Own Authorship (2019)

Figure 6.6show another example, for frequency range of 150 kHz to 1 MHz @ 17dBm of input power. In some situations when the input signal is close to GND, the ΣΔ output signal fluctuates to digital values of 255, identifying the worst possible case of conversion. As in the previous example, the redundant system is able to mitigate this effect, resulting in a non-degraded signal at the output.

Figure 6.6 – Another example of ΣΔ conversion errors and healthy signal at system output.



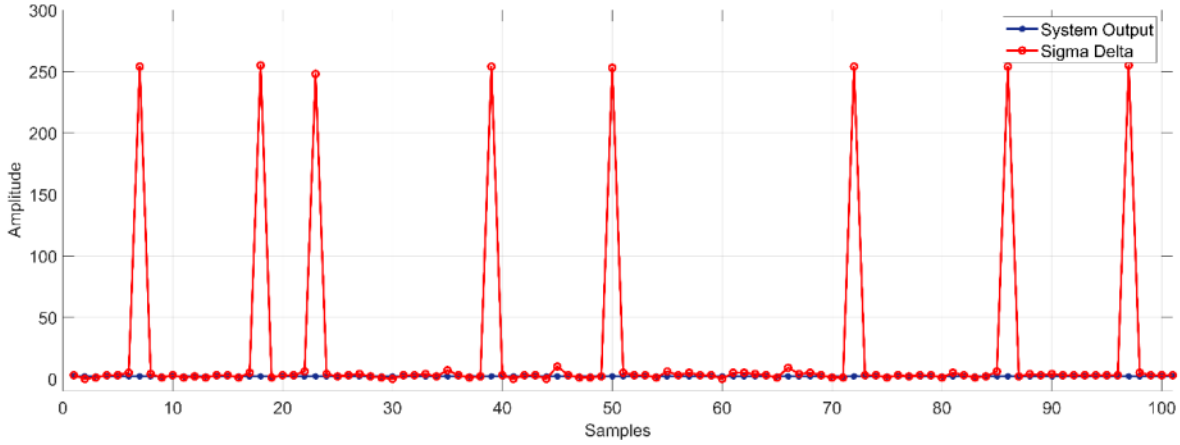
Source: Own Authorship (2019)

As shown in figures 6.5 and 6.6, even though the ΣΔ converter had conversion errors, the system output signal was intact. This proves the correct functionality of the Triple Modular Redundancy (TMR). Disturbance injections were performed in one converter at a time. Even so, it is believed that the system can function satisfactorily when two or more converters are exposed to electromagnetic interference, at the same time. For reasons such as latency, signal delay and clock frequency, converters are unlikely to experience conversion errors at the same time. Another reason that could differentiate the times of eventual conversion errors would be the frequency range in which each converter would be more susceptible. For future work, it would be important to carry out tests by injecting RF signal into two converters at the same time.

In the event that some conversion errors would happen at the same time, it could still be said that the TMR system would function correctly, as this would mitigate the errors of the moments when only one converter would be showing conversion failures.

Figure 6.7 shows the result for the test in which the input signal is Vin = 0 V (GND), for the ΣΔ converter. It can be seen that this pattern repeats along the experiment.

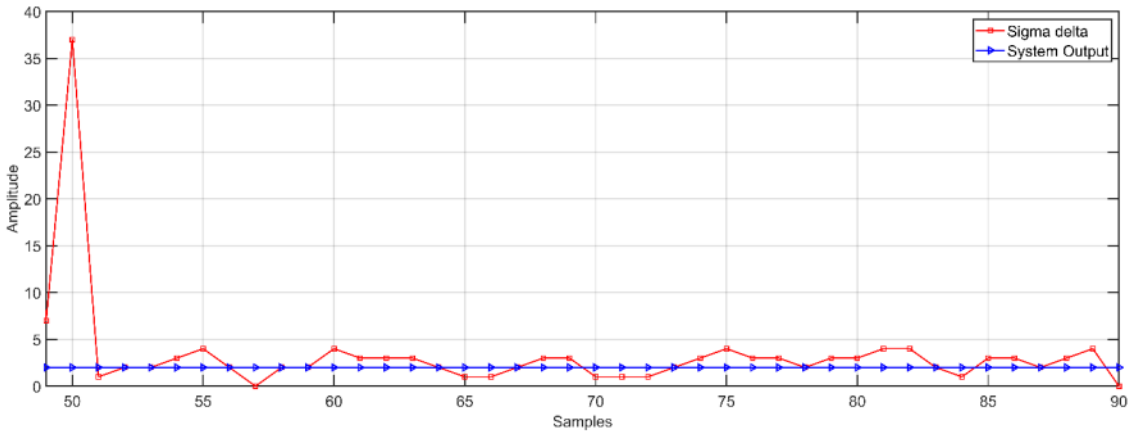
Figure 6.7 – ΣΔconversion errors – critical level



Source: Own Authorship (2019)

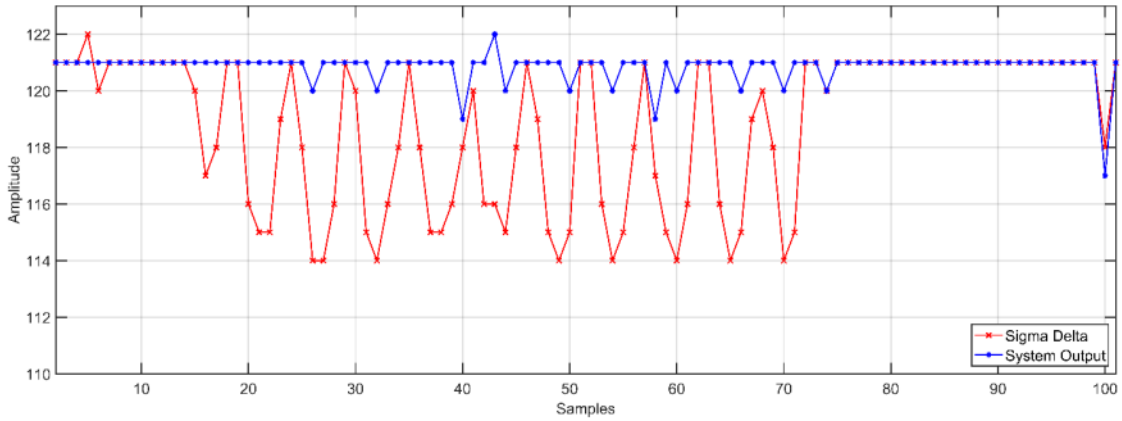
Corroborating with figures 6.6 and 6.7, where is shown the worst case of conversion, occurs when the input signal is close to GND, the ΣΔ output signal fluctuates to digital values of 255, figure 6.8 aims to show one of these cases in an enlarged way. The detailing of this occurrence brings the idea that future works could start from this point. It is believed that understanding the reason for conversion errors (in their worst case) to happen in this situation may be key to the development of technologies immune to the effects of electromagnetic interference. Figure 6.9 shows the variation of the digital value when the input is at the midscale. This oscillation is notable but not as critical when the input signal is in GND.

Figure 6.8 – Detailed visualization of the disturbance in the ΣΔ converter



Source: Own Authorship (2019)

Figure 6.9 – ΣΔ conversion errors with the input at midscale

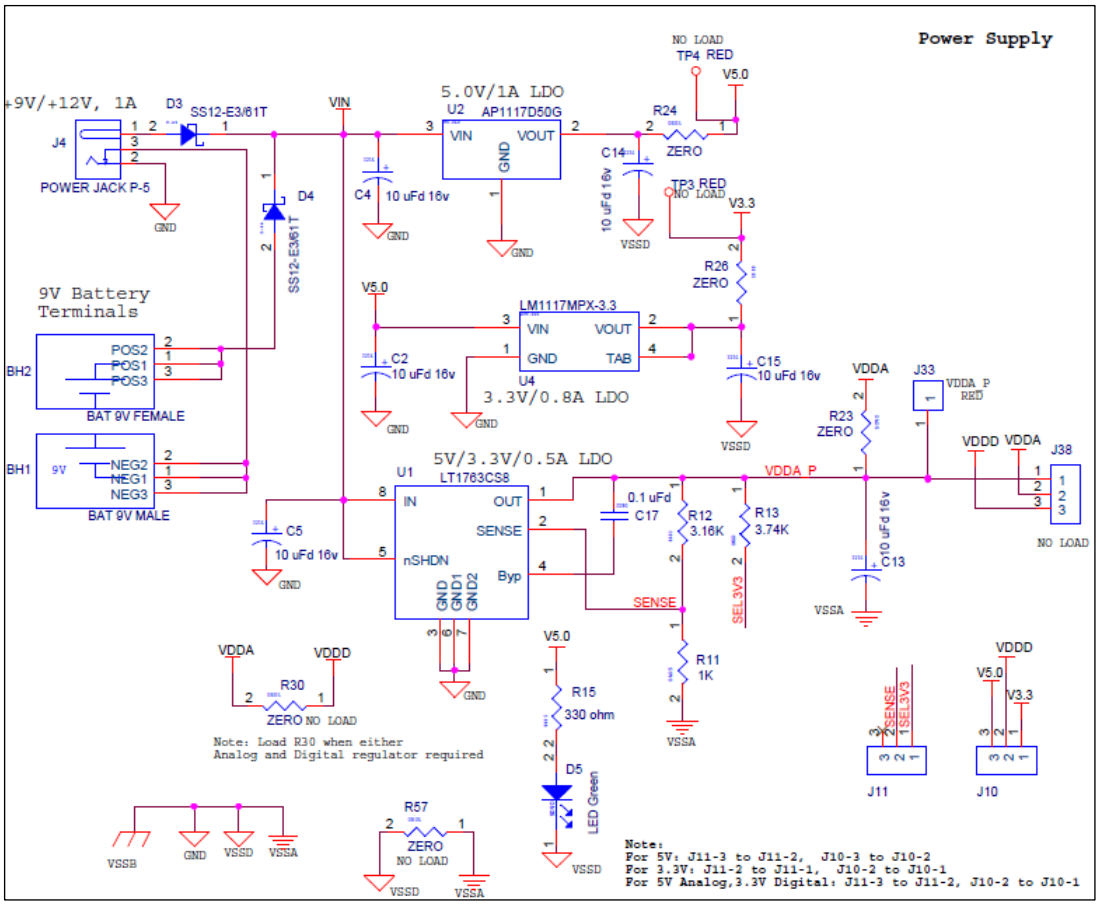


Source: Own Authorship (2019)

6.2 Injecting disturbance on VDDA (analog power supply):

The last part of the tests consisted of injecting interference on VDDA and verifies the behavior of the converters and the voters. To make this experience possible, the PSoC 5LP features had been studied. Therefore, it can be affirmed that PSoC 5LP devices have separate external analog and digital supply pins, labeled VDDA and VDDD, respectively. VDDA is the supply for all analog peripherals and analog core regulator. In figure 6.10, the PSoC development board power supply circuit and the VDDA possible points to inject EMI may be observed.

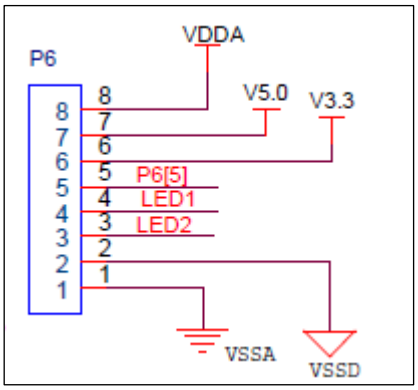
Figure 6.10 – VDDA pin to inject EMI using DPI technique



Source: PSoC 5LP schematic (CYPRESS, 2013, p. 01)

For signal injection and carrying out this test, connector P6 - pin 8 was chosen, since this is a connector dedicated to input and output signals. The figure 6.11 shows the schematic view of this connector.

Figure 6.11 – VDDA pin to EMI DPI



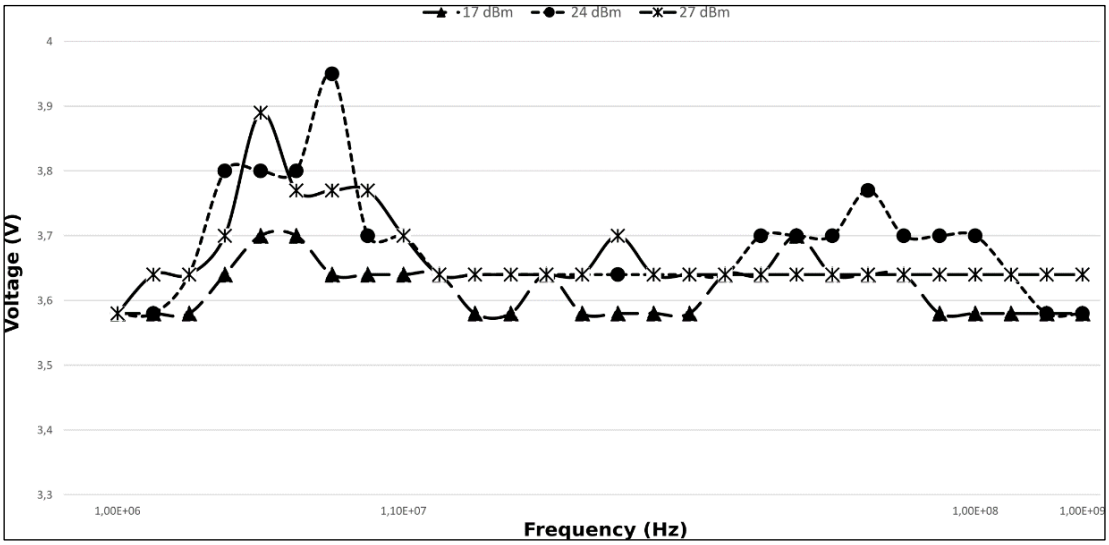
Source: PSoC 5LP schematic (CYPRESS, 2013, p. 01)

Based on what was observed in the previous tests, where 17 dBm signals had a greater number of conversion failures than 10 dBm signals, it was defined that the disturbances injections would be 17, 24 and 27 dBm (as table 5.2) in the frequency range from 150 kHz to 1 GHz. With this test it was expected to verify conversion errors and from these results, it was imagined to draw a parallel with what was observed in the other tests.

However, no conversion errors occurred. On the other hand, voltage fluctuations were noticed and the results obtained were tabulated and shown in Appendix C. As for VDDA, the initial value – without EMI DPI – was 3.58 VDC.

Figure 6.12 illustrates the voltage fluctuation when the VDDA was exposed to frequency range from 150 kHz to 1 GHz.

Figure 6.12 – VDDA fluctuation when exposed to 17, 24 and 27 dBm EMI DPI



Source: Own Authorship (2019)

Even if the system did not present any conversion error, it is clear that when performing EMI DPI on the VDDA source, it presents considerable variations. This encourages us to think, and suggest further research, about the effects that these interferences / fluctuations would have on converters over time.

7. CONCLUSION

The work developed in this Master's Dissertation aimed to evaluate the impact of directly injected electromagnetic interference (EMI) on three different converters of the Cypress Semiconductor programmable SoC system (PSoC 5 LP).

Some techniques to protect electronic systems against EMI have been studied and the Design Diversity Triple Modular Redundancy (DTMR), a system-level technique, was applied in this work. TMR and diversity are mainly used in critical applications in which an error can result in injury, threat for life or loss of high investment (CHENET, 2015). Taking into account the high risk of electromagnetic interference causing degradation of electronic systems reliability and further wide use of TMR techniques and diversity in critical applications, this work has adopted a scheme based on these mitigation techniques for implementing a data acquisition system (DAS). The objectives with this DAS are to observe the behavior of data converters in face of direct radio frequency (RF) power injection in their reference voltage and supply voltage pins, aiming to evaluate the effectiveness of a system based on TMR and spatial-temporal diversity against EMI effects.

To perform the Direct Power Injection (DPI) the technique, the IEC standards 62132-4 (IEC, 2006) and 62132-1 (IEC, 2006) were used as reference and adapted for testing this specific application.

With the noise injection performed at the reference voltage of the converters it can be concluded that ΣΔ ADCis more susceptible to electromagnetic interference than SAR converters. The ΣΔ ADC converter presented conversion errors for practically all frequency ranges when exposed to noise power of 17dBm. While SAR converters showed conversion errors in the 1 MHz 100 MHz frequency range when exposed to electromagnetic interference with 17dBm power. Probably, this reduced number of conversion errors for SAR converters compared with the ΣΔ ADC is due to the default board and intrachip configurations of the employed development kit (regarding the ADCs voltage references), which consists on an internal reference voltage with an external bypass capacitor for SAR converters.

Even in cases in which the converted signal of the ΣΔ converter was degraded, but with the other converters performing well, the system output is able to deliver a good signal. The redundant system is able to mitigate this effect, resulting in a non-degraded signal at the output.

Another relevant fact, considering the performed studies, is that the SAR clock frequency is 18 MHz and the ΣΔ clock is 6 MHz, which may explain why most conversion errors occurred in the frequency range of 1 to 100 MHz of the injected noise signal.

Following the tests, EMI was injected on the analog power supply (VDDA) verifying the behavior of the converters and the voters. For this test no conversion errors occurred. This is due to the good Power Supply Rejection Ratio (PSRR) of the Converters. However, considerable voltage fluctuations (DC) were noticed, probably due to a rectifying effect.

Considering the test conditions of this work, the PSoC configuration and board design issues of the employed kit, it can be concluded that the ΣΔ ADC converter is more susceptible to EMI induced failure than the SAR ADCs. However, in practical field applications, sources of electromagnetic interference are diverse and random and, in other conditions, the result concerning the susceptibility of the converters may be different. For example, according to Gonzáles (2018), the SAR converter architecture was more susceptible when the MS-DTMR system was evaluated under total ionizing dose (TID) effects. Therefore, it can be concluded that the DAS scheme based on TMR and diversity presents improved reliability when considering the diverse environmental degradation sources.

Future works may be focused on evaluating the influence of the converter architecture on its reliability to EMI, with possible design mitigation strategies. Additionally evaluating the next generation device PSoC 6 is also on the horizon of ongoing works.

REFERENCES

ANATEL. **“Regulamento de Avaliação da Conformidade e de Homologação de Produtos para Telecomunicações. ”**Published in 2019, 14 f. Available in: https://www.anatel.gov.br/legislacao/resolucoes/2019/1350-resolucao-715.

ATMEL CORPORATION. **AVR127: Understanding ADC Parameters.**1600 Technology Drive, San Jose, CA 95110 USA, 2016, 24 f. Available in: http://ww1.microchip.com/downloads/en/AppNotes/atmel-8456-8-and-32-bit-avr-microcontrollers-avr127-understanding-adc-parameters_application-note.pdf.

AGUILERA, C. J. G. **Avaliação de Conversores AD sob Efeitos de Radiação e Mitigação Utilizando Redundância com Diversidade.** 2018. Master Thesis (Master in Microelectronics) – Programa de Pós-Graduação em Microeletrônica, Universidade Federal do Rio Grande do Sul – UFRGS, 2018.

CHENET, C. P. et al. **“Exploring Design Diversity Redundancy to Improve Resilience in Mixed-Signal Systems.”** Microelectronics Reliability, Elsevier BV, v. 55, n. 12, p. 2833–2844,dec 2015.

COUNCIL OF EUROPEAN UNION. **“Directive 2014/30/EU - on the harmonization of the laws of the Member States relating to electromagnetic compatibility.”** Published in 2014, 28 f. Official Journal of the European Union.

CYPRESS SEMICONDUCTOR. **PSoC 5LP ADC Successive Approximation Register.** San Jose, 2015, 28f. Available in: https://www.cypress.com/file/179601/download.

CYPRESS SEMICONDUCTOR. **PSoC 5LP Architecture Technical Reference Manual.** San Jose, 2017, 51f. Available in: https://www.cypress.com/file/123561/download.

CYPRESS SEMICONDUCTOR. **PSoC 5LP Delta Sigma Analog to Digital Converter.**San Jose, 2017, 452f. Available in: https://www.cypress.com/file/400466/download.

CYPRESS SEMICONDUCTOR. **PSoC 5LP Development Kit Guide.** San Jose, 2013b, 58 f. Available in: http://www.cypress.com/file/45276/download.

CYPRESS SEMICONDUCTOR. **PSoC 5LP Development Kit - Quick Start Guide.** San J. 2013, Available in: http://www.cypress.com/file/45271/download.

CYPRESS SEMICONDUCTOR. **PSoC 5LP Release Notes.** San Jose, 2013b, 2f. Available in: http://www.cypress.com/file/45266/download.

CYPRESS SEMICONDUCTOR. **PSoC 5LP Schematic and Data Sheet.** San Jose, 2013b, 2 f. Available in: http://www.cypress.com/documentation/development-kitsboards/ cy8ckit-050psoc-5lp-development-kit.

DAVIES, D.; WAKERLY, J. F. **Synchronization and matching in redundant systems.** IEEE
Transactions on Computers, vol. 27, no 6, p. 531–539, 1978.

DORNELAS, H. U. **Low Power SAR Analog-to-Digital Converter for Internet-of-Things RF Receivers.**2018. Master Thesis (Master in Microelectronics) – Programa de Pós-Graduação em Microeletrônica, Universidade Federal do Rio Grande do Sul – UFRGS, 2018.

FIORI, F. **Susceptibility of CMOS Voltage Comparators to Radio Frequency Interference.**IEEE Transactions On Electromagnetic Compatibility, Vol. 54, No. 2, April 2012.

FLORES, M. da G. C. C. **Teste Embarcado de Conversores Analógico-Digitais.** Dissertation (Master) — Universidade Federal do Rio Grande do Sul, Porto Alegre, Brasil, 2003.

FRÉMONT, H. et al. **"A Methodological Approach for Predictive Reliability: Practical Case Studies."** Microelectronics Reliability, Elsevier BV, v. 52, n. 12, p. 3035–3042, sep 2012.

GONZÁLEZ, C. et al. **Reducing Soft Error Rate of SoCs Analog-to-DigitalInterfaces with Design Diversity Redundancy.** Instrumentation Measurement Magazine, IEEE, [S.l.], v.8, n.5, p.44 – 54, Dec. 2005.

GONZÁLEZ, C. et al. **TID Effects on a Data Acquisition System With Design Diversity Redundancy.**IEEE Transactions On Nuclear Science, IEEE, v.15, n.1, Jan. 2018.

GLOBAL MARKET INSIGHTS. **Electromagnetic Interference (EMI) Shielding Materials Market Size.** Available in <https://www.gminsights.com/industry-analysis/electromagneticinterference-emi-shielding-materials-market. Access in 07/07/2018.

HANADA, E. and KUDOU T. **"Managing the Electromagnetic Environment of Hospital IoT Systems"**, 2018.

HAYASHI, Y.; VERBAUWHEDE, I. and RADASKY, W. A.**"Introduction to EM Information Security for IoT devices"**, 2018.

INTERNATIONAL ELECTROTECHNICAL COMMISSION. **IEC 61000-1-2, Electromagnetic compatibility (EMC) - Part 1-2: General - Methodology for the achievement of functional safety of electrical and electronic systems including equipment with regard to electromagnetic phenomena**, December 2016.

INTERNATIONAL ELECTROTECHNICAL COMMISSION. **IEC 62132-1, Integrated Circuits – Measurement of Electromagnetic Immunity, 150 kHz to 1 GHz – Part 1: General Conditions and Definitions**, ed. 1.0, January 2006.

INTERNATIONAL ELECTROTECHNICAL COMMISSION. **IEC 62132-4, Integrated circuits – Measurement of Electromagnetic Immunity, 150 kHz to 1 GHz – Part 4: Direct RF Power Injection Method**, ed. 1.0, February 2006.

JOVIC´, O. **"Susceptibility of ICs to Conducted Electromagnetic Interference"**, 2010**.**

KENNEDY, S. at al.**Susceptibility of flash ADCs to electromagnetic interference.** Microelectronics Reliability, Elsevier BV, v. 81, p. 218–225, dec 2018.

KESTER, W. **“ADC Architectures III: Sigma-Delta ADC Basics”**, 2009**.**

KESTER, W. **“ADC Architectures II: Successive Approximation ADCs”**, 2009**.**

KULARATNA, N. **Electronic Circuit Design: From Concept to Implementation.**CRC Press; 1 edition. June, 2008. ISBN-13: 978-0849376177.

KUMAR, P. S.; NARAYANA, D. L.; TEJESVI, V. R.; CHANDRASEN, M. K. **“FPGA Based Sigma-Delta Analog To Digital Converter For Power Sensing,”** International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT) – 2016.

LANOT, A. J. C. **Estudo de Falhas Transientes e Técnicas de Tolerância a Falhas em Conversores de Dados do Tipo SAR Baseados Em Redistribuição de Carga.** 2014. Master Thesis (Master in Electrical Enginnering) – Programa de Pós-Graduação em Engenharia Elétrica, Universidade Federal do Rio Grande do Sul – UFRGS, 2014.

LAVARDA, A.; DEUTSCHMANN, B. **Direct power injection (DPI) simulation framework and post processing.** IEEE, International Symposium on Electromagnetic Compatibility (EMC), 2015.

MALANDRUCCOLO, V et al. **“A New Built-In Screening Methodology for Successive Approximation Register Analog to Digital Converters.”** Microelectronics Reliability, Elsevier BV, v. 50, p. 1750–1757, dec 2010.

MARDIGUIAN, M. **“EMC at the Integrated Circuit Level a Most Audacious Challenge,” 4th International Workshop on Electromagnetic Compatibility of Integrated Circuits, EMC Compo 2004.**

MUSUMECI, D. and FIORI, F. “**Susceptibility of a Sigma-Delta Converter to EMI”, 20th tnt. Zurich Symposium on EMC, Zurich 2009.**

NASA. **“Electronic Systems Failures and Anomalies Attributed to Electromagnetic Interference” Washington, United States, 1995.** Available in: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/19960009442.pdf.

OVERBR. **Blindagem eletromagnética a Ford trabalha nisso.** Available in <https://overbr.com.br/artigos/blindagem-eletromagnetica-a-ford-trabalha-nisso>. Access in 07/07/2018 – Published in 03/01/2018.

PAUL, C. **Introduction to Electromagnetic Compatibility.**Wiley Interscience, 2006. ISBN-13:978-0471755005.

PELGROM, M. **Analog-to-Digital Conversion.** Springer Netherlands, 2010. ISBN 9789048188888.Disponível: <https://books.google.com.br/books?id=xU5IXpif7bMC>.

PRESTES, D. P. **Plataforma Para Injeção De Ruído Eletromagnético Conduzido Em Circuitos Integrados. 2010.** Master Thesis(Master in Electric Enginnering), Pontifícia Universidade Católica do Rio Grande do Sul – PUC, 2010.

RAMDANI, M.; SICARDI, E.; DHIA, S. B. and CATRYSSE, J. **“Towards an EMC Roadmap for Integrated Circuits”**, 2008.

RAPUANO, S. et al. **ADC parameters and characteristics.** InstrumentationMeasurement Magazine, IEEE, [S.l.], v.8, n.5, p.44 – 54, Dec. 2005.

MALOBERTI, F. **Data Converters.** Springer, 2007. ISBN-13: 978-0-387-32485-2.

MARCO, L. **Interferências Eletromagnéticas, ruídos podem interferir na transmissão de informação.** Available in <https://www.reparacaoautomotiva.com.br/single-post/2018/03/07/Interfer%C3%AAncias-Eletromagn%C3%A9ticas-ru%C3%ADdos-podem-interferir-na-transmiss%C3%A3o-de-informa%C3%A7%C3%A3o>. REPARAÇÃO AUTOMOTIVA. Access in 07/11/2019. Published in 07/03/2018.

RESEARCH AND MARKETS. **Electromagnetic Compatibility (EMC) Shielding and Test Equipment Market by Type, Application, and Geography** - Forecast to 2020,

October 2015 Available in <https://www.researchandmarkets.com/research/np563c/electromagnetic>. Access in 09/07/2018.

RF GLOBALNET. **5 Trends To Watch In EMC Engineering.** Available in <https://www.rfglobalnet.com/doc/trends-to-watch-in-emc-engineering-0001>. Access in 07/09/2018 – Published in 07/25/2012.

WDD – WIRELESS DESIGN & DEVELOPMENT. **EMC Trends and Solutions to Reduce or Eliminate EMI.**<https://www.wirelessdesignmag.com/blog/2015/04/emc-trends-andsolutions-reduce-or-eliminate-emi>. Access 07/09/2018 – Published 01/04/2015.

WIKLUNDH, K. and STENUMGAARD, P. **"EMC Challenges for the Internet of Things".** Proc. of the 2017 International Symposium on Electromagnetic Compatibility - EMC EUROPE 2017, Angers, France, September 4-8, 2017.

WAES, J.; VANKEIRSBILCK, J.; PISSORT D. and BOYDENS, J. **"Electromagnetic Interference in the Internet of Things: an automotive insight"**. Proc. XXVI International Scientific Conference Electronics - ET2017, September 13 - 15, 2017, Sozopol, Bulgaria.

APPENDIX A – INFRASTRUCTURE REQUIRED TO PERFORM THE TESTSACCORDING IEC62132-1 AND IEC62132-4

IEC 62132-4 - Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 4: Direct RF power injection method	Infrastructure	Function			UNISINOS/CIENTEC/UFRGS
Measurement Basics	RF Generator	Provide RF Disturbance	2 w	OK	
Measurement Basics	RF Amplifier	Amplify RF Disturbance		150 W	
Measurement Basics	RF Power Meters	Measure actual forward power injected in to the DUT		OK	
Measurement Basics	Directional Coupler	Measure actual forward power injected in to the DUT		OK	
Measurement Basics	Decoupling Network	Prevent DC supply		VER	
Measurement Basics	Oscilloscope with Pass/fail function	To monitor the behaviour of the DUT	ok	ok	
Measurement Basics	Capacitor 6,8 nF - specified IEC 61697-4	DC block	ok		
Measurement Basics	Resistor 0 ohm or up 100 ohms	Current Limitation	ok		
Test Condition	5W (37 dBm)	Maximum power level of a CW - unprotected IC-PIN externally		OK	
Test Condition	AM signal of 1 kHz 80%	Testing the DUT		OK	
Test Condition		Testing the DUT		OK	
Test Equipment	RF Power Source(RF Generator/Amplifier)	Provide Sufficient power(10-50 W)		OK	
Test Equipment	Impedance of Power Source 50 ohms	Recommend VSWR <1,2 absord reflected waves		OK	
Test Equipment	Coaxial Cables		ok	OK	
Test Equipment	RF Conectors		ok	OK	
	Ponta de Provas	Inject RF signal			

APPENDIX B – ERRORS DATAS GATHERED WITH DIRECT POWER INJECTION ON VREF

DIRECT POWER INJECTION ON VREF						
Input	Errors - GND					
Power	10 dBm			17 dBm		
Frequency	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz
M1	0	0	0	0	0	0
M2	0	0	0	0	0	0
M3	60	131	5	115	413	11

Input	Errors - 0,256 V					
Power	10 dBm			17 dBm		
Frequency	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz
M1	0	2	0	0	11	0
M2	0	10	0	0	9	0
M3	2	182	0	26	197	0

Input	Errors - 0,51 V					
Power	10 dBm			17 dBm		
Frequency	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz
M1	0	0	0	0	0	0
M2	0	0	0	0	0	0
M3	0	2	0	0	80	0

Input	Errors - 0,76 V					
Power	10 dBm			17 dBm		
Frequency	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz
M1	0	0	0	0	32	0
M2	0	0	0	0	45	0
M3	0	64	0	748	316	0

Input	Errors - 1,024 V					
Power	10 dBm			17 dBm		
Frequency	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz
M1	0	1	0	0	32	0
M2	0	1	0	0	20	0
M3	0	23	0	584	148	0

Input	Errors - Seno					
Power	10 dBm			17 dBm		
Frequency	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz	150 kHz - 1 MHz	1 MHz - 100 MHz	100 MHz - 1 GHz
M1	não feito	não feito	não feito	0	0	0
M2	não feito	não feito	não feito	0	0	0
M3	não feito	não feito	não feito	665	762	0

APPENDIX C – VOLTAGE FLUCTUATION AFTER DIRECT POWER INJECTION ON VDDA

DIRECT POWER INJECTION ON VDDA								
Initial Parameters			Initial Parameters			Initial Parameters		
Power dBm	17		Power dBm	24		Power dBm	27	
Voltage (V)	3,58		Voltage (V)	3,58		Voltage (V)	3,58	
Frequency	Voltage (V)		Frequency	Voltage (V)		Frequency	Voltage (V)	
150k	3,58		150k	3,58		1M	3,58	
6 M	3,7		1M	3,58		2M	3,64	
8 M	3,64		3M	3,64		5M	3,7	
11 M	3,64		5M	3,8		6M	3,89	
15 M	3,58		8M	3,95		7M	3,77	
20 M	3,64		9M	3,7		11M	3,7	
21 M	3,58		13M	3,64		18M	3,64	
48 M	3,64		31M	3,64		23M	3,7	
60 M	3,7		50M	3,7		25M	3,64	
62 M	3,64		75M	3,77		100M	3,64	
90 M	3,58		80M	3,7		200M	3,64	
100 M	3,58		130M	3,64		500M	3,64	
500 M	3,58		160M	3,58		750M	3,64	
1 G	3,58		1G	3,58		1G	3,64	