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Design of a SAW-Less CMOS Discrete-Time Receiver for Bluetooth Low Energy

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To my wife Suse.

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Design of a SAW-Less CMOS Discrete-Time Receiver for Bluetooth Low Energy

ABSTRACT

Personal mobile communications and the Internet of Things increased the complexity of radio frequency front-end design, in particular due to the requirements for energy autonomy over long periods, which translates into very hard low-power constraints. Bluetooth Low Energy is a new version of the Bluetooth Standard specified to answer to this recent market need. In the receiver part of the design, discrete-time implementations appear as a new hardly explored possibility to reduce power, benefiting from CMOS technology scaling and adding flexibility to the front-end design. Integration is another important point and traditionally external parts of the design like filters and matching networks, need to be part of the integrated circuit as much as possible. The present work implements a surface acoustic wave (SAW)-less fully discrete-time front-end receiver for Bluetooth Low Energy. The design uses band-pass switched capacitor passive filters recently introduced and a careful choice of sampling rates and anti-aliasing filters to develop a SAW-less ultra low power receiver architecture with state-of-the-art performance. Architectural and block-level strategies associated with a discrete-time design are explained in detail in a top-down approach. The design is implemented in TSMC 28nm Low Power CMOS. Measurement results show a performance of 6.5 dB noise figure including internal matching network and switch, and -19 dBm IIP3 for a power cost of 2.75 mW.

Keywords: CMOS, Bluetooth Low Energy, discrete-time receiver, switched capacitor.

Projeto de um receptor em tempo discreto CMOS para *Bluetooth Low Energy* sem filtro externo de seleção de banda

RESUMO

Comunicações móveis e a *Internet das Coisas* adicionaram complexidade ao projeto de circuitos de rádio frequência, principalmente devido à necessidade de autonomia de bateria por longos períodos. Em consequência, ocasionando requisitos rígidos de baixa potência. *Bluetooth Low Energy* é uma nova versão do protocolo *Bluetooth* destinada a atender esta recente demanda de Mercado. No projeto da parte analógica do receptor, novas técnicas de projeto em tempo discreto aparecem como uma possibilidade de reduzir o consumo de potência pouco explorada, que se beneficia da modernização das tecnologias CMOS e adiciona flexibilidade ao projeto do receptor. Integração é outro ponto importante e componentes externos ao receptor como filtros e redes de casamento agora necessitam fazer parte do circuito integrado de forma a reduzir os custos. O presente trabalho se insere neste contexto, com o desenvolvimento de um receptor para *Bluetooth Low Energy* totalmente em tempo discreto e sem filtros externos. O projeto utiliza filtros passa-faixas passivos implementados usando capacitores chaveados e escolha criteriosa de taxas de amostragem e filtros *anti-aliasing* para implementar uma arquitetura de tempo discreto sem filtros externos de baixíssimo consumo e com desempenho equiparável ao estado da arte em receptores para *Bluetooth Low Energy*. A arquitetura inovadora e as técnicas adotadas no projeto dos blocos em tempo discreto são apresentadas detalhadamente a partir do nível sistêmico. O projeto foi realizado em tecnologia de 28nm CMOS *Low Power*. Resultados de medida mostram que o receptor apresenta 6.5 dB de figura de ruído com rede de casamento e chaveamento integrado, e -19 dBm de IIP3 com um consumo total de 2.75 mW.

Palavras-chave: CMOS, *Bluetooth Low Energy*, receptor de tempo discreto, capacitor chaveado.

LIST OF SYMBOLS

α	$\alpha = gm/gd0$
α_n, β_n	capacitor charge ratios
γ	excess noise factor
γ_M	mixer linear time-varying coefficient
ω	angular frequency
τ	time constant
φ_n	clock signal *n*
A_i	gain of block *i*
a_n	linearity coefficient
B	noise equivalent bandwidth
Bw	bandwidth of a signal
C_H	history capacitor of a discrete-time filter
C_R	rotating capacitor of a discrete-time filter
Fi	noise factor of block *i*
f_s	sampling frequency
f_{LO}	local oscillator frequency
G_i	available power gain of block *i*
k	Boltzmann constant
K_f	flicker noise factor
L	MOS channel length
P_n	component power *n*
Q	quality factor
$q_{in}[n]$	charge packet
R_{sw}	switch resistance
S_{ij}	S-parameter

T	absolute temperature
v_n	component voltage *n*
V_T	threshold voltage
V_{ds}	MOS drain-source voltage
V_{gs}	MOS gate-source voltage
v_{in}	input voltage
v_{out}	output voltage
W	MOS channel width
Z_0	filter input impedance
Z_{ij}	Z-parameter
Z_n	impedance *n*

LIST OF ACRONYMS AND ABBREVIATIONS

ADC	Analog-to-Digital Converter
BER	Bit-Error-Rate
BLE	Bluetooth Low-Energy
BT	Bandwidth-bit Period Product
CMFB	Common-mode Feedback
CMOS	Complementary Metal-Oxide-Semiconductor
COB	Chip-on-board
CS	Charge Sharing
CT	Continuous Time
CW	Continuous-wave
DCO	Digital Controlled Oscillator
DR	Dynamic Range
DT	Discrete-Time
F	Noise Factor
FIR	Finite Impulse Response
GFSK	Gaussian Frequency Shift Keying
IF	Intermediate Frequency
IIR	Infinite Impulse Response
IM2	Second Order Intermodulation Tone
IM3	Third Order Intermodulation Tone
IoT	Internet of Things
IP2	Second Order Intercept Point
IP3	Third Order Intercept Point
LMV	LNA-Mixer-VCO

LNA	Low Noise Amplifier
LNTA	Low Noise Transconductance Amplifier
LO	Local Oscillator
LSB	Lower Side Band
LTV	Linear Time-Varying
MDS	Minimum Detectable Signal
MOM	Metal-oxide-metal
NF	Noise Figure
OOB	Out-of-Band
P1dB	1 dB compression point
PAC	Periodic AC Analysis
PCB	Printed circuit board
PDK	Process Design Kit
PER	Packet Error Rate
PNOISE	Periodic Noise Analysis
PSS	Periodic Steady State Analysis
PVT	Process, Voltage and Temperature
QN	Quantization Noise
RF	Radio Frequency
SAR	Successive Approximation Register
SAW	Surface Acoustic Wave
SC	Switched Capacitor
SDR	Software Defined Radio
SNR	Signal-to-Noise Ratio
TDD	Time Division Duplexing
TIA	Trans-Impedance Amplifier
TSMC	Taiwan Semiconductor Manufacturing Company Limited
WIS	Windowed Integration Sampler
WLAN	Wireless Local Area Network

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1 INTRODUCTION

From an analog and radio-frequency (RF) design point of view, power consumption has not always been the main constraint. Design of communication transceiver front-ends has been mainly defined by performance (NILSSON; SVENSSON, 2014). To complicate the matter, integrated circuit fabrication processes, mainly complementary metal-oxide-semiconductor (CMOS), are developed for digital applications that dominate the market. In this sense, analog and RF circuits have also to adapt to these sometimes inadequate process technologies.

Digital applications, on the other hand, have long been focusing on low power constraints in order to reduce costs of cooling, power, and to extend battery life as well.

These scenario has been slowly changing due to personal mobile communications need of longer battery time and more recently to the advent of the Internet of Things (IoT) concept. Several standards have emerged or enhanced in order to attend this recent need of low power wireless applications. Consequently, it has also become a big concern for analog and RF designers nowadays.

Low power and connectivity among intelligent devices are envisioned for the IoT. To support this, standards are designed for low data rates, low-complexity modulation schemes, and short link distances to achieve power-battery operation (HUANG, 2014). Bluetooth Smart^{TM}, also known as Bluetooth Low Energy (BLE), and Zigbee 3.0^{TM} are new popular standard versions specified to address this recent developed market. Several proprietary short-range radio solutions were also introduced, e.g. ANT+^{TM}, and NIKE+^{TM} (Nordic Semiconductor, 2010, 2008; Texas Instruments, 2015).

In the analog and RF design, this reduction of power consumption for IoT is usually obtained using different strategies, either system-level or block-level oriented. On the system-level side, event-driven operation modes are usually available in the new standards and the transceiver can be turned off or waked up for immediate or intermittent operation, with an average reduction of power consumption. On the block-level side, high performance analog intensive architectures now target less demanding specifications, also at low power. Operation at low-voltage supply and digitally-assisted analog circuits are common strategies.

Cost is another important issue in this low power wireless market, and it is strongly associated with integration. Not only technology processes optimized for low power digital are mainly used, but also traditionally external components like highly selective band-pass filters, matching networks, and duplexers have now to be integrated adding complexity to the RF design (MIRZAEI; DARABI; MURPHY, 2011; MASUCH; DELGADO-RESTITUTO, 2013; MADADI et al., 2015; PRUMMEL et al., 2015).

Recently, discrete-time (DT) transceiver implementations have being on the rise mainly associated with high performance and flexible Software Defined Radio (SDR) applica-

tions (ABIDI, 2007; MUHAMMAD et al., 2004, 2005). DT processing offers flexible tuning of filters by sampling rate adjustment with better control of filter corners when compared to continuous time processing (NIKOLIC; BORIVOJE, 2011). When implemented with passive switched-capacitor filters that do not have active elements, it also benefits from CMOS scaling, and its performance is mainly determined by the proper sizing of MOS switches (NIKOLIC; BORIVOJE, 2011). Nevertheless, discrete-time strategies have not been well explored for low power receiver applications yet.

The present work is well inserted in this context. This thesis presents the development of the first SAW (Surface Acoustic Wave)-less discrete-time (DT) Bluetooth Low Energy (BLE) receiver, with very competitive specifications for low power applications. The design was developed, implemented, and tested in TSMC 28nm CMOS.

1.1 Organization of this Thesis

Chapter 2 starts with a brief review of receiver concepts. Basic and advanced architectures trade-offs are discussed with a special emphasis on the discrete-time approach. state-of-the-art receivers for Bluetooth Low Energy are presented to enable the discussion of the requirements for the discrete-time BLE receiver which is the focus of this work.

BLE receiver system-level requirements are discussed in Chapter 3.

The architecture of the receiver is presented in Chapter 4 where block level requirements to achieve a state-of-the-art BLE receiver are developed. The main strategies adopted in the discrete-time signal processing are presented in detail, such as anti-aliasing strategies, out-of-band linearity protection and analog decimation.

In Chapter 5, the block-level circuits are presented with emphasis on the discrete-time band-pass charge-sharing filters. Block-level simulations and top-level measurements verify that the proposed solution surpass BLE standard specifications.

Finally, Chapter 6 summarizes the work and presents conclusions and future work perspectives.

2 RF RECEIVER BASIC CONCEPTS

This chapter starts with a quick review of top-level receiver design constraints moving next to basic and more advanced receiver architectures and finally presents some solutions already published targeting low power receivers mainly for Bluetooth Low Energy.

2.1 Receiver Figures

For a top-level design of a RF receiver, some requirements have to be considered from the very beginning. This section concentrates on reviewing basic parameters involved in the receiver design, namely:

- Noise Figure
- Sensitivity
- Maximum input signal
- Dynamic Range

2.1.1 Noise Figure and Noise Factor

Noise Factor (F) is defined as the ratio between the signal-to-noise ratio (SNR) at the input and the signal-to-noise ratio at the output. It characterizes how much noise was added by a specific block or system (Eq. 2.1).

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{2.1}$$

Noise Figure (NF) is the Noise Factor expressed in decibels (dB), Eq. 2.2.

$$NF = 10\log_{10}(F) \tag{2.2}$$

2.1.2 Sensitivity

Sensitivity of an RF receiver is defined as the *minimum detectable signal* (MDS) that a system can perceive with acceptable signal-to-noise ratio (RAZAVI, 2012). Since SNR_{in} can be given by the ratio between input power (P_{sig}) and input noise power given by kTB, where k is the Boltzmann constant, T is the absolute temperature in Kelvin and B is the noise equivalent bandwidth, Eq. 2.1 can also be presented as Eq. 2.3.

$$F = \frac{P_{sig}/(kTB)}{SNR_{out}} \tag{2.3}$$

Sensitivity is given by Eq. 2.4 when the minimum SNR_{out} necessary for baseband detection is considered.

$$S = P_{sig,min} = F.SNR_{out,min}.kTB \tag{2.4}$$

2.1.3 Maximum Input Signal and Dynamic Range

The *maximum input signal* that can be accepted by a system is limited by system linearity requirements. The difference between the maximum input signal and MDS is defined as *dynamic range* (DR).

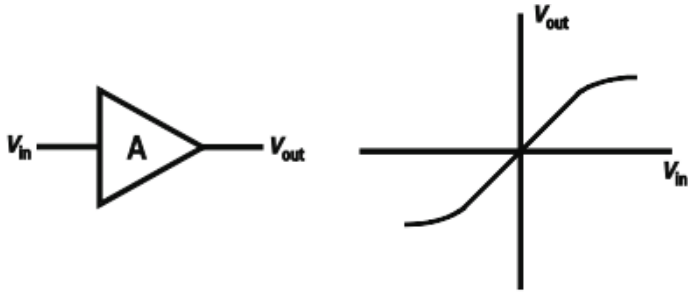
2.1.3.1 Linearity

In an ideal (linear) system, the output is linearly related to the input. In real systems, however, circuits are usually nonlinear to a certain extent. The example below helps to better understand the linearity requirements of a system. The system illustrated in Figure 2.1 presents a typical nonlinear memory-less behavior that can be represented by a truncated power expansion series (Eq. 2.5) (ROGERS; PLETT, 2003).

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 \tag{2.5}$$

In the equation, v_{in} corresponds to the system input voltage, v_{out} to the output voltage and a_0, a_1, a_2 and a_3 are coefficients that characterize system linearity. In receivers, the output curve is usually compressed as shown in Figure 2.1 and consequently a_3 assumes a negative value.

Figure 2.1: Typical nonlinear system.



Source: The Author.

A common way to measure linearity is through a test denominated *two-tone test*. In this test, two signals with different angular frequencies are presented to a system, such as the amplifier in Figure 2.1 (Eq. 2.5).

$$v_{in} = v_1 \cos \omega_1 t + v_2 \cos \omega_2 t \tag{2.6}$$

Eq. 2.7 is obtained when signal v_{in} is applied to the transfer function given by Eq. 2.5.

$$v_{out} = a_0 + a_1(v_1 \cos \omega_1 t + v_2 \cos \omega_2 t) + a_2(v_1 \cos \omega_1 t + v_2 \cos \omega_2 t)^2 + a_3(...)^3 \tag{2.7}$$

After simplification using trigonometric identities in Eq. 2.7, many different frequency components appear, such as: DC (zero frequency component), ω_1, ω_2, $\omega_1 \pm \omega_2$, $\omega_2 \pm \omega_1$, $3\omega_1$, $3\omega_2$, $2\omega_1 \pm \omega_2$, $2\omega_2 \pm \omega_1$.

In Eq. 2.7, second order terms generate components at *DC*, second harmonics and the combination of input frequencies: $\omega_2 \pm \omega_1$. For instance:

$$(v_1 \cos \omega_1 t + v_2 \cos \omega_2 t)^2 = \frac{v_1^2}{2} + \frac{v_2^2}{2} + \frac{v_1^2}{2} \cos 2\omega_1 t + \frac{v_2^2}{2} \cos 2\omega_2 t + v_1 v_2 \cos(\omega_1 \pm \omega_2) t \quad (2.8)$$

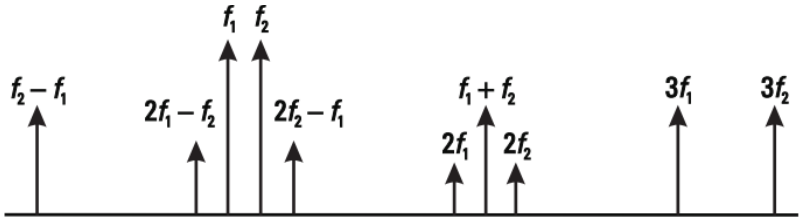
Third order terms generate components in the fundamental frequency, third harmonics and the combination of frequencies: $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$.

$$(v_1 \cos \omega_1 t \ + \ v_2 \cos \omega_2 t)^3 \ = \ v_1 \left(\frac{3}{4} v_1^2 + \frac{3}{2} v_2^2 \right) \cos \omega_1 t \ + \ v_2 \left(\frac{3}{4} v_2^2 + \frac{3}{2} v_1^2 \right) \cos \omega_2 t$$

$$+ \frac{3}{4} v_1^2 v_2 \cos(2\omega_1 \pm \omega_2) t + \frac{3}{4} v_1 v_2^2 \cos(2\omega_2 \pm \omega_1) t + \frac{v_1^3}{4} \cos 3\omega_1 t + \frac{v_2^3}{4} \cos 3\omega_2 t \quad (2.9)$$

Of particular interest are the fundamental frequency and the third order combination of frequencies because they are close to the fundamental and can appear inside the frequency band of a receiver. Figure 2.2 shows the second harmonics in black and the third harmonics in gray at the output of the modeled system.

Figure 2.2: Combination of harmonics for the modeled system.



Source: Adapted from (ROGERS; PLETT, 2003).

2.1.3.2 Third Order Intercept Point

By varying the amplitude of the input signals in a two-tone test, the fundamental output and the intermodulation output power can be plot as a function of the input power resulting in a graph such as presented in Figure 2.3. From the plot, the *third order intercept point* (IP3), a theoretical extrapolation point where the amplitude of the intermodulation tones ($2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$) are equal to the amplitudes of the fundamental tones is established.

With two tones of same amplitude $v_1 = v_2 = v_i$, the sum of the components of Eq. 2.6 that appear in the fundamental frequency is given by 2.10 (ROGERS; PLETT, 2003).

$$v_{fund} = a_1 v_i + \frac{9}{4} a_3 v_i^3 \quad (2.10)$$

The component amplitudes that appear at the third order intermodulation tones (IM3) are given by Eq. 2.11.

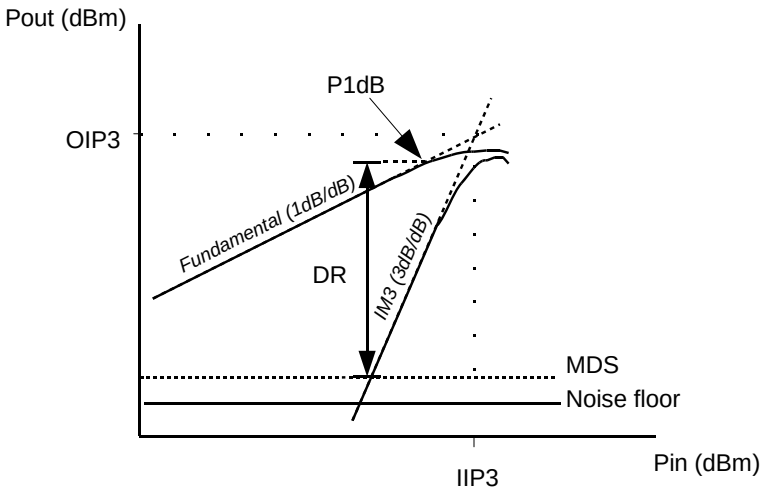
$$v_{IM3} = \frac{3}{4} a_3 v_i^3 \quad (2.11)$$

IP3 extrapolation point can be calculated when the linear component of Eq. 2.10 is equal to the IM3 component of Eq. 2.11. It is important to observe that as presented from the beginning v_{IP3} is defined in peak voltage values.

$$v_{fund} = v_{IM3} \Rightarrow \alpha_1 v_i = \frac{3}{4} a_3 v_i^3 \Rightarrow v_{IP3} = v_i = \sqrt{\frac{4a_1}{3|a_3|}} \tag{2.12}$$

In Figure 2.3, it can be observed that the slope of the fundamental line is 1 dB/dB while the slope of the IM3 line is 3 dB/dB. The extrapolation point defines both *input 3rd order intercept point* (IIP3) and *output 3rd order intercept point* (OIP3).

Figure 2.3: Output power of fundamental and IM3 versus input power.



Source: the Author.

Linearity figures are usually measured in dBm, or decibel referred to 1 mW (Eq. 2.13).

$$P_{dBm} = 10 \log_{10}(P_W / 1\ mW) \tag{2.13}$$

2.1.3.3 1dB Compression Point

Figure 2.3 also shows the definition of MDS (sensitivity), dynamic range and *1 dB compression point* (P1dB) that defines the dynamic range.

P1dB is defined as the point where the power level at the output is 1 dB compressed. The definition of compression point establishes the use of one tone instead of two tones. The fundamental components are given by Eq. 2.14.

$$v_{fund} = \alpha_1 v_i + \frac{3}{4} a_3 v_i^3 \tag{2.14}$$

When compared to Eq. 2.10 the result is slightly different and the measurements usually do not match when compression point is calculated through both methods. The (*one-tone*) compression point can be calculated by Eq. 2.15.

$$v_{1dB} = \sqrt{0.145 \frac{a_1}{|a_3|}} \tag{2.15}$$

P1dB compression point and *IIP3* are related. Eq. 2.16 can be easily obtained through equations 2.12 and 2.15.

$$IIP3 \cong P1dB + 9.6 \tag{2.16}$$

It is important to emphasize that while Eq. 2.12 was obtained in a two-tone test, Eq. 2.15 was obtained in a one-tone test. Consequently, this approximation holds only if only one-tone is producing the distortion during signal compression. In a two-tone test it is not possible to observe both results at the same time[1].

2.1.3.4 Second Order Intercept Point

Second order intercept point (IP2) is also of interest, specially when working with direct conversion or low IF (Intermediate Frequency) receivers because the second order products appear at DC or at low frequencies $(\omega_2 - \omega_1)$.

From Eq. 2.8, it is easy to show that DC component amplitudes due to the second order intermodulation tones (IM2) are given by Eq. 2.17, since $v_i = v_1 = v_2$.

$$v_{IM2} = av_i^2 \tag{2.17}$$

Consequently, the slope would be 2 dB/dB in a plot like Figure 2.3 and v_{IP2} can be solved as Eq. 2.18. IIP2 is usually tens of decibels higher than IIP3.

$$v_{fund} = v_{IM2} \Rightarrow a_1 v_i = a_2 v_i^2 \Rightarrow v_{IP2} = \frac{a_1}{a_2} \tag{2.18}$$

2.1.4 Gain, Linearity and Noise Factor of Cascaded Stages

The first stage in a receiver is the main responsible for the overall system noise factor. When it comes to linearity, on the other hand, first stages have less impact. Consequently, in receiver design it is very important to know where to put effort in improving linearity or noise factor.

Figure 2.4 shows a system of cascaded amplifiers. In the figure, F_i, G_i, A_i and $v_{IP3,i}$ are noise factor, available power gain, gain and IIP3 of block i. Cascaded gain is defined by Eq. 2.19 and total noise factor (F) is given by the relation known as Friis equation (Eq. 2.20).

$$G = G_1 G_2 G_3 \tag{2.19}$$

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... \tag{2.20}$$

In Eq. 2.20, G is the available power gain and it takes into account both matching and the difference between source and load impedances of each block. In this sense, it is different than the traditional power gain defined by Eq.2.21 when equal input and output impedances are considered not accounting for matching.

$$powergain = A_1^2 \tag{2.21}$$

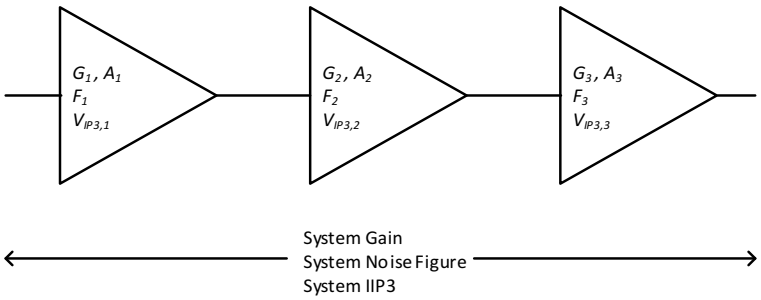
The worst case IIP3 of such a system is given by Eq. 2.22. Good linearity is represented by higher IP3 values. Consequently, if the stages at the front of the receiver chain have higher gains then latter stages are more critical in terms of linearity.

[1] Some simulation tools make this measurement possible since they can use one tone that produces distortion and one tone that does not. It is an analysis of large signal usually using *Harmonic Balance method* performed together with a small signal analysis. Cadence SpectreRF^{TM} analysis *PSS* and *PAC* used together can provide this result. Nevertheless, this type of measurement is only valid for receivers.

$$\frac{1}{v_{IIP3}^2} = \frac{1}{v_{IP3,1}^2} + \frac{A_1^2}{v_{IP3,2}^2} + \frac{A_1^2 A_2^2}{v_{IP3,3}^2} \ldots \tag{2.22}$$

In fact, Eq. 2.22 is an approximation. More precise calculations or simulations must be performed to better predict the overall system IIP3 (RAZAVI, 2012). The result predicted by the equation is more pessimistic and consequently implies in a larger design effort.

Figure 2.4: Cascaded system.



Source: the Author.

Although equations 2.20 and 2.22 were initially developed for amplifiers, they are also valid for mixers and filters and are readily applicable in the receiver design. For this calculation in the mixer case, the mixing or frequency translation effect have to be also considered.

2.2 Receiver Architectures

This section reviews traditional and modern receiver architectures focusing on a brief discussion about the advantages and disadvantages of each topology.

2.2.1 Direct Conversion Receiver

A direct conversion architecture (Figure 2.5) is characterized by a direct translation of the received signal to baseband in a single step. The first block in the receiver chain is denominated *low noise amplifier* (LNA) and is the main responsible for the noise figure of the system, as discussed in Section 2.1.4. Therefore, it needs to provide moderate gain while introducing little noise. The output of the LNA is downconverted directly to the baseband by the quadrature mixer. The highest gain in the receiver chain is provided by the baseband amplifier. The baseband amplifier usually has programmable gain and offset correction circuits due to requisites of the dynamic range of the analog-to-digital converter (ADC) and to the offset voltage introduced by the mixer circuit. Frequency generated by the local oscillator (LO) or synthesizer is at the center of the channel and must cover the complete frequency range.

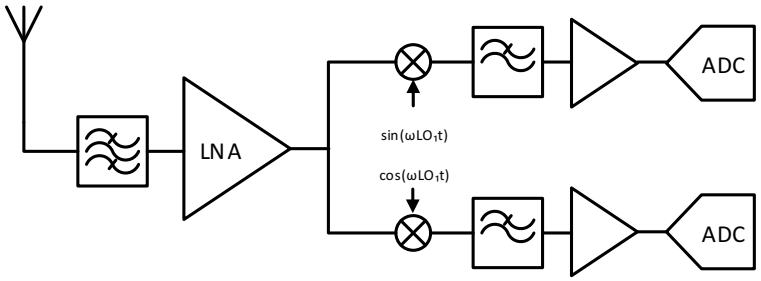
The main advantages of this architecture are (TUTTLEBEE, 2002):

- low complexity, suitable for integrated circuit realization ;
- reduced number of blocks (when compared to the multiple conversion architecture to be presented following);
- simple filtering requirements.

Some disadvantages are:

- quality in-phase and quadrature signal generation is necessary over the complete frequency range;
- balanced mixers are necessary in order to better reject the oscillator fundamental frequency at the output and to reduce oscillator leakage to the input[2];
- the second order distortion product falls *in-band*;
- 1/f noise can not be eliminated and may become a severe noise problem.

Figure 2.5: Direct conversion architecture.



Source: the Author.

2.2.2 Heterodyne Receiver

In a heterodyne architecture, the received signal is translated to the baseband in multiple steps, originating intermediate frequencies. This approach minimizes some of the problems presented by the direct conversion, such as *LO self mixing* and second order distortion but it adds complexity to the system, and usually increases power consumption. A possible implementation of an heterodyne architecture is presented in Figure 2.6 (RAZAVI, 2012).

Its main advantages are:

- better selectivity (a channel filter is added after the first mixer);
- gain is distributed over several amplifiers in different frequency bands, which leads to an easier implementation;
- the first mixer is not a quadrature mixer.

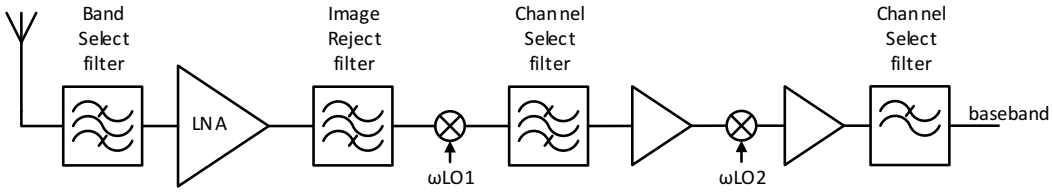
Its main disadvantages are:

- high complexity: many blocks and consequent higher power consumption;
- more local oscillator signals have to be generated;
- highly selective IF filters are required to remove signal image, making it hard to obtain single chip realizations.

[2]Local oscillator leakage to the input of the mixer can be reflected by the LNA, the antenna or by external obstacles returning back to the antenna, being amplified by the LNA and downconverted back to a DC component that is *in band* in this architecture. This *time varying* DC offset caused by *self-mixing* is a typical problem of the direct conversion architecture (TUTTLEBEE, 2002; RAZAVI, 2012).

In a heterodyne architecture, the second mixer can be implemented digitally with stronger requirements for the ADC or using analog components with additional requisites for the synthesizer, and additional filters as well.

Figure 2.6: Heterodyne architecture.



Source: the Author.

2.2.3 Sliding IF Architecture

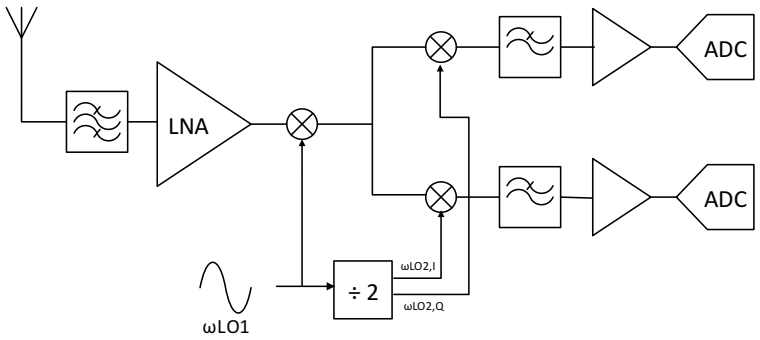
Recently, sliding IF architectures have been adopted as a means to simplify receiver design of multiple conversion architectures using only one synthesizer (RAZAVI, 2012; LIU et al., 2014). They use frequency division in order to generate different clocks, emulating different local oscillators. As a consequence, the first IF frequency varies according to the selected channel. This characteristic can be observed in Figure 2.7.

The main advantages of this architecture are:

- the first mixer is not a quadrature mixer;
- only one local oscillator is required;
- no problem of second order distortion or 1/f noise.

The main disadvantage is the high complexity of the architecture.

Figure 2.7: Sliding IF architecture .



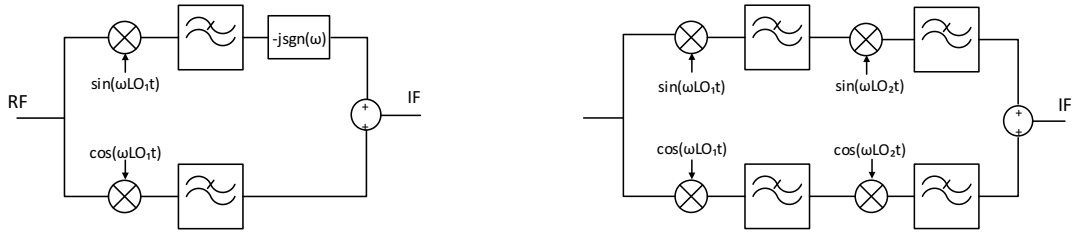
Source: the Author.

2.2.4 Image-Reject Architecture

The need for a filter to remove image in a heterodyne receiver makes it generally unsuitable to integrated circuit implementation. Alternative implementations make use of different strategies to cancel image without the need of high performance filtering, like *Hartley* and *Weaver* architecture presented in Figure 2.8a and 2.8b respectively(RAZAVI, 2012).

Hartley architecture uses a Hilbert filter to eliminate the image, while Weaver architecture needs two different quadrature local oscillators to achieve image cancellation. In both cases, LO_1 can have tough requirements because of the quadrature implementation at a higher frequency. The implementation of a Hilbert filter, though traditional in analog design, may present some difficulties in CMOS due to resistors and capacitors mismatches (RAZAVI, 2012).

Figure 2.8: Image-reject architectures.



a)Hartley b)Weaver

Source: the Author.

2.2.5 Low-IF and High-IF Architectures

Low-IF and high-IF architectures are alternatives that combine advantages both from direct conversion and heterodyne architectures. In a low-IF receiver, the IF is chosen as half the bandwidth of the signal (RAZAVI, 2012), while high-IF have IF bigger than signal bandwidth. Low-IF or high-IF architectures reduce requirements of image rejection. Image rejection will be partly performed in the digital domain, after analog-to-digital conversion. Additionaly, since it does not convert the signal directly to baseband it avoids problems with DC offset, flicker noise and IP2.

Its main advantages are:

- less DC Offset problems;
- lower complexity than the heterodyne approach.

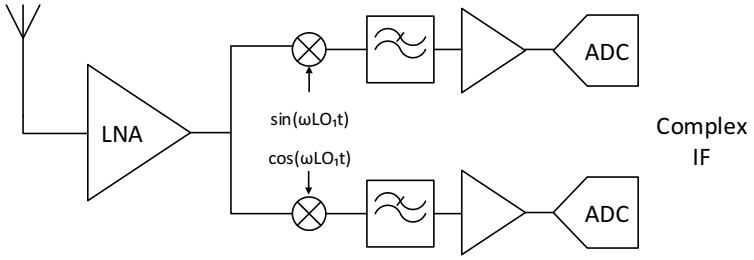
Its main disadvantages are

- need of a better image rejection when compared with direct conversion architectures;
- higher ADC sampling rate is required.

2.3 Discrete-Time Receivers

The feasibility of discrete-time (DT) receiver architectures has been presented in several applications, e.g. Bluetooth (STASZEWSKI et al., 2004), GSM (MUHAMMAD et al., 2005), WLAN (JAKONIS et al., 2005), and SDR (BAGHERI et al., 2006a). They offer several advantages when compared to continuous time (CT) receivers, mainly when implemented in new deep sub-micron technologies, e.g. due to the excellent component matching of capacitors and the possible implementation of programmability to compensate for process, voltage and temperature (PVT) variations (RU; KLUMPERINK; NAUTA, 2007).

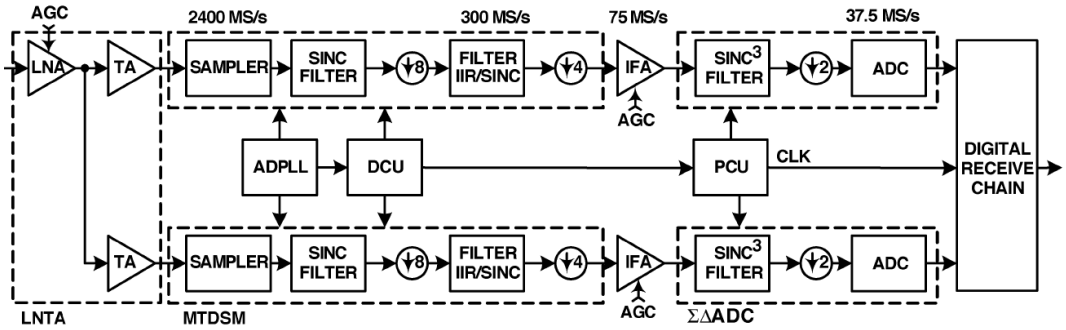
Figure 2.9: Low IF architecture.



Source: the Author.

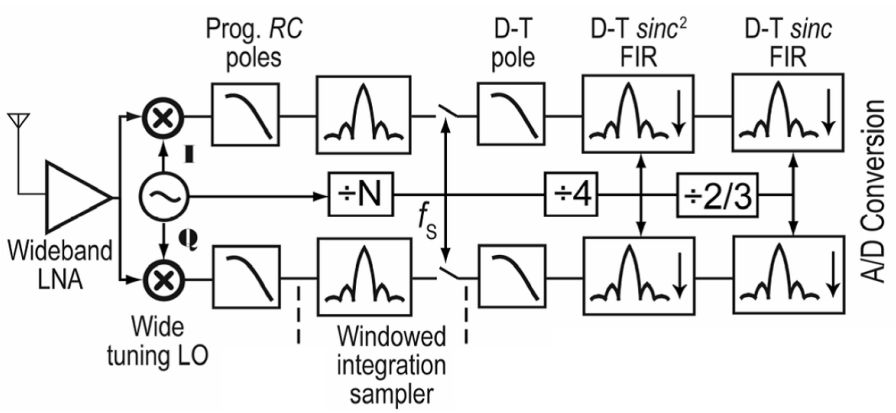
Figures 2.10 and 2.11 present a commercial and an academic discrete-time receiver proposed (STASZEWSKI et al., 2004; BAGHERI et al., 2006a) . In the first architecture, the signal is directly subsampled after amplification by a low noise transconductance amplifier (LNTA) and, in the second structure it is downconverted by an analog high linearity mixer after LNA amplification. The main difference between the two architectures is the interface between LNA/LNTA and sampler/mixer. The adoption of a current input and current output in the sampler insert additional filtering due to the windowing effect that is detailed in the next sections. In both cases, filter processing is performed in the discrete-time domain after downconversion.

Figure 2.10: Bluetooth discrete-time receiver presented by Texas Instruments.



Source: (STASZEWSKI et al., 2004).

Figure 2.11: Wideband discrete-time receiver.



Source: (BAGHERI et al., 2006a).

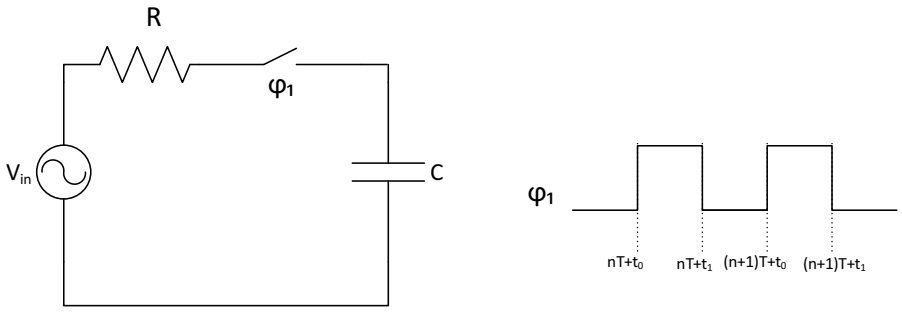
The functional blocks typically adopted in DT receivers for downconversion and filtering are sampling mixers, finite impulse response (FIR) filters, and infinite impulse response (IIR) filters. Below, these blocks are briefly described.

2.3.1 Sampling Mixer

In the first DT architecture presented in this section (Figure 2.10), a sampler is adopted for the downconversion instead of a traditional active mixer. In DT receivers, RF sampling is performed in voltage or in charge domain, in both cases using a subsampling technique since Nyquist sampling is usually not feasible. Both voltage sampling and charge sampling cases were analyzed in detail in (XU; YUAN, 2000).

The structure of the voltage sampling mixer is presented in Figure 2.12. The time needed to acquire the voltage sample depends on a time constant $\tau = RC$. The product between the time constant and the frequency of the sampled signal ($\tau\omega$) has to be minimized to reduce the group delay introduced by the circuit (should be less than 0.1 according to (XU; YUAN, 2000)). The circuit requires a trade off since a small sampling capacitance reduces the group delay but increases the error voltage due to the clock feedthrough (EICHENBERGER; GUGGENBUHL, 1991).

Figure 2.12: (a) Voltage sampling principle. (b) Clock waveform.

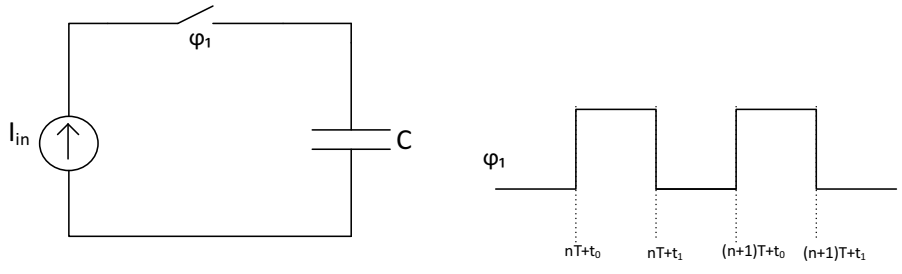


(a) (b)

Source: the Author.

The charge sampling approach is presented in Figure 2.13. The charge q_{in} is integrated over the capacitor C from t_0 to t_1 in the *sample phas*e, to be *hold* until the end of the period. Charge sampled in the previous interval can be discharged during a reset phase, as presented in (XU; YUAN, 2000), or added to the charge stored in the capacitor during previous samples, as presented in Figure 2.13.

Figure 2.13: (a) Charge sampling principle. (b) Clock waveform.



(a) (b)

Source: the Author.

To analyze the charge sampling process, we start with the definition of a discrete-time series of the voltage over the capacitor at time *n* (Eq. 2.23), as proposed in (NIKOLIC; BORIVOJE, 2011):

$$v_{out}\left[n\right] = \frac{q_{in}[n]}{C} + v_{out}[n-1] \tag{2.23}$$

$$q_{in}\left[n\right] = \int_{nT+t_0}^{nT+t_1} i\left(t\right) dt \tag{2.24}$$

where $q_{in}[n]$ is the charge packet created at the sampling time *n* and T is the sampling period.

The charge packet $q_{in}[n]$ can also be represented as a continuous-time convolution between the input signal $i(t)$ and a windowing function $p(t)$ that shapes the sampling pulses and acts as a continuous-time filter (Eq. 2.25 and 2.26).

$$q_{in}\left[n\right] = \int_{nT}^{nT+\delta T} i\left(\tau\right) p\left(\left(nT+\delta T\right)-\tau\right) d\tau \tag{2.25}$$

$$p\left(t\right) = \begin{cases} \frac{1}{\delta T}, & if\ 0 \leq t \leq \delta T \\ 0, & otherwise \end{cases} \tag{2.26}$$

where $\delta T = t_1 - t_0$, and amplitude $\frac{1}{\delta T}$ of the filter is used to normalize its DC gain to 0 dB.

In the frequency domain, the transfer function *in modulus* of the windowing filter is:

$$\left|H_p\left(\omega\right)\right| = \frac{sin\left(\frac{\omega\delta T}{2}\right)}{\frac{\omega\delta T}{2}} = sinc\left(\frac{\omega\delta T}{2}\right) \tag{2.27}$$

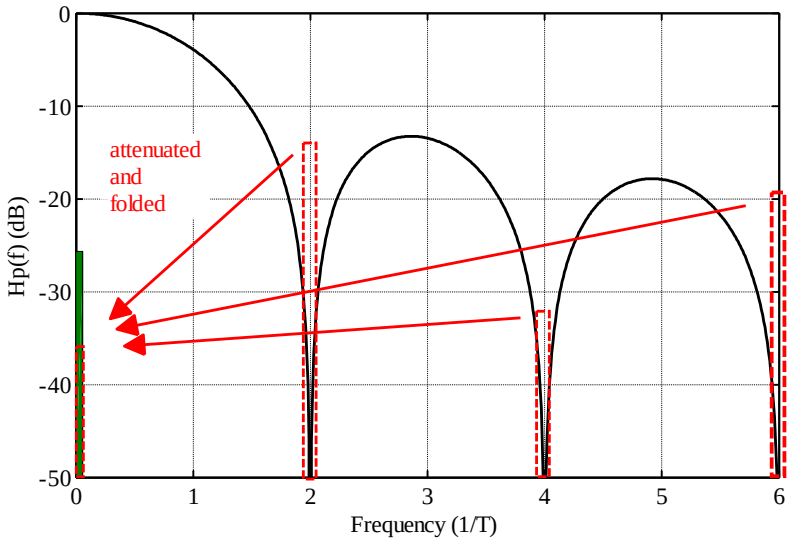
Figure 2.14 shows the transfer function (Eq. 2.27) obtained when δT is chosen as 50 % of the sampling period. In the figure, it is possible to observe that there is a built-in anti-aliasing effect characterized by a strong attenuation at even multiples of the sampling frequency $1/T$. This anti-aliasing effect is not observed in voltage sampling.

Besides being attenuated by the windowed integration sampler (WIS), signals at these nulls are also folded to DC (BAGHERI et al., 2006; TOHIDIAN; MADADI; STASZEWSKI, 2014).

Besides the built-in anti-alisiasing filter effect, charge sampling offers several advantages over voltage sampling in newer technologies (XU; YUAN, 2000, 2005), such as:

- linear phase shift and constant group delay (also sampling capacitor can be designed to minimize clock feedthrough independently of group delay);
- thermal noise is reduced since it is shaped by the sampling window;
- error from charge sampling due to jitter does not increase at higher frequencies.

Figure 2.14: 50 % duty-cycle charge sampling transfer function. *(Matlab^{TM})*



Source: the Author.

2.3.2 Infinite Impulse Response Filter

In the charge sampling circuit presented in Figure 2.13, there is both a discrete-time integrator and a sampler circuit. The discrete-time integrator can also be modeled as a running sum of the input charge packets over time.

Consider $q_H[n]$ the total charge contained by the capacitor C_H at the sample time n.

$$q_H[n] = q_H[n-1] + q_{in}[n] \tag{2.28}$$

The transfer function of the ideal discrete-time integrator in the z-domain is given by :

$$\frac{Q_H(z)}{Q_{in}(z)} = \frac{1}{1-z^{-1}} \tag{2.29}$$

As presented in Figure 2.15 adapted from (NIKOLIC; BORIVOJE, 2011), a generic IIR filter can be implemented as a cascade of two discrete-time lossy-integrators. The term 'lossy' is adopted because part of the charge originally residing in C_H intentionally 'leaks' to C_R in the next phase.

The first DT lossy-integrator is formed by $C_{H1}$and C_R, with the transfer function given by:

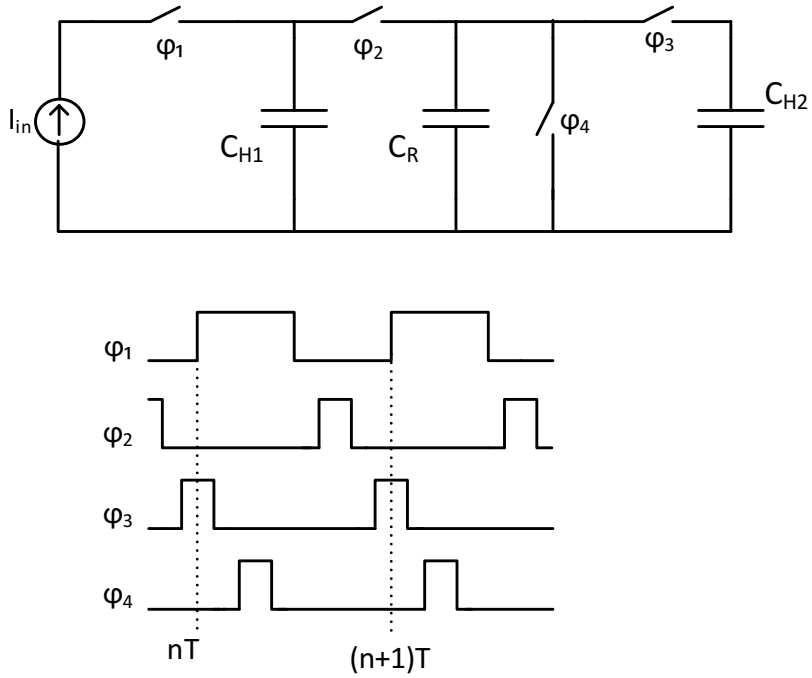
$$\frac{Q_{H1}(z)}{Q_{in}(z)} = \frac{1}{1-\alpha_1 z^{-1}} \tag{2.30}$$

where $\alpha_1 = C_{H1}/(C_{H1}+C_R)$ represents the charge ratio kept in C_{H1} and $\beta_1 = C_R/(C_{H1}+C_R)$ is the ratio of the charge transferred (by the *lossy* integration in the process) to C_R in φ_2.

And the second DT lossy-integrator is formed by C_R and C_{H2}, with transfer function given by:

$$\frac{Q_{H2}(z)}{Q_R(z)} = \frac{1}{1-\alpha_2 z^{-1}} \tag{2.31}$$

Figure 2.15: IIR discrete-time implementation.



Source: the Author.

where $\alpha_2 = C_{H2}/\left(C_{H2} + C_R\right)$ is the charge ratio transferred from C_R to C_{H2} in φ_4.

As shown in the complete circuit (Figure 2.15), charge is first transferred from C_{H1} to C_R, and subsequently transferred from C_R to C_{H2}. During phase φ_3, the intermediate charge in C_R is removed.

The complete transfer function of this IIR filter, without considering the charge sampling effect created by φ_1 (presented in Section 2.3.1), is given by:

$$\frac{V_{H2}(z)}{Q_{in}(z)} = \frac{\beta_1/C_{H2}}{\left(1-\alpha_1 z^{-1}\right)\left(1-\alpha_2 z^{-1}\right)} \tag{2.32}$$

Figure 2.16 presents the normalized IIR filter transfer function (Eq. 2.32). The transfer function presented in the figure is ideal and does not include the pulse shape effect. Since it is a discrete-time filter, the transfer function of this low pass filter is repeated with the period of the sampling rate ($1/T_s$), as presented in the figure. Based on the Nyquist sampling theory, sampling a continuous time signal will fold components at multiples of the sampling rate to DC, as shown in the the figure.

The attenuation of the filter at $0.5/T_S$ is given by:

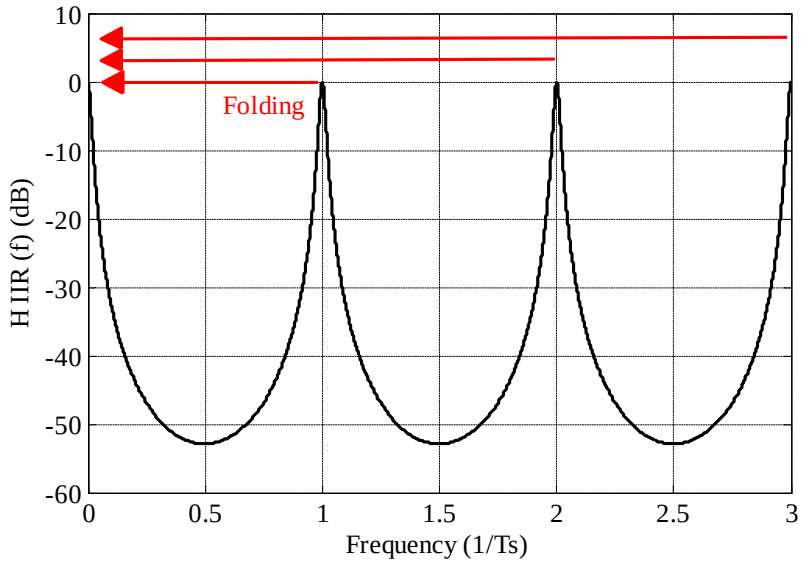
$$Atten_{1/2} = 20\log_{10}\left(\frac{C_R^2}{\left(C_R + 2C_{H1}\right)\left(C_R + 2C_{H2}\right)}\right) \tag{2.33}$$

When the pulse sampling effect is considered in the 50 % duty-cycle case proposed in Figure 2.15, there is a strong attenuation of the even replicas of the signal as can be observed in Figure 2.17.

2.3.3 Finite Impulse Response Filter

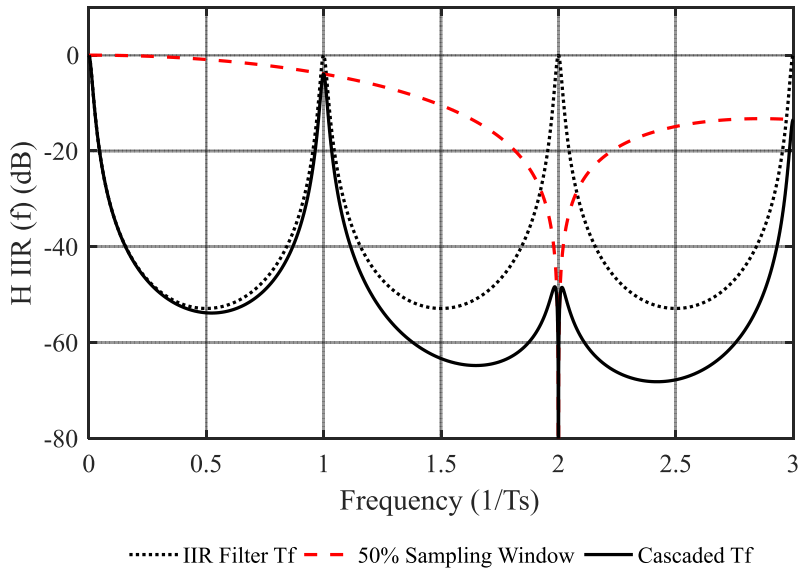
A finite impulse response (FIR) filter can be used to implement a decimation filter, typically used in a multirate DT receiver as an anti-aliasing filter for the process of down-

Figure 2.16: IIR transfer function. *(Matlab)*



Source: the Author.

Figure 2.17: IIR transfer function. *(Matlab)*



Source: the Author.

sampling.

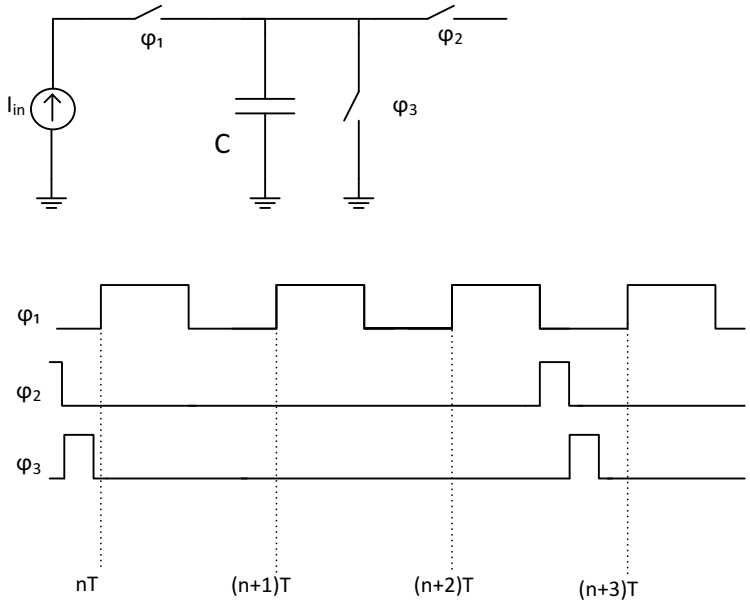
The simplest realization is an N-stage FIR filter with uniform tap weights (BAGHERI et al., 2006b; KARVONEN, 2006), where N corresponds to the decimation factor.

$$H_2(z) = \frac{1 - z^{-N}}{1 - z^{-1}} = 1 + z^{-1} + z^{-2} + ... + z^{-(N-1)} \tag{2.34}$$

Figure 2.18 presents a simplified implementation of a FIR filter, also known as a moving-average filter in this case. In the circuit, three charge samples are integrated in

the capacitor C. The charge is removed from the capacitor at phase φ_3 after read in phase φ_2, implementing a 3-stage FIR filter.

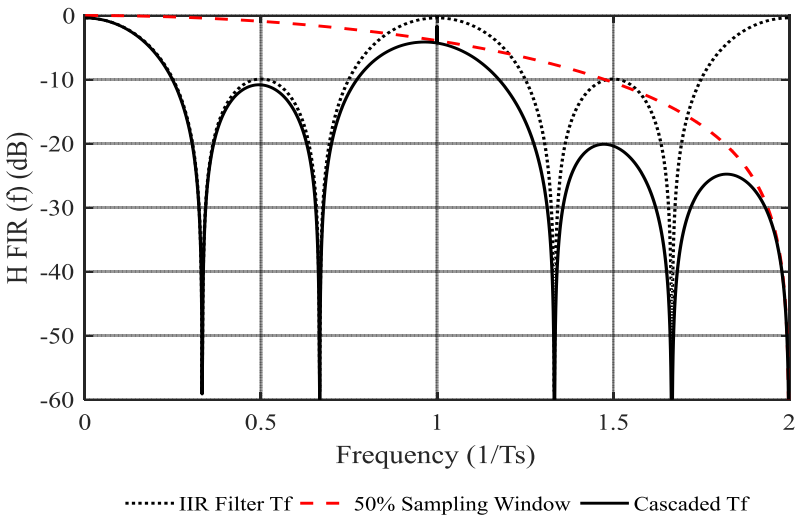
Figure 2.18: FIR DT implementation.



Source: the Author.

The transfer function of the 3-stage FIR decimation filter is presented in Figure 2.19. In the plot, the nulls at multiples of f_s/N , implement the anti-aliasing filter and define the stopbands. The folding and the window sampling effect are also illustrated in the figure.

Figure 2.19: FIR transfer function. *(Matlab)*



Source: the Author.

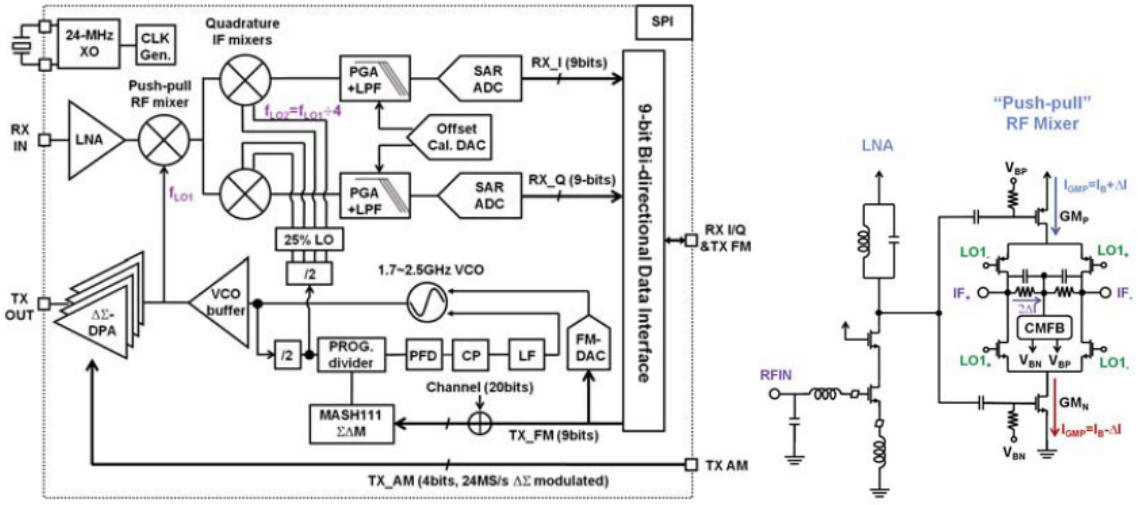
2.4 State of the Art in BLE Receiver Design

This section discusses receiver architectures recently presented for low power applications in 2.4 GHz targeting BLE Standard.

Initially, two sliding-IF receivers are presented in Figures 2.20 and 2.21. As presented before, both alternatives adopt a real (non-quadrature) mixer for the first stage to reduce power as well as a traditional common-source cascoded LNA for the first stage filtering and input matching.

The first approach (LIU et al., 2013) uses a push-pull active mixer with single input and differential output and $f_{LO} = f_{RF} * 4/5$, with a consequent bigger IF and better image rejection. The second approach (WONG et al., 2012) adopts a Gilbert-cell mixer with one input tied to AC ground, and a consequent 6 dB loss in gain, and $f_{LO} = f_{RF} * 16/17$. Both receivers use complex IQ passive mixers for the frequency translation to baseband, but with some differences. The first approach uses a 25 % duty-cycle LO, and the second receiver uses a 50 % duty-cycle LO mixer that is pre-amplified by an IF buffer. Both receivers also adopt an analog programmable buffer with filtering and DC offset correction for the baseband amplification. The receivers consume 3.6 mW and 6.5 mW of power respectively with roughly the same performance, as presented in Table 2.1 at the end of this section.

Figure 2.20: (a) Sliding-IF BLE receiver for Zigbee and Bluetooth. (b) RF front-end receiver with push-pull mixer.

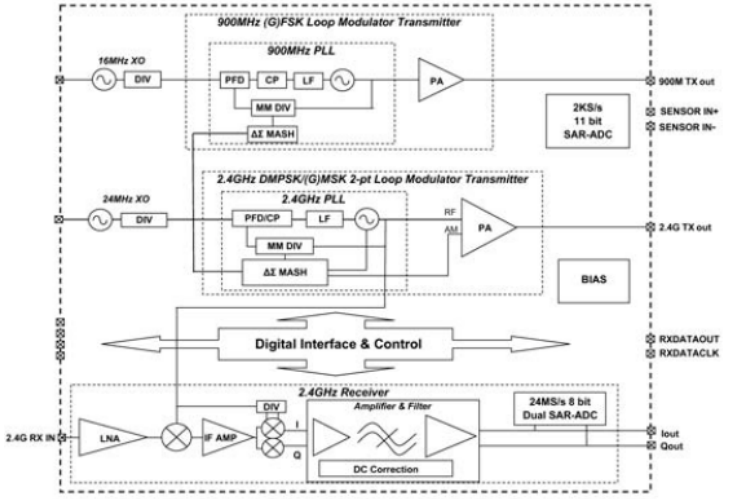


(a) (b)

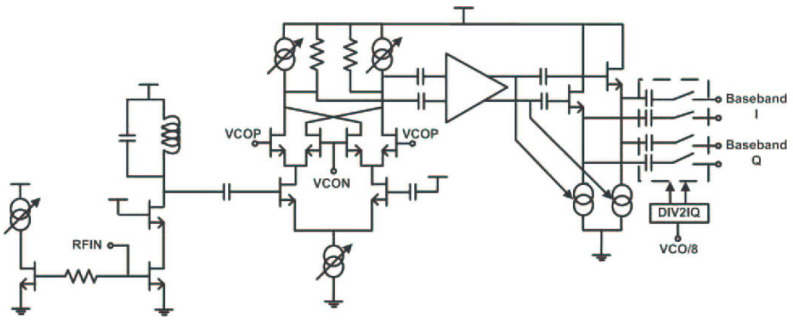
Source: (LIU et al., 2013).

Figure 2.22 proposes a Low IF receiver that uses an LNA-Mixer-VCO (LMV) approach for first stage (SELVAKUMAR; ZARGHAM; LISCIDINI, 2015). Two main strategies are applied in this receiver in order to reduce the power consumption: quadrature LNA is implemented to allow for a simpler non-quadrature VCO, and current supply is reused by LNA, mixer and VCO. Finally, the low IF signal is amplified by transimpedance amplifiers (TIA) and filtered by a complex filter centered in 2 MHz. The result is an impressive sub-1 mW power consumption with an acceptable NF of 15 dB, since BLE requires 19 dB for a -80 dBm sensitivity target (Table 2.1).

Figure 2.21: (a) Sliding-IF BLE receiver for biotelemetry application. (b) RF front-end detail.



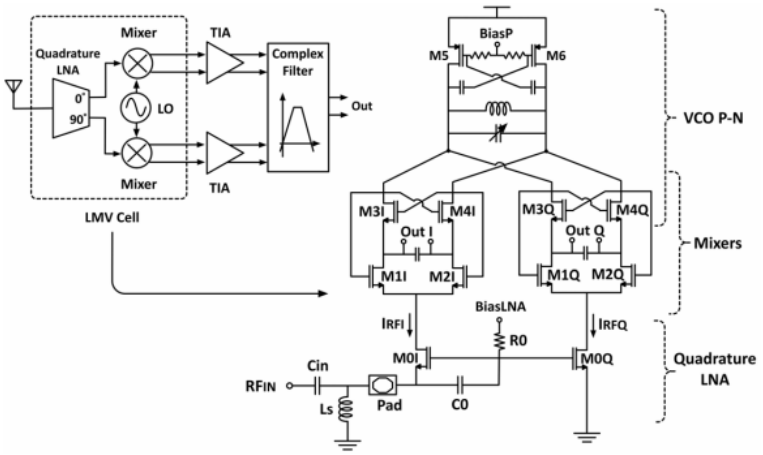
(a)



(b)

Source: (WONG et al., 2012); (WONG et al., 2013).

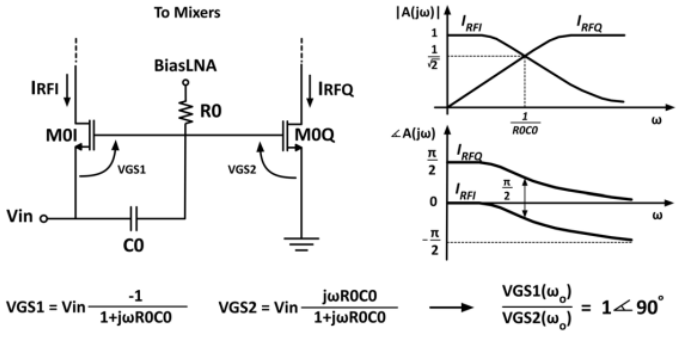
Figure 2.22: BLE receiver using LMV front-end.



Source: (SELVAKUMAR; ZARGHAM; LISCIDINI, 2015).

The quadrature LNA of the LMV receiver is detailed in Figure 2.23. It is a common-source, common-gate single-input, with an RC passive 90^o phase shifter. The matching between I and Q is sensitive to process variations.

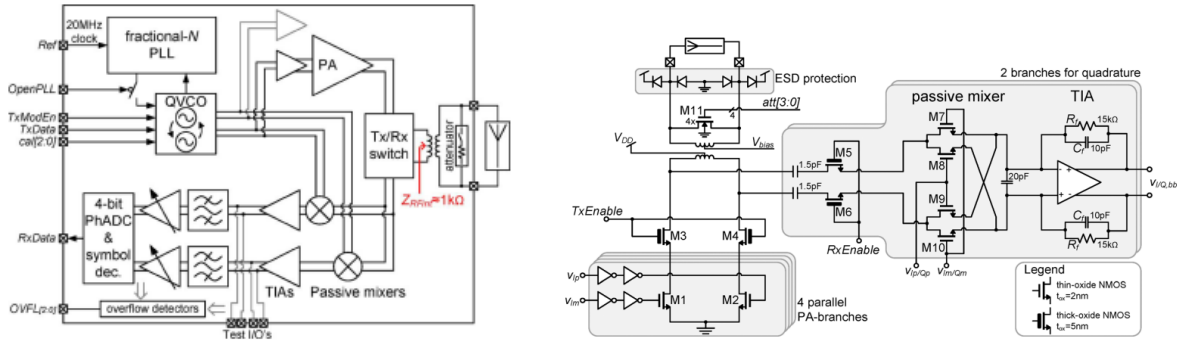
Figure 2.23: Quadrature LNA detail.



Source: (SELVAKUMAR; ZARGHAM; LISCIDINI, 2015).

In order to reduce costs, newer BLE approaches aim at integration of the transceiver switch as well as the input matching. Figure 2.24 presents a receiver differential input, an internal transformer and no LNA. Since noise and sensitivity requirements of BLE standard are not challenging, it is possible to achieve 16.5 dB of noise figure without LNA and at a 1.1 mW of power consumption. The integration of the switch and matching is facilitated by TX and RX internal switches that are used to uncouple receiver and transmitter during the Time Division Duplexing (TDD) operation of the standard. The receiver implements a direct conversion strategy using quadrature passive mixers. A 4-bit phase-domain ADC is used for the GFSK demodulation. The overall performance is comparable to the low-IF receiver presented in Figure 2.23 (Table2.1).

Figure 2.24: (a) BLE transceiver without LNA. (b) Details of passive conventional mixer.



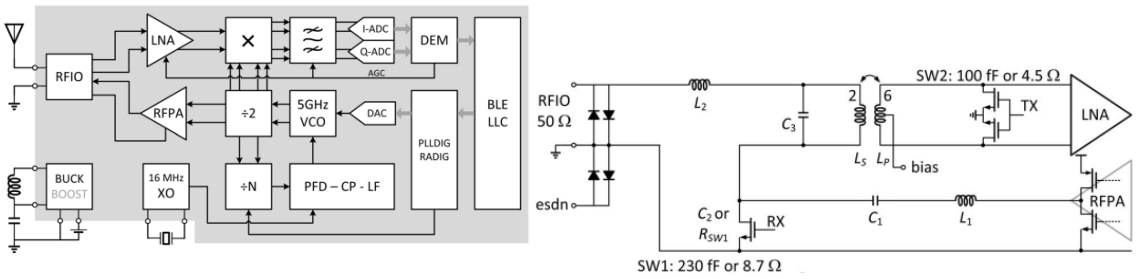
(a) (b)

Source: (MASUCH; DELGADO-RESTITUTO, 2013).

The last analyzed receiver also integrates the switch, but using a single-input approach (Figure 2.25). The differential LNA is connected to the single input through an internal

passive balun. A switch is placed before the LNA to disconnect it from the input during the transmission. In receiver operation, there is also a switch to disconnect the PA. A differential common-source cascoded LNA is followed by a quadrature mixer using a switched transconductance design in a direct conversion topology. Baseband amplification is implemented using conventional AGC with DC offset-correction. The receiver presents good performance but at a higher power consumption cost when compared to the other analyzed architectures (Table2.1).

Figure 2.25: (a) Integrated switch BLE transceiver. (b) Detail of LNA and PA antenna matching.



(a) (b)

Source: (PRUMMEL et al., 2015).

Table 2.1 presents the main figures of the continuous-time BLE receivers analyzed. They offer a good trade-off between power and performance, except for (PRUMMEL et al., 2015) that was chosen also because of the integrated switch.

2.5 Summary

This chapter reviewed the main receiver system-level figures such as noise figure, compression point, IIP2, IIP3 and gain. Basic and more advanced receiver architectures were also reviewed with their advantages and disadvantages briefly discussed. Discrete-time receiver techniques were reviewed in more detail to prepare for the receiver development in Chapter 4. For comparison, system-level figures of recently published low power receivers were also presented. As it can be observed in this brief comparison, discrete-time architectures have not been well-explored for BLE applications yet. It indicates that research is still needed in this area.

Table 2.1: Comparison of state-of-the-art Bluetooth Low Energy receivers previously published.

Standard	Zigbee+BLE +MBAN	BLE	BLE +MBAN	BLE	BLE
Technology	90n	55n	0.12u	0.13u	0.13u (1.0V)
Data rate (MBPS)	0.25/1/0.97	1	1	1	1
Noise Figure (dB)	6	$\sim 6*$	6	15.1	16.5
IIP3 (dBm)	-19	-	-	-15.8	-2.9
Image Reject (dB)	35	-	-	30.5	-
Sensitivity (dBm)	-100/-98/-96	-94.5	-96.5	-84.9	-81.4
Consumption (mW)	3.8	11.2**	6.5	0.6	1.1
E Efficiency (nJ/b)	15.2/3.8/3.9	11.2	6.5/6.7	0.6	1.1
Architecture	Sliding IF	DC	Sliding IF	Low IF	No LNA
Rx area (mm^2)	1.6	2.9	2.9	0.7	2.1
External components	YES	NO	YES	YES	NO
Reference	(a)	(b)	(c)	(d)	(e)

$*$ Estimated from paper results.

$**$complete receiver front-end, ADCs, synthesizer, baseband and microprocessor.

(a) (LIU et al., 2013) (b)(PRUMMEL et al., 2015) (c) (WONG et al., 2012) (d) (SELVAKUMAR; ZARGHAM; LISCIDINI, 2015) (e) (MASUCH; DELGADO-RESTITUTO, 2013)

Source: the Author.

3 BLUETOOTH LOW ENERGY RECEIVER REQUIREMENTS

This chapter describes system-level requirements for a Bluetooth Low Energy receiver (Bluetooth Special Interest Group, 2010). Relaxed Bluetooth specifications were developed for the core system package denominated Bluetooth Low Energy in order to reduce power consumption when compared to the basic rate. Main differences are increased channel separation and reduction in interference performance and out-of-band blocking specifications.

The main receiver specifications for BLE are presented in Table 3.1. These specifications are discussed in more detail in the following sections.

Table 3.1: BLE specifications.

Preliminary specs		
BW	From literature references	1 MHz
Frequency range		2400.0 - 2483.5 MHz
1.SNR_{out}	From literature references	21 dB
2. Sensitivity	Required BER of 0.1 %	-70 dBm
3.Interference performance	Co-channel interference (C/I)	21 dB
	Adjacent (1 MHz) interference	15 dB
	Adjacent (2 MHz) interference	-17 dB
	Adjacent (¿= 3 MHz) interference	-27 dB
	Image frequency Interference	-9 dB
	Adjacent (1 MHz) interference to in-band image	-15 dB
4. Out of band Blocking	Interfering signal frequency	
	30 MHz – 2000 MHz	-30 dBm
	2003 – 2399 MHz	-35 dBm
	2484 – 2997 MHz	-35 dBm
	3000 MHz – 12.75 GHz	-30 dBm
5. Intermodulation	(F0) signal is 6 dB over sensitivity	
	(F1) sine wave	-50 dBm
	(F2) bluetooth signal (—F2-F1— = 3, 4, 5 MHz)	-50 dBm
6. Maximum input		-10 dBm

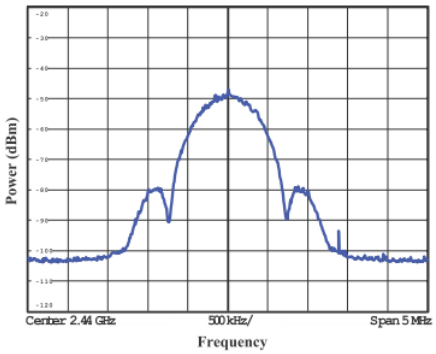
Source: the Author.

3.1 System-Level Considerations

3.1.1 Sensitivity

Proposed sensitivity of -70 dBm was specified for short distance application and reduced power consumption and, therefore is not challenging. BLE uses Gaussian Frequency Shift Keying (GFSK) modulation, with a bandwidth-bit period product (BT) of 0.5 and a modulation index of 0.45 to 0.55 . Its spectrum is presented in Figure 3.1 (ATAC et al., 2012).

Figure 3.1: Bluetooth Low Energy spectrum.



Source: ATAC et al. (2012)

According to (SCHIPHORST; HOEKSEMA; SLUMP, 2002), typical demodulation SNR_{out} for BLE may vary from 21 dB down to 15 dB . The best reported baseband demodulator indicates a minimum SNR of 11dB for the Bit-Error-Rate (BER) required by the standard of 0.1 % (SCHIPHORST; HOEKSEMA; SLUMP, 2003). Considering 21 dB required SNR_{out} and a bandwidth (B) of 1 MHz, noise floor and the (worst case) required NF are -114 dBm and 23 dB (Eq. 3.1 and 3.2) at 300 K.

$$Noisefloor = KTB = -114\,\text{dBm}(1\,\text{MHz}) \tag{3.1}$$

$$NF = S - KTB - SNR_{out} = 23\,\text{dB} \tag{3.2}$$

Figure 3.2 presents an ideal scenario with no interferers. Channel separation for BLE is relaxed to 2 MHz while it was previously 1 MHz for high performance Bluetooth.

High gain requirement depends on Analog-to-Digital Converter specification and will be discussed ahead.

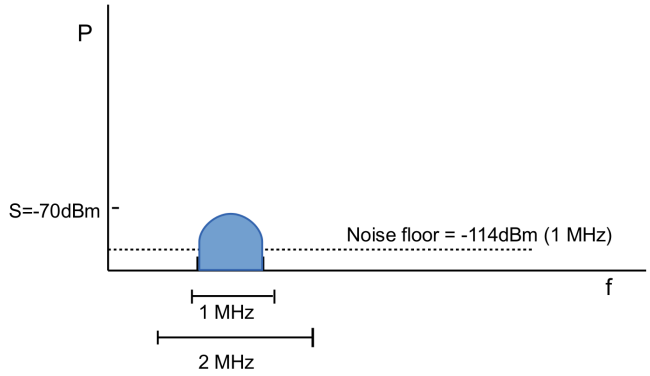
3.1.2 Linearity

Linearity is established by the standard in terms of interference performance, out-of-band blocking, intermodulation, and maximum input by BLE standard (Bluetooth Special Interest Group, 2010).

3.1.2.1 Interference Performance

Figure 3.3 presents graphically the worst interferers scenario defined by the standard in Table 3.1 (Bluetooth Special Interest Group, 2010; ATAC et al., 2012). During the

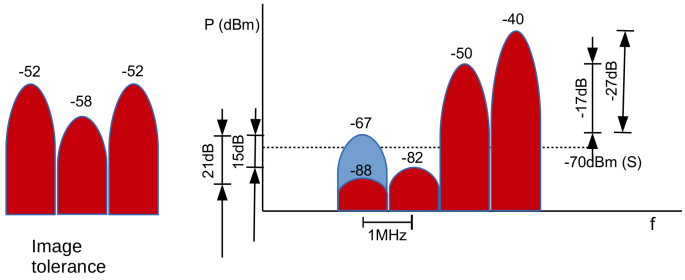
Figure 3.2: BLE sensitivity requirements.



Source: the Author.

interference performance test, a Bluetooth signal 3 dB higher than the sensitivity needs to be demodulated with a BER of 0.1 % in the presence of interferers defined by the mask.

Figure 3.3: Interference performance test.



Source: the Author.

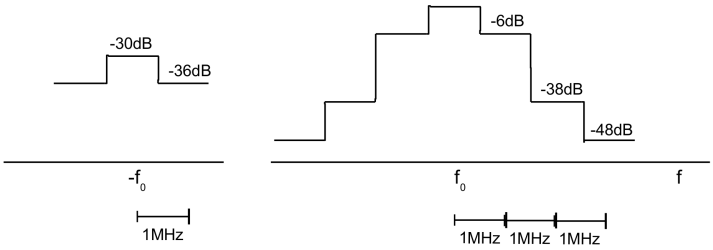
The main idea behind this test is to attenuate the blockers in order not to saturate the ADC. For the baseband filter requirements, a possible solution is to establish a filter mask that attenuates the blocker to the co-channel interference allowed by the standard, resulting in the mask presented in Figure 3.4 (ATAC et al., 2012). These requirements are very challenging for a low-power analog baseband filter and a minimum of six order low-pass filter would be needed. In the figure, the mask for the image filter is also presented on the left.

For an heterodyne receiver, or more specifically, a low IF receiver, the requirements for the IF filtering can be relaxed. It is still important to ensure that the interferers allowed by the standard in Figure 3.3 do not saturate the ADC.

Considering a maximum input of 0 dBm at the ADC, we can calculate the required attenuation of the IF filter using the equation 3.3. The test does not need to be performed using the maximum receiver gain. Consequently, part of the interferers dynamic range can be absorbed by the ADC, with a more relaxed filter mask. Adopting a gain of 44 dB for the calculation, the filter mask shown in Figure 3.5 is obtained.

$$At = P_{out(ADC)} - (P_{int} + gain) \tag{3.3}$$

Figure 3.4: BB filter requirements.

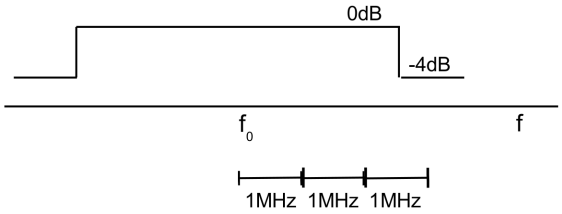


Source: the Author.

where $P_{out(ADC)}$ is the power delivered to the ADC, P_{int} is the allowed interferer power presented in Figure 3.3, $gain$ is the receiver gain used during the test.

In this case, before a downconversion to baseband, a complex signal is available and no image filter is required.

Figure 3.5: IF filter requirements.

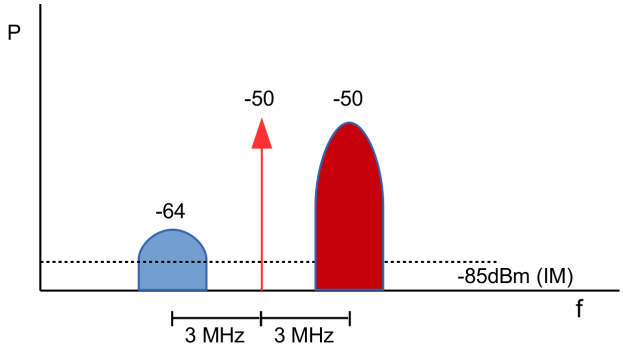


Source: the Author.

3.1.2.2 Intermodulation

According to the BLE standard, intermodulation is tested with the signal 6 dB higher than the sensitivity. One pure tone and a Bluetooth signal at -50 dBm are tested for intermodulation as shown in Figure 3.6.

Figure 3.6: BLE intermodulation requirements.



Source: the Author.

P_{IM3} and P_{IM2} limits are defined at the same level as the acceptable noise in the

channel in a test to detect a signal 6 dB higher than sensitivity (Eq. 3.4).

$$P_{IM3} = P_{IM2} = S + 6 - S/N_{out} \tag{3.4}$$

Considering the sensitivity proposed by the standard and the SNR_{out} of 21 dB, system requirements are defined by the equations 3.5 and 3.6.

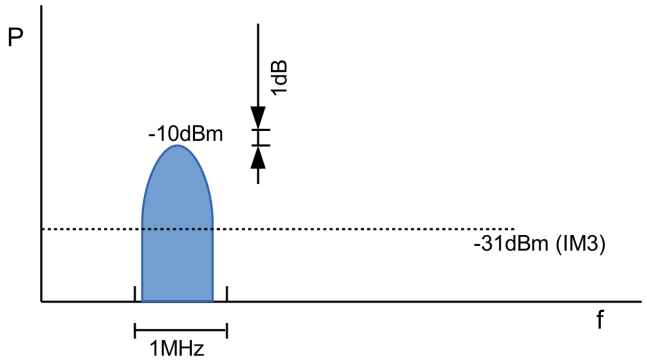
$$P_{IIP3} = \frac{3P_{interf} - P_{IM3}}{2} = \text{-32.5 dBm} \tag{3.5}$$

$$P_{IIP2} = 2P_{interf} - P_{IM2} = \text{-15 dBm} \tag{3.6}$$

3.1.2.3 Maximum Input

Under low gain assumptions, blocking conditions can be considered as a compression point equal to the maximum acceptable signal proposed by the standard (Figure 3.7), P_{1dB} = -10 dBm+1 dB. Resulting in a *low gain* IIP3 definition, $P_{IIP3} = P_{1dB} + 9.6 =$ 0.6 dBm.

Figure 3.7: Blocking sensitivity at low gain.



Source: the Author.

3.1.2.4 Out-of-band Blocking

Out-of-band (OOB) blocking is mainly defined in the system by IF filtering and LNA. The BLE standard also defines the required signal for the blocking test as 3 dB above sensitivity at the central frequency of 2440 MHz, as presented with the filter mask in Fig.3.8.

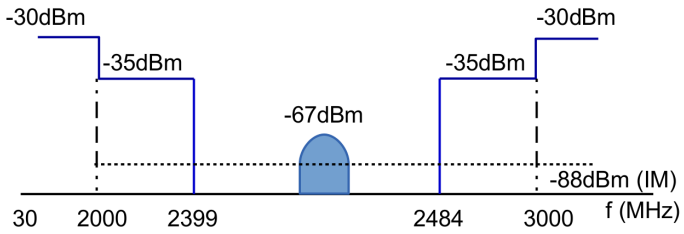
To analyze the compression due to the blockers, we can start from the output signal at the carrier frequency given by Eq. 3.7 (from analysis in Section 2.1.3.1).

$$v_{out} = \left(a_1 v_1 + a_3 \frac{3}{4} v_1^3 + a_3 \frac{3}{2} v_1 v_{interf}^2 \right) \cos \omega_1 t \tag{3.7}$$

where v_1 is the carrier and $v_{interf} = v_2$ is the blocker defined by the mask.

The second term in Eq.3.7 can be ignored since the carrier is much smaller than the blocker, and we can estimate the compression (or reduction) in the gain due to the blocker as:

Figure 3.8: BLE out-of-band blocking.



Source: the Author.

$$\Delta gain \simeq 1 - \frac{3}{2}\frac{|a_3|}{a_1}v_{interf}^2 \tag{3.8}$$

Using the definition of v_{IIP3} given by Eq. 2.12, and the definition of decibel, it is easy to show that:

$$\Delta gain_{(dB)} \simeq 10\log_{10}\left(1 - 2.10^{(P_{interf}-P_{IIP3})/10}\right) \tag{3.9}$$

Considering a margin of 5 dB for compression in the -35 dBm mask to define the compression point (P_{1dB}), P_{IIP3} can be estimated as (Eq.2.16):

$$P_{IIP3} = -35\,\text{dBm} + 5\,\text{dB}(margin) + 9.6\,\text{dB} = -20.4\,\text{dBm} \tag{3.10}$$

A P_{IIP3} of -20.4 dBm resulting in an acceptable degradation of 0.3 dB in the gain from Eq.3.9. P_{IIP3} estimated by Eq.3.10 is a conservative value since LNA filtering and external were not considered in the analysis.

For the -30 dBm mask, LNA selectivity can offer a strong protection of 10 dB and the degradation would be even smaller, bringing the OOB IIP3 to around -30 dBm.

3.1.2.5 Phase Noise

During the downconversion process, not only the BLE signal is translated to IF, but also the interferers are multiplied by local oscillator clock and translated to a close frequency. In this mixing process, the phase noise of the oscillator is copied to the interferers and ends up increasing the noise at the frequency of interest as can be observed in Figure 3.9. In the figure, interferer in red receives a copy of the local oscillator phase noise and the noise 'skirt' corrupts the BLE signal in blue. This process is called reciprocal mixing and produces additional requirements for the oscillator, from the receiver point of view.

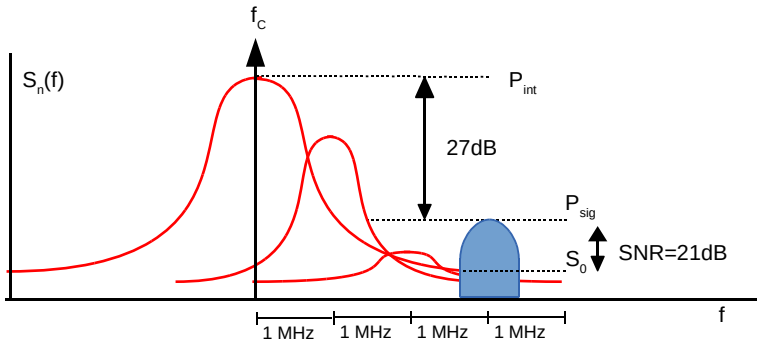
The required SNR_{out} of the signal after reciprocal mixing with the local oscillator can be represented by Eq. 3.11(RAZAVI, 2012):

$$SNR_{out} = \frac{P_{sig}}{S_0\,(Bw)} \tag{3.11}$$

where P_{sig} is the signal power requirement (equivalent to -67 dBm), Bw is BLE bandwidth of 1 MHz and S_0 is the noise density at the band of interest.

Eq. 3.11 can be rearranged to allow the direct calculation of the phase noise requirement below:

Figure 3.9: BLE phase noise requirement.



Source: the Author.

$$10\log_{10}\frac{S_0}{P_{int}} = -SNR_{out} - 10\log_{10} Bw - 10\log_{10}\frac{P_{int}}{P_{sig}} \tag{3.12}$$

In the equation P_{int}/P_{sig} is the relative level of the interferer to the signal accepted by the standard (Table 3.1). For a required SNR of 21 dB, the requirements of phase noise at $1\,$MHz, $2\,$MHz and $3\,$MHz are $-66\,$dBc/Hz, $-98\,$dBc/Hz and $-108\,$dBc/Hz respectively. The requirement at $1\,$MHz is intentionally mild because BLE channel separation is $2\,$MHz. Consequently, the requirements at $2\,$MHz and $3\,$MHz are the important phase noise requirements.

3.2 Summary

This chapter briefly derived the main system-level requirements for a BLE receiver. These relaxed requirements are summarized in Table 3.2 and can be easily surpassed by state-of-the-art receivers such as the works presented in Section 2.4.

Next chapter introduces the requirements for a very competitive BLE receiver. In order to be competitive the proposed receiver targets state-of-the-art noise figure, sensitivity, and IIP3, but with low power consumption, and high integration.

Table 3.2: BLE Standard system-level requirements.

	Standard requirements
Sensitivity	-70 dBm
Noise figure	23 dB
in band IIP3	-32.5 dBm
out-of-band IIP3	-30 dBm
Phase Noise at 2 MHz	-98 dBc/Hz

Source: the Author.

4 PROPOSED RECEIVER ARCHITECTURE

The design of a complete receiver for a specific standard involves several important steps. Initially, system-level figures of merit (gain, NF, IIP3) are defined to surpass BLE specifications presented in Table 3.1. In a second step, block-level figures of merit are divided among the blocks taking into account the cascaded effects presented in Section 2.1.4. Finally, block-level circuits are developed and integrated in the top-level.

The proposed receiver is a fully discrete-time high-IF receiver based on passive complex band-pass filters (Figure 4.1). High-IF approach was selected in order to reduce low-IF and direct conversion typical problems such as flicker noise and low IIP2.

In a discrete-time receiver, additional steps are necessary specially in low power design, for instance: definition of sampling rates, and analysis of possible aliasing in the decimation steps. Definition of an intermediate frequency (IF) is also a necessary step in the development of a high-IF receiver. Some trade-offs have to be considered in this step. IF frequency should be high enough to avoid flicker noise and IIP2 limitations and small enough to reduce the sampling rate of the ADC, and its power consumption. Additionally, selectivity of the filters may be related to IF frequency, as will be shown ahead in this chapter.

In the proposed architecture, required gain is provided by LNTA and inverter-type gain stages which are intercalated with passive switched capacitor (SC) filters. Out-of-band linearity is controlled by LNTA selectivity and careful choice of filters transfer functions. Passive mixers and passive filters are chosen due to their high linearity. An IF of $5\,\mathrm{MHz}$ was defined because the adopted passive filters have increased selectivity at lower IF frequencies and also to reduce the power consumption of the ADC.

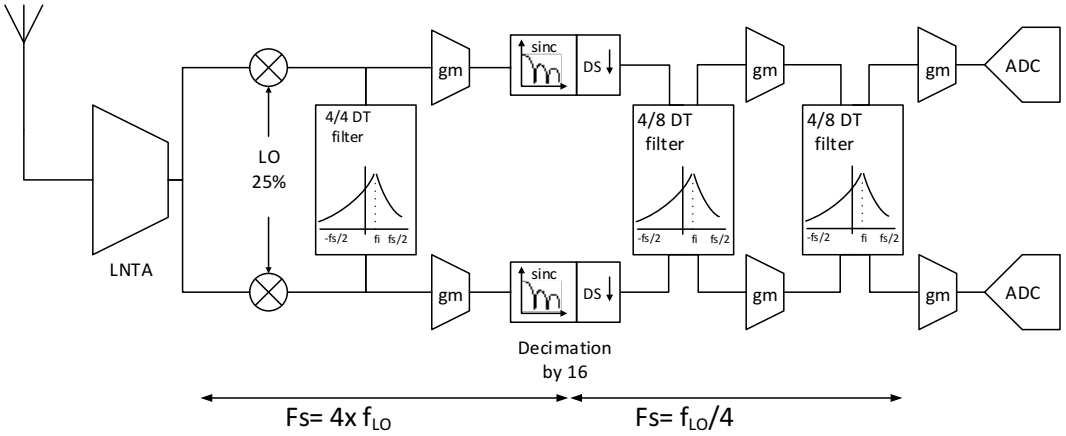
This architecture implementation is targeted for an advanced bulk CMOS technology. The electrical and layout designs were done for a 28 nm CMOS bulk PDK.

4.1 System-Level Figures

System-level figures obtained from standard requirements (Table 3.2) are quite relaxed and easily surpassed not only by state-of-the-art receivers but also by commercial products. Consequently, receiver requirements adopted in this design were defined to make it as competitive as state-of-the-art receivers presented in Table 2.1. Target NF and IIP3 were defined as 6 dB and -19 dBm, respectively, with a target power consumption of 2 mW.

To calculate the maximum gain of the receiver, it is necessary to estimate the desired sensitivity and to define the signal level for the ADC. Considering an SNR_{out} of 15 dB (Section 3.1.1), a sensitivity of -93 dBm can be estimated from Eq. 2.4. A maximum input of -10 dBm is also required by the standard resulting in a dynamic range of around 85 dB

Figure 4.1: BLE proposed architecture.



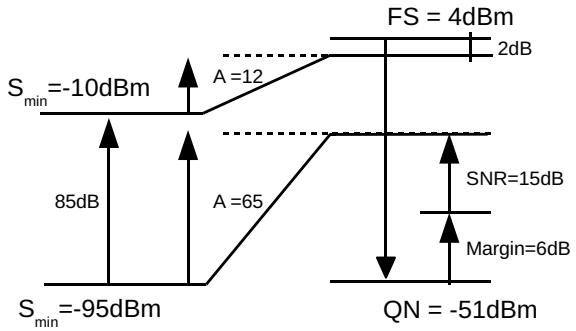
Source: the Author.

at the receiver input. A fraction of this DR can be absorbed by the ADC in order to reduce power consumption in the analog part (ABIDI, 2007).

A successive approximation register (SAR) topology was chosen for the ADC. In order to reduce power, the ADC uses larger input swing and a maximum signal of 4 dBm (= -9 dBVrms = 1 Vpp) was considered for input with a margin of 2 dB as shown in Figure 4.2. A resolution of 9 bits for the ADC corresponds to a dynamic range of 55 dB, resulting in a quantization noise (QN) of -51 dBm (= -64 dBVrms = 1.8 mVpp). The variable gain of 12 dB to 65 dB designed to accommodate the ADC dynamic range is also shown in the figure.

The system-level ADC requirements were developed in this work by the author. The electrical and layout designs of the ADC are not part of this thesis, however.

Figure 4.2: ADC specs.



Source: the Author.

Table 4.1 summarizes system-level requirements proposed for the receiver in order to achieve competitiveness with state-of-the-art BLE receivers.

In order to develop the block-level requirements it is necessary to understand clearly the trade-offs between gain, noise, linearity and power consumption for each one of the blocks. In this sense, the final cascaded distribution presented in Table 4.2 could only be achieved after some iteration during the development of the blocks that will be presented in detail in the next sections. In the table, individual gain, noise figure, and IIP3 were

Table 4.1: DT receiver system-level requirements.

	Design requirements
Voltage gain	65 dB
Noise figure	6 dB
IIP3	-19 dBm
Power consumption	2 mW

Source: the Author.

obtained through simulation using TSMC 28nm CMOS Process Design Kit (PDK). The cascaded results were estimated in a spreadsheet using Eq.2.19, 2.20, and 2.22.

The conventional IIP3 cascaded equation (Eq. 2.22) does not take into account the selectivity of the filters making the requirements tougher than necessary. An adapted version is presented in Eq. 4.1 and was implemented in the spread sheet. In the equation, two tones specified according to BLE filter masks are attenuated by filter selectivity in order to give a more realistic value.

$$IIP3_{dBm} = -10log10(10^{\frac{IIP3_1}{10}} + \\ + 10^{\frac{-IIP3_2+Gain_1-At_{1,f1}-0.5At_{1,f2}}{10}} + 10^{\frac{-IIP3_3+Gain_1+Gain2-At_{2,f1}-0.5At_{2,f2}}{10}}) \quad (4.1)$$

where $IIP3_k$ and $Gain_k$ are 3rd intercept point in dBm and gain in dB for the kth block, and $At_{k,f1}$ and $At_{k,f2}$ are the attenuation in dB of the tone tests 1 and 2 considering the effective filtering at the kth block. In Table 4.2 both *out-of-band* IIP3 and *in-band* IIP3 calculations are presented taking into account the different masks proposed by the standard. As it was expected, OOB IIP3 is due mainly to the LNTA block.

Noise Figure and IIP3 for LNTA, mixer and first filter were simulated together in the same test bench, so their individual results are not presented in Table 4.2.

Table 4.2: High gain block-level requirements.

Max Gain	LNTA	Mixer	Filter	gm	Filter	gm2	Filter	gm3	Rx
Power Gain (dB)	18								
Voltage Gain (dB)	31	-6		10.5	0	10.5	0	20	65
NF (dB)			5.5	16	13	16	13	13	
IIP3 (dBm)			-17.5	40	20	40	20	40	
Cascaded									
Gain (dB)	31	24	24	34.5	34.5	45	45	65	
F			3.5	3.7	3.7	3.7	3.7	3.7	
NF (dB)			5.5	5.7	5.7	5.7	5.7	5.7	5.7
In-band IIP3 (dBm)			-17.5	-17.5	-18.4	-18.4	-19.1	-19.1	-19.1
OOB IIP3 (dBm)			-17.5	-17.5	-17.5	-17.5	-17.5	-17.5	-17.5

Source: the Author.

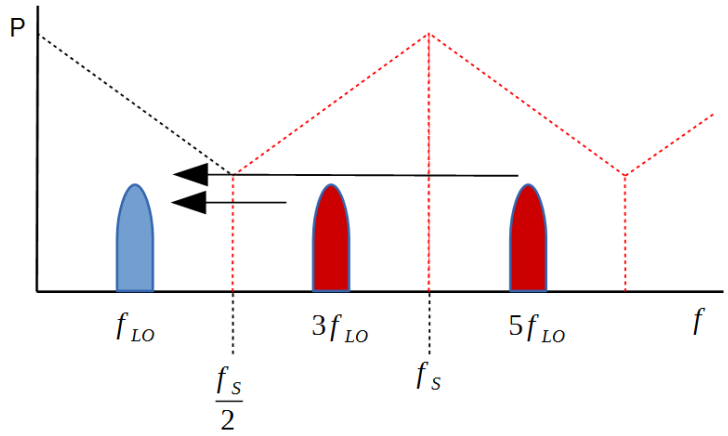
4.2 Receiver Architecture

Receiver concept introduced in Figure 4.1 is presented in this section. Initially, full-rate operation aiming to reduce aliasing and improve OOB filtering is presented. Later, IF filtering at a clock decimated by 16 in order to reduce power consumption is presented. Downsampling or decimation is simply performed by reducing the clock with a consequent integration of 16 samples in a moving average architecture, with a sinc-type shape and its consequent anti-aliasing effect as observed in Section 2.3.3.

4.2.1 Full-rate Operation

In the first part of the receiver architecture presented in Figure 4.1, the sampling mixer and the first filter (4/4 DT filter) are implemented at a sampling rate $4f_{LO}$ in order to reduce aliasing. Since the mixer operates at f_{LO}, odd multiples of f_{LO} are folded due to the sampling process, for instance $3f_{LO}$, $5f_{LO}$, and so forth as shown in Figure 4.3.

Figure 4.3: Front-end aliasing due to mixer sampling.



Source: the Author.

These aliasing frequencies need to be protected according to the OOB blocking mask as defined by the standard (Table 3.1). Figure 4.4 shows the highest blockers allowed at the frequencies $3f_{LO}$ and $5f_{LO}$. The OOB suppression is tested with a desired signal 3 dB higher than the reference sensitivity, at the center channel ($f_{ch} = 2440$ MHz) according to the standard. To attend this specification, a required attenuation of 58 dB at the aliasing frequency is given by Eq. 4.2, and should be provided by a combined anti-aliasing protection given mainly by LNTA selectivity and by the WIS filter created by the charge sampling mixer (Section 2.3.1).

$$Atten_{dB} = P_{interf} - (P_{sig} - SNR_{out}) \tag{4.2}$$

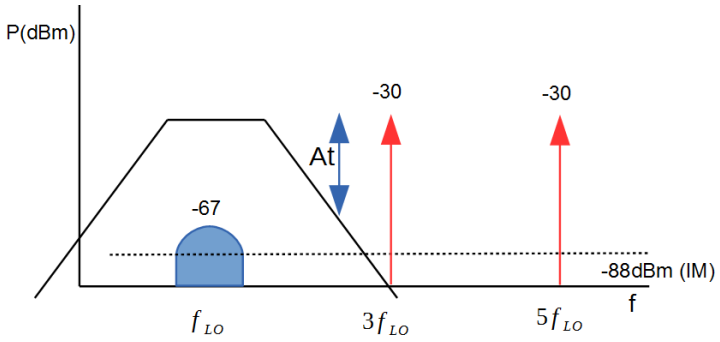
where P_{interf} and P_{sig} are interferer power and BLE standard test signal power shown if Figure 4.4 and SNR_{out} is the required SNR for detection (-21 dB in this calculation).

LNTA selectivity is mainly due to a second order RLC tank impedance given by Equation 4.3.

$$Z_T = \frac{RLs}{RLCs^2 + Ls + R} \tag{4.3}$$

where s is the complex frequency $j\omega$.

Figure 4.4: LNTA front-end filtering.



Source: the Author.

Consequently, LNTA impedance in square modulus equals to:

$$|Z_T|^2 = \frac{L^2\omega^2}{(1-LC\omega^2)^2 + \frac{L^2\omega^2}{R^2}}. \tag{4.4}$$

If resonance frequency of the tank is given by $\omega_{LO} = 1/\sqrt{LC}$ and At is the attenuation at $\omega = 3\omega_{LO}$, Equation 4.5 is obtained.

$$|Z_T|^2 = \frac{L^2\,(3\omega_{LO})^2}{\left(1-\frac{(3\omega_{LO})^2}{\omega_{LO}^2}\right)^2 + \frac{L^2(3\omega_{LO})^2}{R^2}} = \frac{R^2}{At^2} \tag{4.5}$$

The quality factor of a LC tank is given by $Q = R/L\omega_{LO}$ (RAZAVI, 2012) and from Eq. 4.5, attenuation at $3\omega_{LO}$ is given by:

$$At^2 = \frac{(1-9)^2 + 9/Q^2}{9/Q^2} \tag{4.6}$$

which corresponds to an attenuation of 28.5 dB for a LNTA of $Q = 10$, using high Q inductors implemented in the thick metal layer.

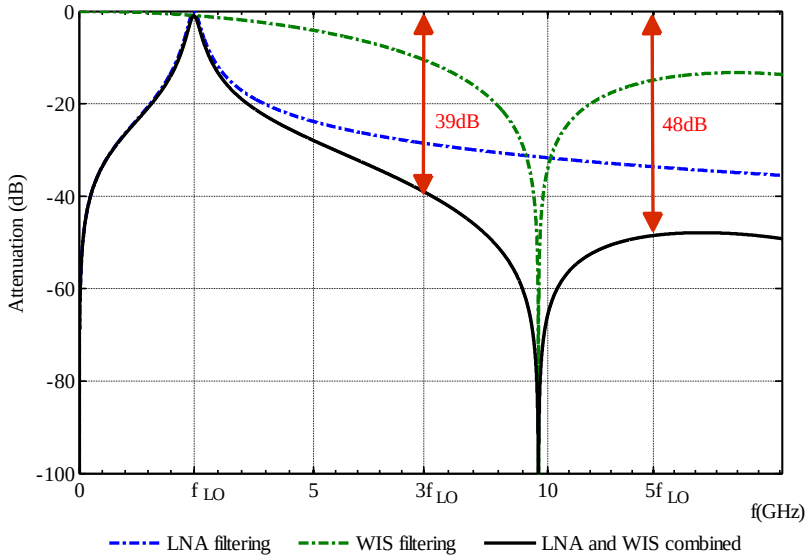
Figure 4.5 presents the combined effect of the LNTA selectivity and the window integrated sampling (WIS) filter created by the charge sampling mixer (Figure 4.1). The combined filter response was calculated using *Matlab* and shows the attenuation at these folding frequencies ($3f_{LO}$ and $5f_{LO}$) by 39 dB and 48 dB respectively. In the figure, a quality factor (Q) of 10 is assumed for the LNTA.

BLE standard also establishes that up to 10 exceptions are allowed in the OOB blocking mask. In 7 of these spurious response frequencies, a reduced level of -50 dBm is permitted resulting in 38 dB attenuation to prevent aliasing from Eq. 4.2.

It was also shown in (MIRZAEI et al., 2010; MIRZAEI; DARABI; MURPHY, 2011) that output load of a 25 % duty-cycle current-driven passive mixer is frequency translated to f_{LO}, $2f_{LO}$, $3f_{LO}$, ... at input, according to the Equation 4.7.

$$\begin{aligned} Z_{in}(\omega) \approx\ & R_{sw} + \tfrac{1}{4}Z_{BB}(\omega) \\ & + \tfrac{2}{\pi^2}\left[Z_{BB}(\omega-\omega_{LO}) + Z_{BB}(\omega+\omega_{LO})\right] \\ & + \tfrac{1}{\pi^2}\left[Z_{BB}(\omega-2\omega_{LO}) + Z_{BB}(\omega+2\omega_{LO})\right] \\ & + \tfrac{2}{9\pi^2}\left[Z_{BB}(\omega-3\omega_{LO}) + Z_{BB}(\omega+3\omega_{LO})\right] \\ & + \ldots \end{aligned} \tag{4.7}$$

Figure 4.5: Combined LNTA selectivity and charge sampling WIS filter effect. *(Matlab)*



Source: the Author.

This *impedance transformation* effect transform a low-Q baseband or IF impedance to a high-Q RF impedance offering an additional filtering protection.

In order to evaluate this additional filtering protection, we start from the transfer function of the 4/4 (IIR) DT Filter presented in Figure 4.1 described by Equations 4.8 and 4.9 (MADADI; TOHIDIAN; STASZEWSKI, 2013). The transfer function will be obtained in detail in Chapter 5, when the filter design is presented.

$$H(z) = \frac{k}{1 - [\alpha + j\,(1-\alpha)]\,z^{-1}} \tag{4.8}$$

$$k = \frac{1}{C_H + C_R},\ \alpha = \frac{C_H}{C_H + C_R} \tag{4.9}$$

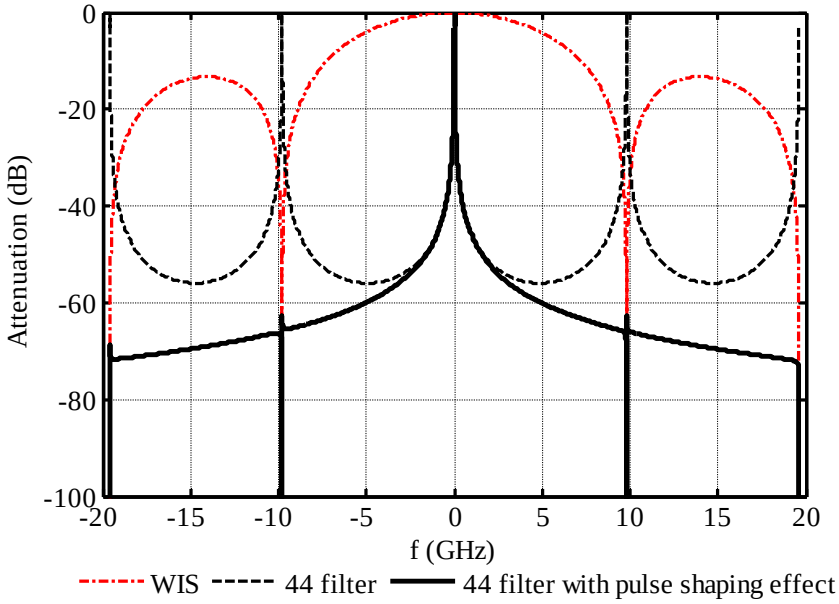
In the implementation, the filter is also affected by pulse shaping (WIS filter, Eq. 2.27) and it is sampled at the same rate as the sampling mixer ($4x f_{LO}$). Figure 4.6 presents the combined transfer function of the 4/4 filter and its own pulse shaping effect (Eq. 4.8 and 2.27).

When LNTA selectivity is combined with 4/4 filter, pulse shaping effect and mixer translation the complete filtering effect offered by the full-rate stage can be estimated in Figure 4.7. In the figure, the multiples of the sampling rate $fs = 4f_{LO}$ which will be folded to baseband are shown to be sufficiently attenuated, with around 100 dB of attenuation.

4.2.2 IF Filtering at Decimated Clock

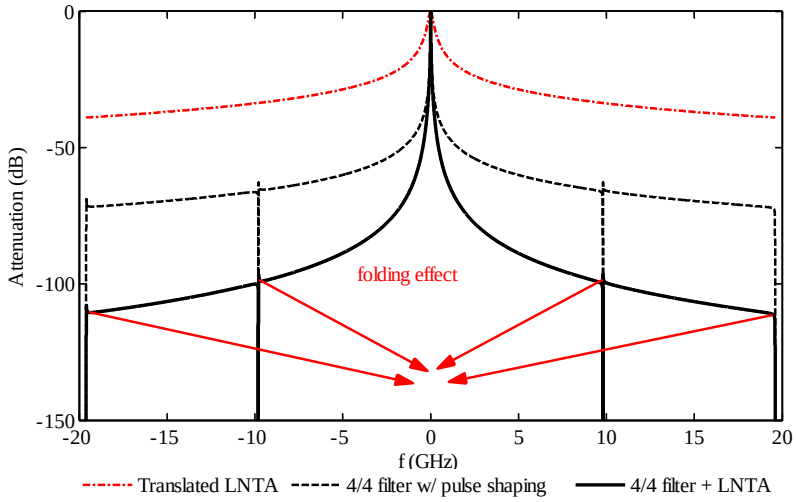
Unlike the full-rate operation section, the main function of the IF filtering section is to prepare for the ADC sampling. Consequently, it is characterized by filters of higher selectively, complexity and a consequent increase in power consumption, as well as gain stages. Equations 4.10 and 4.11 describe the transfer function of the 4/8 IIR filter that will be presented in detail in Chapter 5. Like the 4/4 IIR filter transfer function presented before, the 4/8 IIR filter is also affected by pulse shaping (Eq. 2.27) with $fs = f_{LO}/4$ and the combined transfer function is presented in Figure 4.8.

Figure 4.6: Pulse shaping effect in the 4/4 filter transfer function. *(Matlab)*



Source: the Author.

Figure 4.7: Full-rate front filtering effect. *(Matlab)*



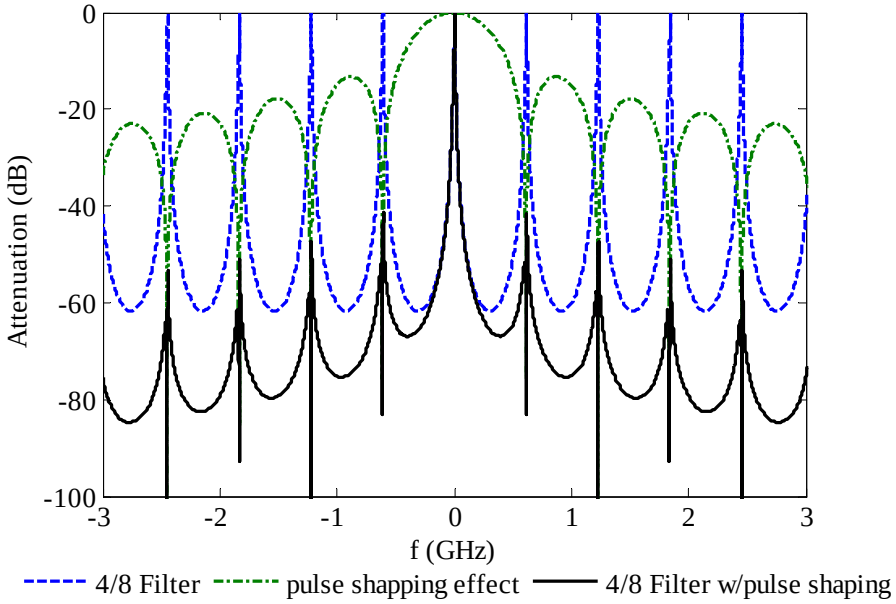
Source: the Author.

$$H(z) = \frac{V(z)}{Q(z)} = \frac{k}{(1-\alpha z^{-1})^2 - j\left[(1-\alpha)\, z^{-1}\right]^2} \tag{4.10}$$

$$k = \frac{1}{C_H + C_R},\ \alpha = \frac{C_H}{C_H + C_R} \tag{4.11}$$

In the beginning of the IF processing, there is a clock decimation by 16 to reduce power consumption. This decimation is implemented just by reducing the clock and

Figure 4.8: Filter 4/8 with pulse shaping effect. *(Matlab)*



Source: the Author.

consequently integrating 16 samples, which creates an anti-aliasing sinc-type filter with transfer function presented in Eq. 4.12. It is called *sinc-type* because its transfer function is similar to a sinc transfer function (BAGHERI et al., 2006b).

$$H(z) = \frac{1 - z^{-16}}{1 - z^{-1}} \Rightarrow |H(f)| = |\frac{sin(\pi f\, 16/fs)}{sin(\pi f/fs)}| \tag{4.12}$$

Attenuation of the anti-aliasing filter for a bandwidth B at the kth null is given by Eq. 4.13 (ABIDI, 2007).

$$H_B(kfs) \approx \frac{B}{kfs} \tag{4.13}$$

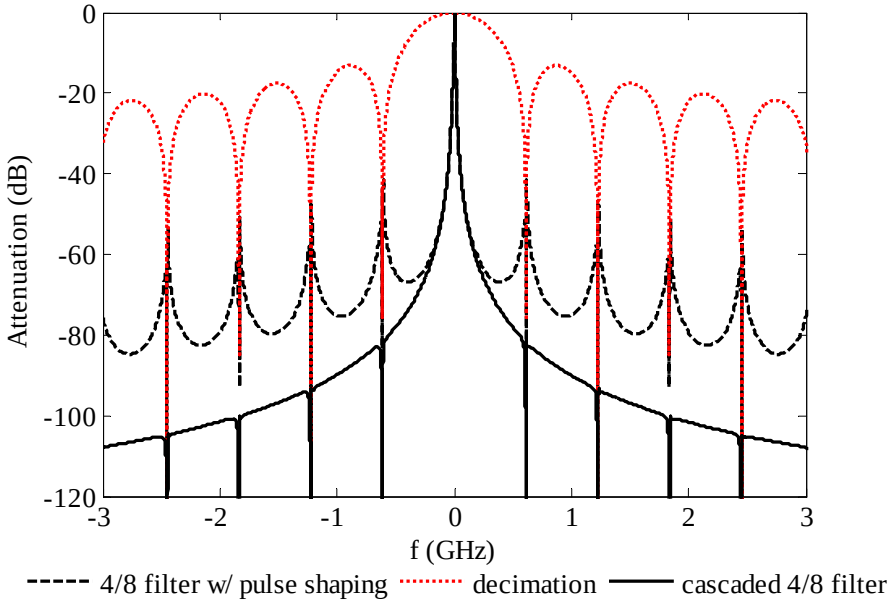
where fs is the sampling rate before decimation.

For $fs = f_{LO}/4 = 612.5$ MHz, IF of 5 MHz and a signal of 1 MHz, we can estimate a bandwidth B of 20 MHz with margin, which results in an attenuation of $20 \log 10 \left(\frac{B}{kfs}\right) \approx -30$ dB for the first null due to the decimation process. This attenuation is added to the pulse-shaping effect already presented by the filter, as well as the previous filtering stages.

The complete response of the 4/8 filter combined with pulse shaping and decimation can be observed in Figure 4.9.

The multiples of the sampling rate ($fs = 612.5$ MHz) in Figure 4.9 should be sufficiently attenuated in the receiver chain in order to avoid aliasing. This attenuation can be observed in detail in Figure 4.10 which shows the transfer functions of the WIS filter, the translated LNTA filter, the decimation filter, and the combined 4/4 filter. LNTA filter represents the filtering effect of the LNTA after translation to baseband. It is possible to observe the combined anti-aliasing effect of the three filters (LNTA, decimation, 4/4 filter), with a very good protection of around $83\,\text{dB} = 13\,\text{dB} + 30\,\text{dB} + 40\,\text{dB}$. The required protection in the worst case scenario happens with the last channel of BLE band

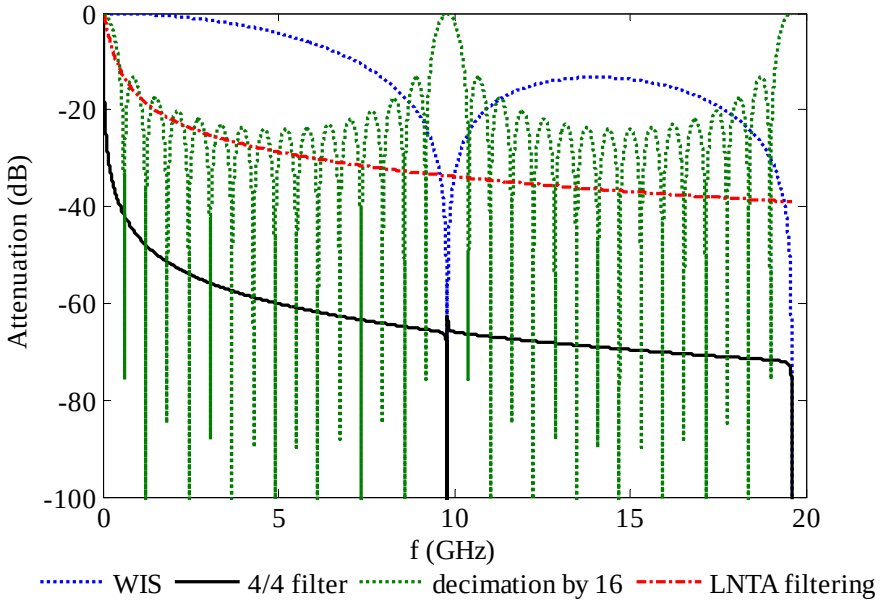
Figure 4.9: Filter 4/8 with pulse shaping effect and decimation. *(Matlab)*



Source: the Author.

which needs to be protected against an OOB blocker of 30 dBm, also with a requirement of 58 dB as calculated in Section 4.2.1.

Figure 4.10: Anti-aliasing protection FIR filter implemented by clock decimation by 16. *(Matlab)*



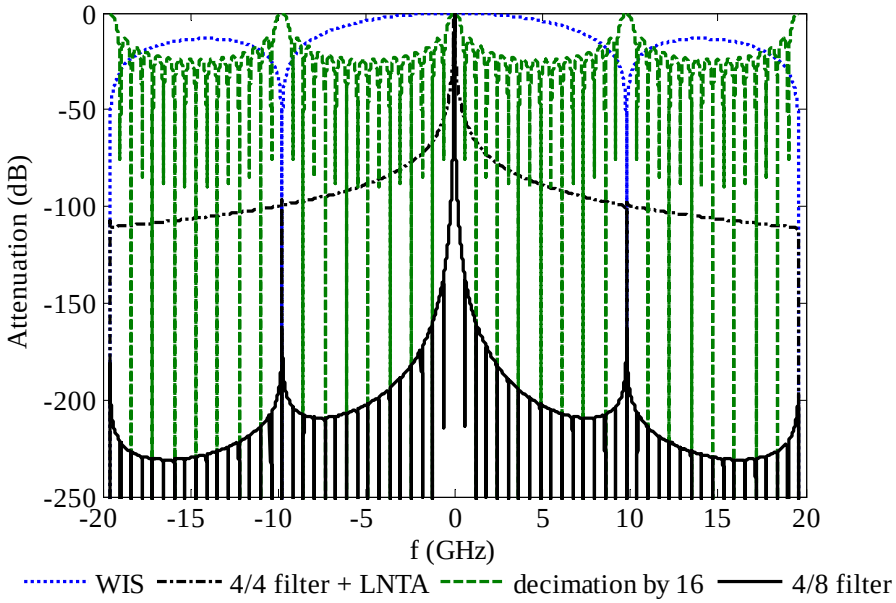
Source: the Author.

4.3 Top-level Signal Flow

Receiver top-level signal flow is summarized below using the DT signal processing described. In the development of the figures, only the equations presented in Section 4.2 were used.

Figure 4.11 presents the cascaded filtering obtained after the first 4/8 filter. It shows the good protection offered by the DT processing to the 4/8 filter. Figure 4.12 shows a zoomed version to present the first aliasing frequency of 612.5 MHz in detail.

Figure 4.11: IF complex filtering. *(Matlab)*

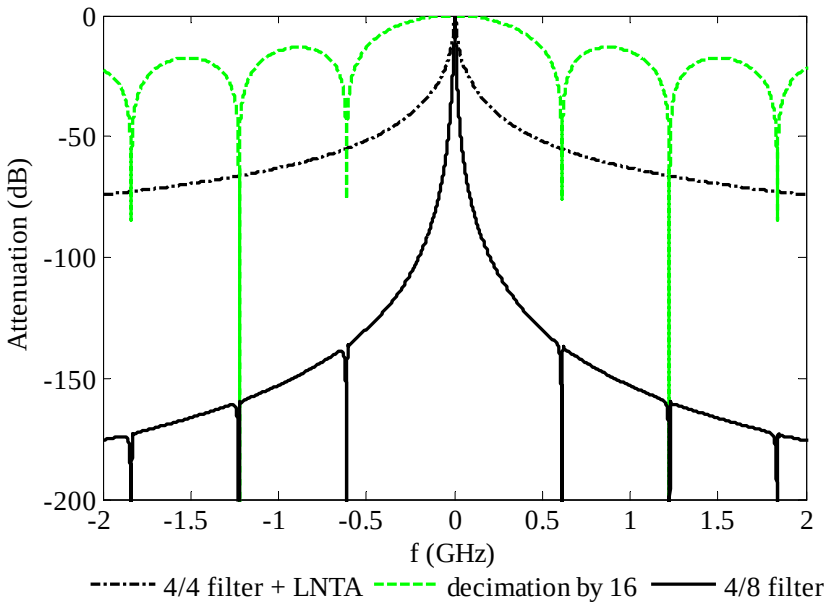


Source: the Author.

Figure 4.13 shows the final cascaded filtering obtained just before it is presented to the ADC. The main function of the last filter is to reduce the necessary dynamic range of the ADC by attenuating the interferers that are allowed by the standard masks. Figure 4.14 presents a zoomed version showing the three passive filters effect that result in a theoretical IF image rejection of about 31 dB. In practice, image rejection will be smaller due to practical implementation issues, mainly low output impedance of gm cells, for instance. A smaller resulting image rejection is acceptable since there will be also complex baseband processing.

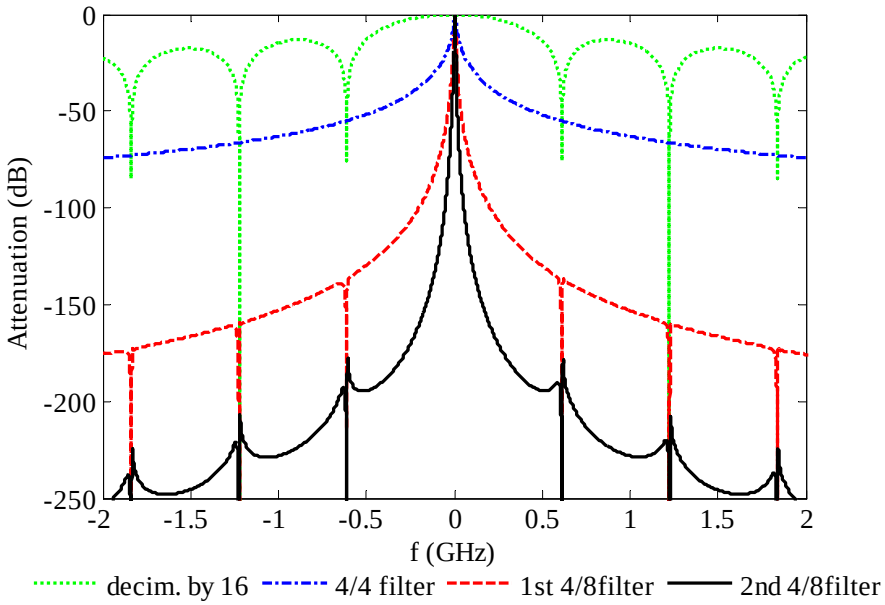
In order to complete the necessary filtering for the baseband and to satisfy the baseband interferers mask presented before (Figure 3.4), a 6th order low-pass Butterworth filter can be added. This filter should be added in the digital part of the receiver right after a complex demodulation to baseband, for instance using a Weaver approach. Figure 4.15 shows the complete filtering offered by the proposed complete solution. It shows a small attenuation of around 0.5 dB at the corners of the signal band due to the shape of the cascaded filters. Considering the BLE spectrum presented in Figure 3.1 which is well attenuated at the band extremities, the impact of this filter shape in the receiver sensitivity is expected to be very small.

Figure 4.12: IF complex filtering - zoom. *(Matlab)*



Source: the Author.

Figure 4.13: Cascaded IF complex filtering in the complete receiver chain. *(Matlab)*

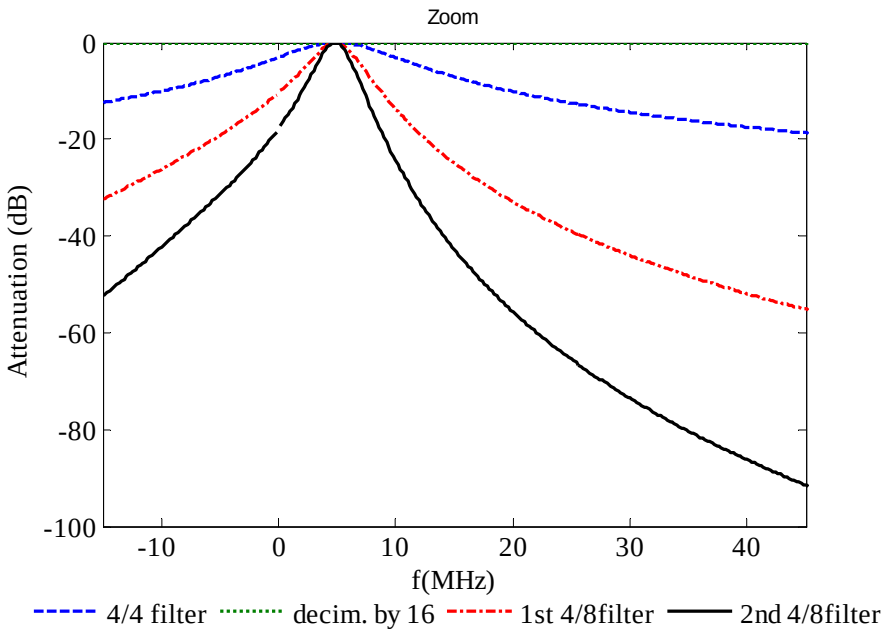


Source: the Author.

4.4 Summary

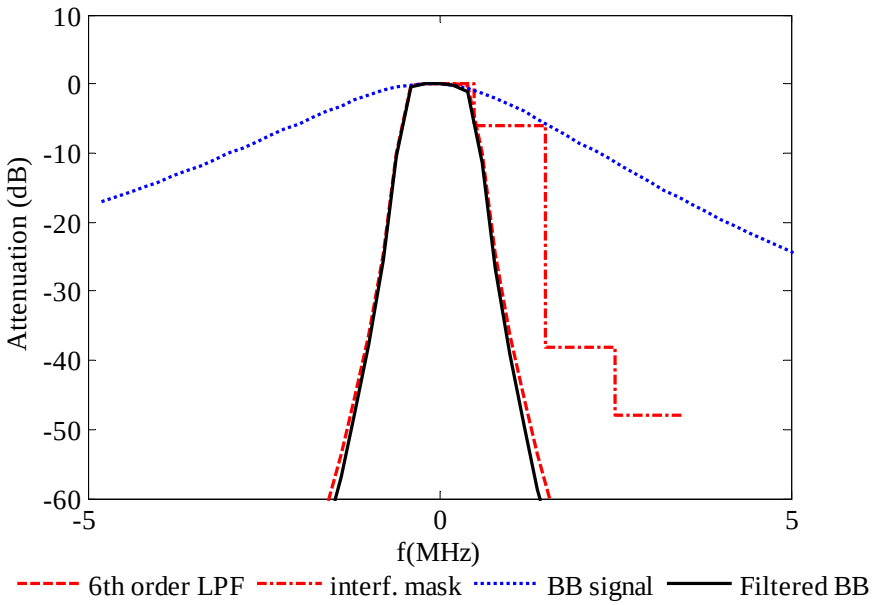
This chapter presented the proposed discrete-time architecture in detail as well as the decimation and pulse shaping effects that are part of the filtering process. The transfer function of each block is analyzed and cascaded in the receiver in order to estimate

Figure 4.14: IF complex filtering (zoom). *(Matlab)*



Source: the Author.

Figure 4.15: Baseband filtering. *(Matlab)*



Source: the Author.

the overall performance. The OOB blocking is performed by the first stage which is composed by LNTA, mixer and 4/4 filter and operates at the full sampling rate. The theoretical selectivity of the first stage enables the receiver to handle the OOB blockers proposed by the BLE standard without the need of external filters. The second stage operates at a decimated clock and is dedicated to prepare the received signal for the ADC acquisition. The

cascaded transfer functions show that the received signal after digital baseband processing respects the interferers mask.

5 DESIGN AND MEASUREMENT RESULTS

This Chapter presents the design of the blocks of the discrete-time receiver shown in Figure 4.1 with main specifications defined by system-level analysis in Table 4.2.

5.1 Block level Design

The proposed architecture (Figure 4.1) is composed mainly of gm stages, switches and capacitors, except for the LNTA and the common mode feedback (CMFB) amplifier that is part of the gm-cell. LNTA, gm-cells and amplifier were designed using the gm/Id methodology (SILVEIRA; FLANDRE; JESPERS, 1996; PAIXAO CORTES, 2008).

The gm/Id ratio versus the normalized current $i = i_D/(W/L)$ is a intrinsic characteristic and indicates the inversion level of the transistor (SILVEIRA; FLANDRE; JESPERS, 1996). In this design most of the blocks were polarized in moderate inversion to offer a good trade-off between power, speed and noise. Even though the gm/Id methodology itself was not the focus of this thesis, gm/Id (Figure 5.1), gds/Id (Figure 5.2), device specific capacitances (Figure 5.3), and noise coefficients γ/α and K_f (Figure 5.4) were extracted for different V_{ds} for several devices available in the 28nm LP Bulk CMOS PDK as proposed by FIORELLI MARTEGANI (2011). This approach proved very useful during block design in this technology.

The switches design as shown in this chapter is based on a desired resistance during operation to establish a specific time constant when charging the capacitors. In this sense, a good trade-off between resistance and power required to turn on the switch is achieved. Figure 5.5 shows the resistance dependency with width for the Low VT and Regular VT NMOS devices used in this design.

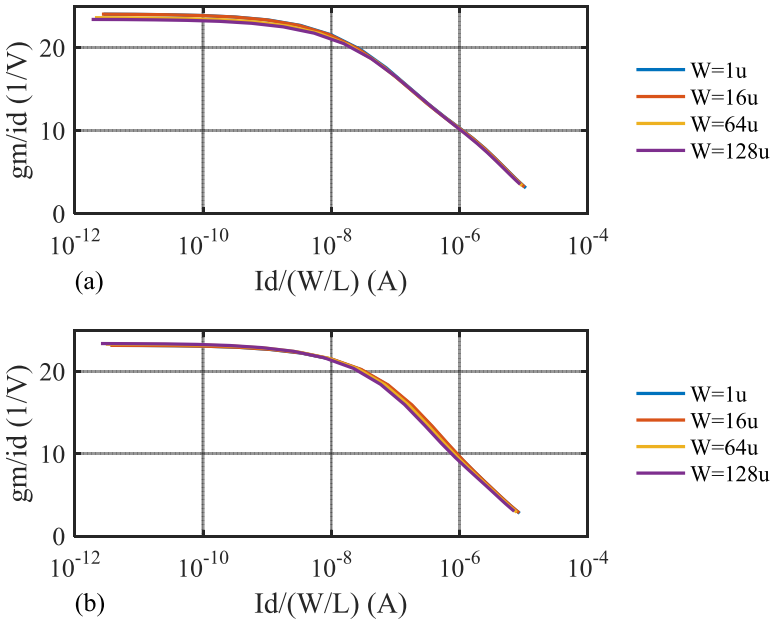
5.1.1 LNTA

The designed LNTA is composed of a traditional cascode LNA and a transconductor stage (Figure 5.6). The cascode LNA topology was selected since it offers the best trade-off between power and noise figure for narrow band applications. The narrow-band LNA design is based mainly on achieving input impedance matching to the antenna ($50\,\Omega$) and selective gain, both at the center frequency ω_0 of $2\pi 2.45$ GHz.

Input matching is implemented on-chip using a LC network composed by Lg, Ls and Cg. The input impedance (Z_{in}) of the LNA in the s domain is given by Eq 5.1(RAZAVI, 2012):

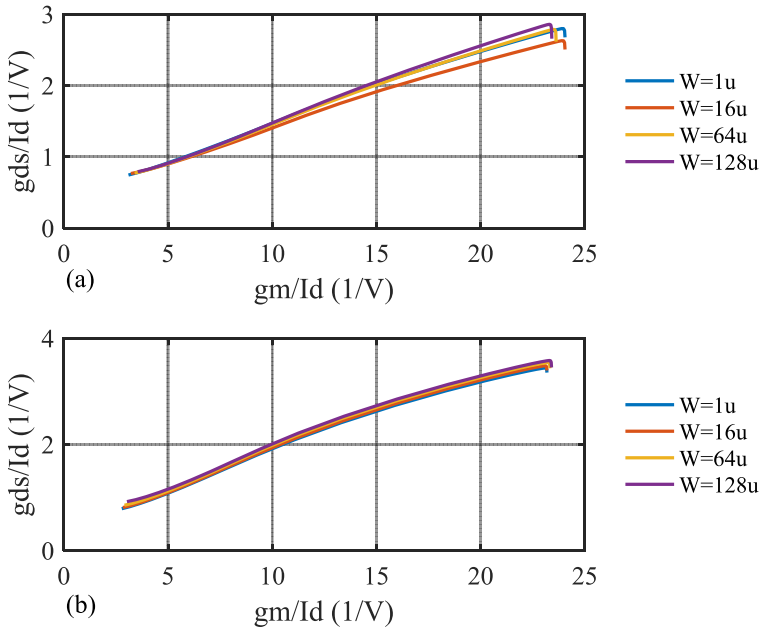
$$Z_{in}(s) \approx \frac{1}{s(Cgs_1 + Cg)} + s(Lg + Ls) + \frac{gm_1 Ls}{Cgs_1 + Cg} \tag{5.1}$$

Figure 5.1: (a) NMOS - gm/Id vs i (L=30 nm, V_{ds}=0.5 V) (b) PMOS - gm/Id vs i (L=30 nm, V_{ds}=0.5 V).



Source: the Author.

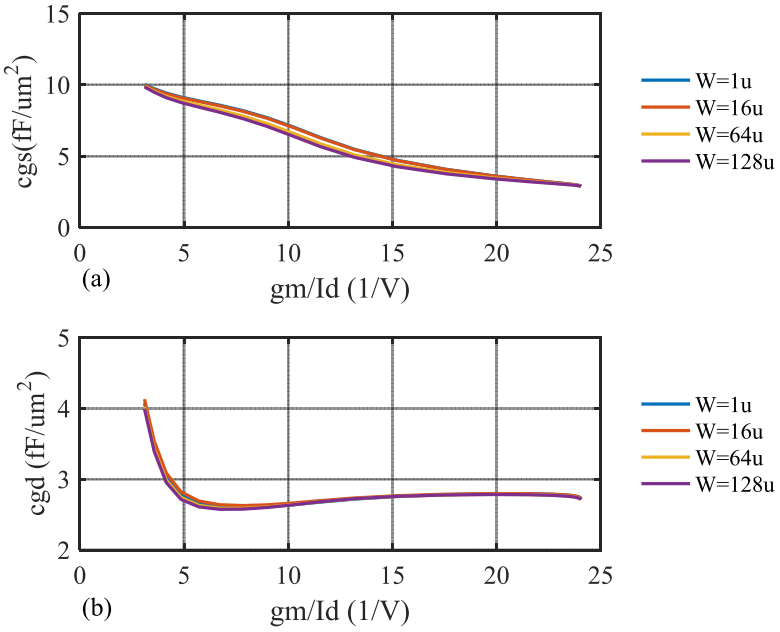
Figure 5.2: (a) NMOS - gds/Id vs gm/Id (L=30 nm, V_{ds}=0.5 V) (b) PMOS - gds/Id vs gm/Id (L=30 nm, V_{ds}=0.5 V).



Source: the Author.

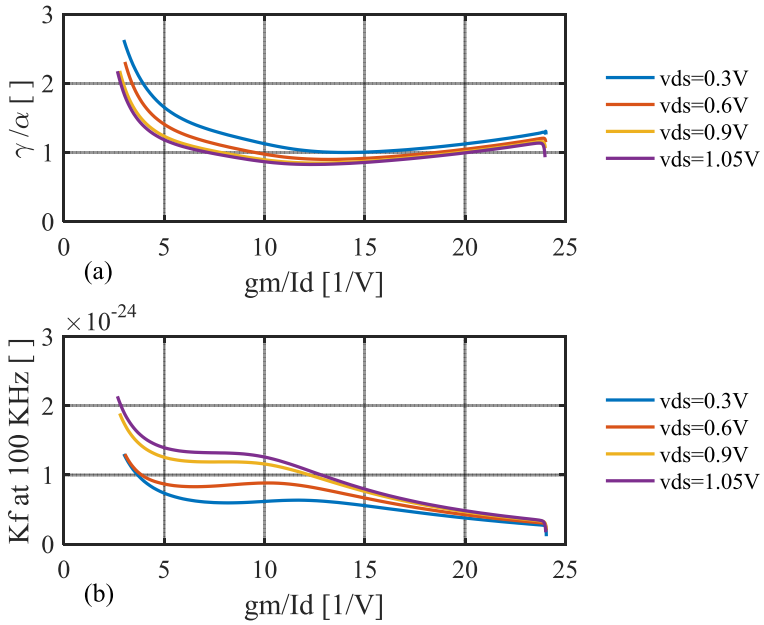
where Cgs_1 and gm_1 are gate-source capacitance of device M1 and its transconductance respectively, Lg and Ls are PDK inductors. Cg and Cd in Figure 5.6 are two capacitor banks that offer additional degrees of freedom in the design and allow for independent

Figure 5.3: (a) NMOS - Cgs capacitance vs gm/Id (L=30 nm, V_{ds}=0.5 V) (b) NMOS Cgd capacitance vs gm/Id (L=30 nm, V_{ds}=0.5 V).



Source: the Author.

Figure 5.4: (a) NMOS - thermal noise coefficient vs gm/Id (L=30 nm, W=2.4 um) (b) NMOS flicker noise coefficient vs gm/Id (L=30 nm, W=2.4 um).

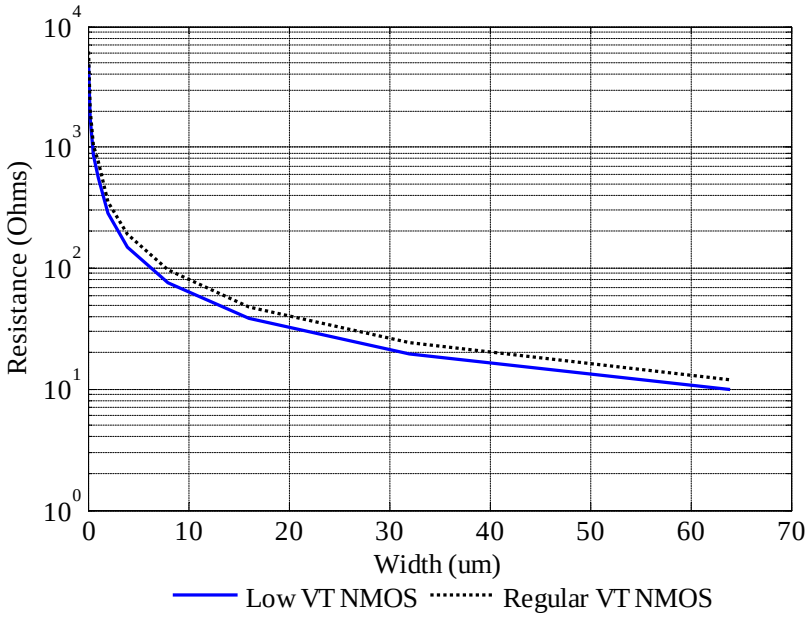


Source: the Author.

tune of input matching and load. Cg and Cd are implemented using metal-oxide-metal (MOM) capacitors available in TSMC 28nm CMOS.

In Eq. 5.1, the last term of the equation gives the resistance to be matched to the $50\,\Omega$

Figure 5.5: Switch resistance of regular V_T and low V_T NMOS device in conduction ($Vgs = 1.05$ V , $Vds = 0.1$ V, L = 30 nm) .



Source: the Author.

antenna and Cgs_1,Cg, Lg and Ls should resonate at the center frequency.

The gain of LNA (first stage of the LNTA) is defined as(SHAEFFER; LEE, 1997) :

$$Av = Q_{in} gm_1 R_{Ld} \tag{5.2}$$

where Q_{in} is the quality factor of the input network at ω_0, given by, gm_1 is the transconductance of M1 device and R_{Ld} is the parallel resistance of inductor Ld, given by $R_{Ld} = \omega_0.Ld.Q_{Ld}$, where $Q_{Ld} = 9$ is the quality factor of the PDK inductor Ld at ω_0.

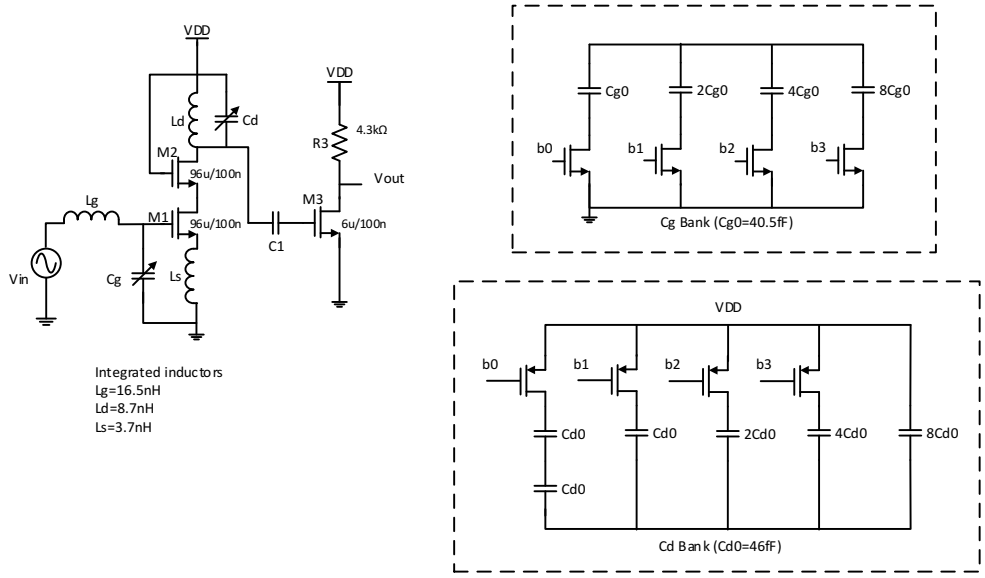
$$Q_{in} \approx \frac{1}{\left(Rs + \frac{gm_1 Ls}{Cgs_1 + Cg}\right) \omega_0 \left(Cgs_1 + Cg\right)} \tag{5.3}$$

In this design, M1 and M3 were biased in moderate inversion ($gm/I_d = 18$ and 12) in order to reduce power consumption with currents of 400 uA and 100 uA respectively using current mirrors not shown in Figure 5.6. Second stage is polarized close to strong inversion ($gm/I_d = 12$) in order to increase the output impedance of the LNTA.

Figure 5.7 presents simulation results of the designed gain, noise figure and S11 showing the LNTA is well tuned to the center frequency of the BLE band. Figure 5.7(b) shows the output impedance (Z_{22}) of $3.3\,\text{k}\Omega$ which is important for the transconductance implementation of the LNTA when loaded by the mixer and filter impedance of $1\,\text{k}\Omega$.

It is very difficult to achieve good linearity for a two stage LNTA. The first stage concentrates the gain in order to reduce the noise figure and severely impacts the linearity of the block (through Equation 2.22). The second stage is just responsible for converting voltage to current and to keep the output impedance high. IIP3 was simulated using PSS/PAC (Periodic Steady State /Periodic AC) analysis in schematic. Simulated input

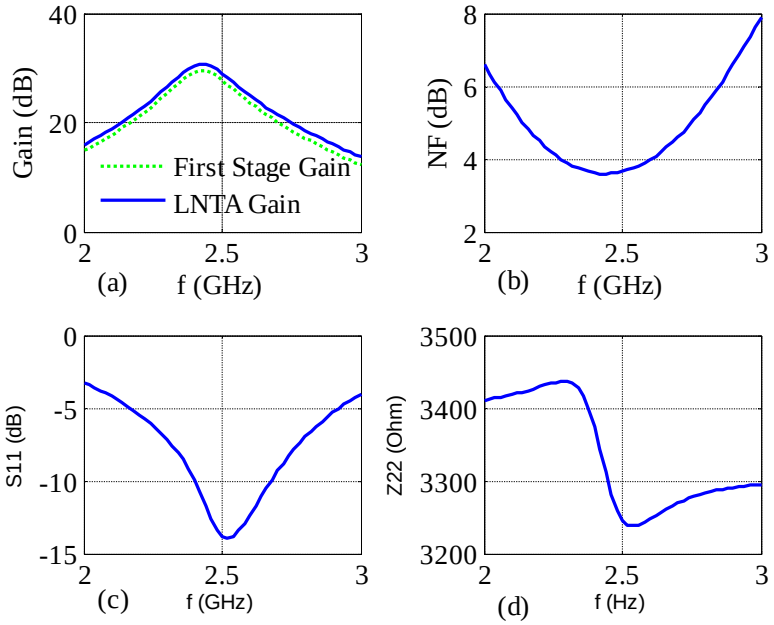
Figure 5.6: Schematics of LNTA and trimming capacitors.



Source: the Author.

IIP3 of -17.5 dBm is presented in Figure 5.8 which attends block requirements but is establishes a limit to the receiver linearity.

Figure 5.7: LNTA electrical simulation results: (a) gain; (b) NF; (c) S_{11}; (d) Z_{22}.

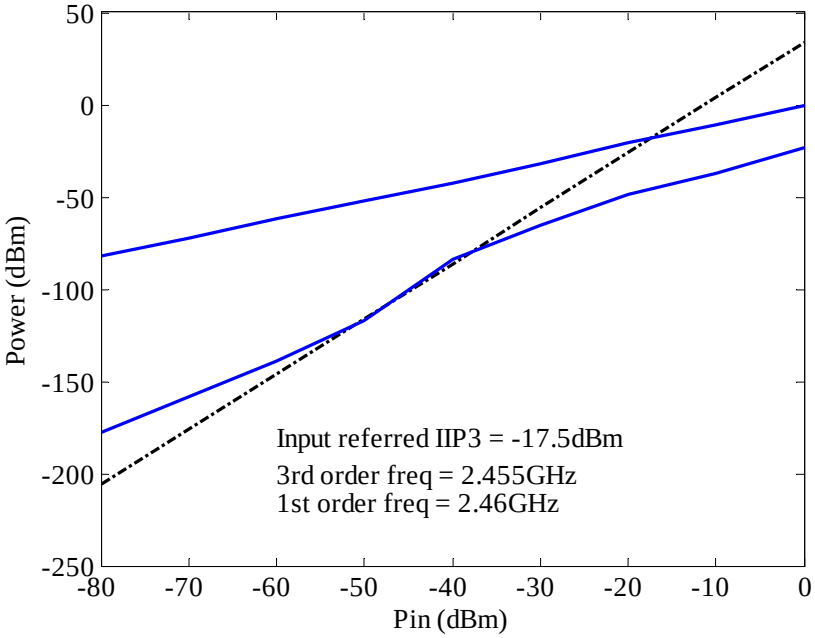


Source: the Author.

Transient simulation output with a power input of-80 dBm is presented in Figure 5.9 and shows LNTA start up and stability.

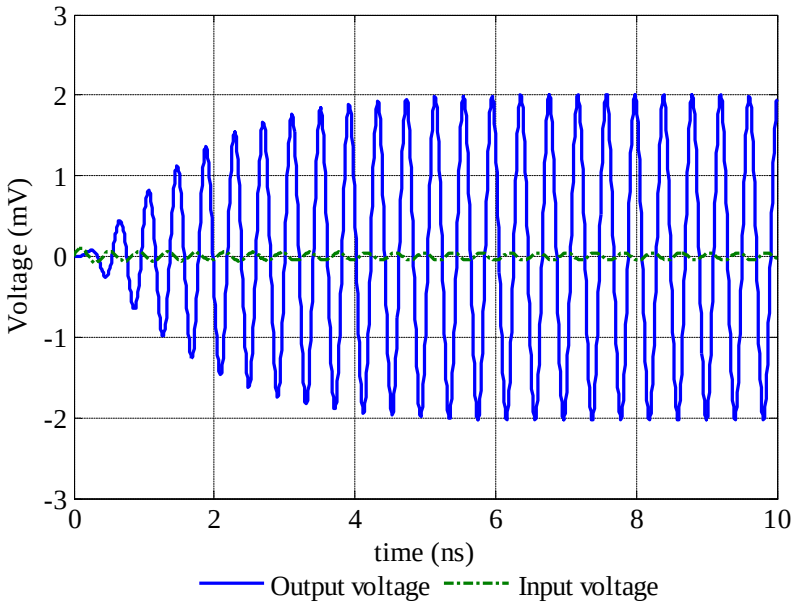
To account for process variations, Cg and Cd are implemented using 4-bit programmable banks with a variation of around 400 fF (Figure 5.6). Gain and S11 corners in Figure 5.10 show variation of the center frequency which can be corrected by adjusting Cd and Cg

Figure 5.8: LNTA input referred IIP3.



Source: the Author.

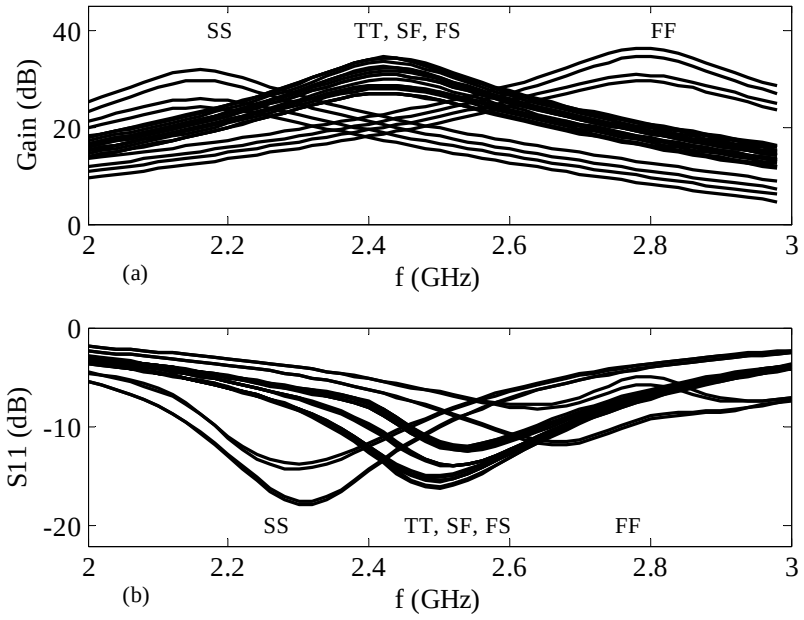
Figure 5.9: LNTA input and output transient.



Source: the Author.

respectively. Simulation was varied over process corners (TT, SS, FF, FS and SF), temperature (125, 27 and -40^{o}C) and voltage ($1.05\,\text{V} \pm 10\%$).

Figure 5.10: LNTA gain and S11 corners.



Source: the Author.

5.1.2 Sampling Mixer

Apart from traditional Gilbert cell mixers or passive voltage mixers, passive quadrature charge sampling mixers were introduced as a very good solution for RF sampling. When driven by 25 % duty-cycle quadrature clocks, these mixers show several advantages regarding cross-talk, flicker noise and linearity (MIRZAEI et al., 2010; KARVONEN; RILEY; KOSTAMOVAARA, 2000). As can be observed in Figure 5.11, the 25 % duty-cycle clock reduces drastically the overlap between phases (φ_1, φ_2, φ_3 and φ_4) with a consequent reduction in IQ cross-talk that is a traditional problem in 50 % duty-cycle quadrature mixers. A lower flicker noise corner is also observed as a reduced DC current is typically flowing on the switches of passive mixers. Additionally, the current operation and small voltage swing at the output contributes to a reduction in IIP2 and IIP3 numbers. The main disadvantage of the 25 % duty-cycle proposed mixer is the (current) conversion gain, estimated as $\sqrt{2}/\pi$ (MIRZAEI et al., 2010), which should be compensated by LNTA gain.

Figure 5.11 presents a simplified schematic of the designed passive quadrature sampling mixer and the 25 % clock strategy. The single-to-differential implementation allows the use of a single LNTA without the need of a balun, saving area and power. Design is basically performed by sizing mixer switches to obtain a good trade-off between power, noise and linearity. Passive mixers also allow current flow in both directions, with a consequent transparency between input and output. The input impedance of a quadrature passive mixer was studied in detail by ANDREWS; MOLNAR (2010) and is well represented by Equation 5.4.

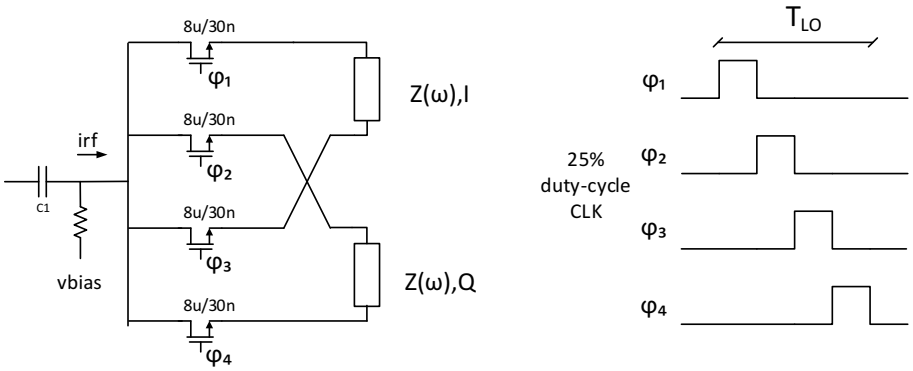
$$Z_{in}(s) = R_{sw} + \gamma_M Z_B(s) \| R_{sh} \tag{5.4}$$

where R_{sw} is the switch resistance, $\gamma_M = 2/\pi^2$ is a coefficient that accounts for the linear time-varying (LTV) effects, $Z_B(s)$ is the next stage impedance and R_{sh} is a shunt

resistance that accounts for the power loss of the harmonics in the up conversion through the switches.

For the current-mode implementation, the input impedance of the mixer was designed to be 3x smaller than LNTA output impedance (around $3.3\,\mathrm{k}\Omega$) presented in Figure 5.7. In this design, R_{sw} was set to $100\,\Omega$ corresponding to 10% of next stage input impedance. Figure 5.5 shows the resistance of a regular VT NMOS transistor during conduction with Vds equals to $100\,\mathrm{mV}$. This polarization was chosen because it improves the linearity of the following stage.

Figure 5.11: Quadrature sampling mixer.



Source: the Author.

As presented in Section 2.3.1, charge sampling also includes an anti-aliasing effect, implementing a WIS filter shown in Figure 4.5.

5.1.3 4/4 IQ Filter Design

The presence of a low-Q filter at the output of a charge sampling mixer creates a high Q band-pass at f_{LO} by means of frequency translation as presented in (MIRZAEI et al., 2010). This strategy improves OOB filtering, helping LNA selectivity and WIS filtering, and allowing for a SAW-less implementation. In the particular case of a band-pass filter at the IF frequency, it also improves image rejection.

Figure 5.12 presents a complex DT passive filter architecture proposed by (MADADI; TOHIDIAN; STASZEWSKI, 2013). The filter uses 4 rotating capacitors that are commuted in 4 different phases, so it was denominated 4/4 filter. The filter shares the charge at the differential input *I* with its quadrature output *Q* at different clock phases and vice-versa. Consequently, differential input and output are located at the same nodes.

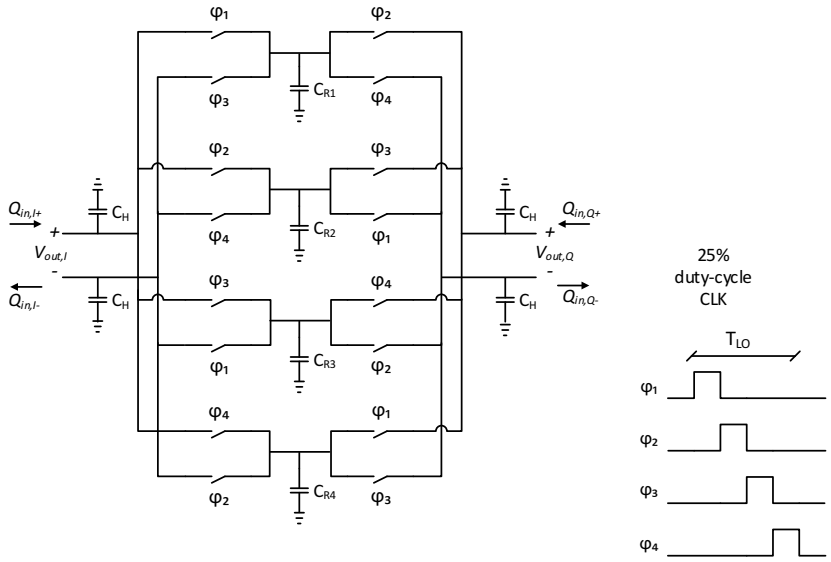
In the schematics, the differential input charge and output voltage in quadrature are given respectively by Eq. 5.5 and 5.6 below:

$$Q_{in} = Q_{in,I} + jQ_{in,Q} \tag{5.5}$$

$$V_{out} = V_{out,I} + jV_{out,Q} \tag{5.6}$$

Since the filter is based on rotating capacitors, we follow the same idea presented in Section 2.3 to calculate the voltage at the output $V_{out,I}$ at the instant n. The charge $Q_{in,I}$ transferred to the capacitors C_H and C_R at the instant n (at φ_1 pulse) is added to the previous voltage at the instant $n-1$ (at φ_4 pulse). $V_{out,I}[n]$ is a fraction of the voltage

Figure 5.12: 4/4 filter architecture.



Source: (MADADI; TOHIDIAN; STASZEWSKI, 2015).

available before at $V_{out,I}$ and $V_{out,Q}$ at the instant $[n-1]$, where α was given in Eq. 4.9, which is repeated below. In Figure 5.12, it is also possible to observe (visually) that there is an inversion in the polarity of the differential voltage $V_{out,I}$ at φ_1 and $V_{out,Q}$ at φ_4 (Eq. 5.7).

$$V_{out,I}\left[n\right] = \alpha V_{out,I}\left[n-1\right] - \left(1-\alpha\right) V_{out,Q}\left[n-1\right] + \frac{Q_{in,I}\left[n\right]}{C_H + C_R} \tag{5.7}$$

$$k = \frac{1}{C_H + C_R},\ \alpha = \frac{C_H}{C_H + C_R} \tag{4.9}$$

Now in the calculation of $V_{out,Q}[n]$, Figure 5.12 shows that there is no inversion in the polarity of the differential voltage $V_{out,Q}$ at φ_1 and $V_{out,I}$ at φ_4. Additionally, at the instant n the capacitors that participate in the charge sharing at input I are different than the capacitors that participate in the charge sharing at input Q, and the process occurs simultaneously.

$$V_{out,Q}\left[n\right] = \alpha V_{out,Q}\left[n-1\right] + \left(1-\alpha\right) V_{out,I}\left[n-1\right] + \frac{Q_{in,Q}\left[n\right]}{C_H + C_R} \tag{5.8}$$

Using equations 5.5 and 5.6 on the charge-sharing (CS) equations 5.7 and 5.8, we obtain the complex CS expression of the filter at the instant n and its *z-transform* version.

$$V_{out}\left[n\right] = \alpha V_{out}\left[n-1\right] + j\left(1-\alpha\right) V_{out}\left[n-1\right] + \frac{Q_{in}\left[n\right]}{C_H + C_R} \tag{5.9}$$

$$\left(1-\alpha z^{-1}\right) V_{out} = j\left(1-\alpha\right) z^{-1} V_{out} + \frac{Q_{in}}{C_H + C_R} \tag{5.10}$$

The resulting transfer function of the filter is given by Eq. 5.11 and Eq. 4.8 (already presented in Chapter 4).

$$H(z) = \frac{V(z)}{Q(z)} \tag{5.11}$$

$$H(z) = \frac{k}{1-[\alpha+j(1-\alpha)]z^{-1}} \tag{4.8}$$

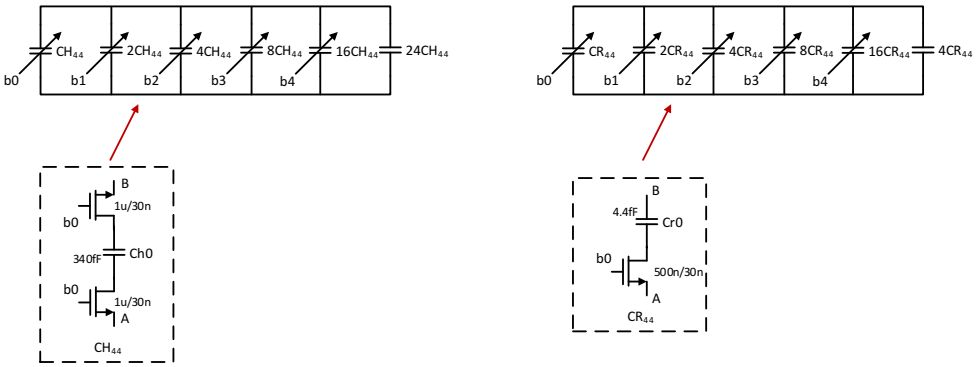
The input impedance of the filter and the center frequency are given by Eq.5.12 and 5.13, respectively.

$$Z_0 = {}^{1}/_{C_R f_s} \tag{5.12}$$

$$f_c = \frac{f_s}{2\pi} \arctan(\frac{C_R}{C_H}) \tag{5.13}$$

To account for PVT and offer flexibility in frequency tuning to the charge sharing (CS) filter, C_H and C_R are implemented using 5-bit capacitor banks presented in Figure 5.13. Combined banks enable an adjustment in the center frequency and in the input impedance from 1 to 14 MHz (from Eq. 5.13) and from $667\,\Omega$ to $4.67\,\text{k}\Omega$ (from Eq. 5.12). Change in the input impedance can be used to adjust quality factor and gain of the receiver, and compensate for temperature variations.

Figure 5.13: C_H and C_R capacitor banks.

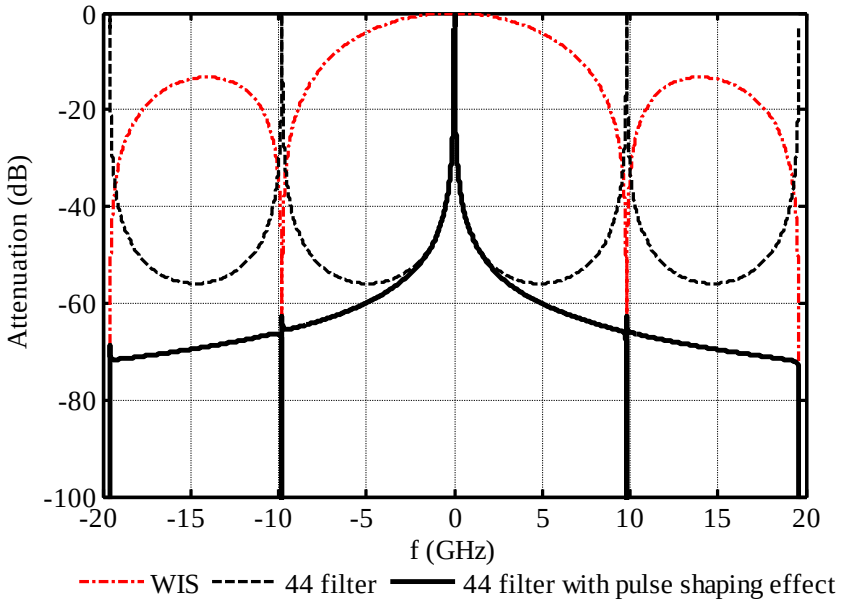


Source: the Author.

The transfer function of this IIR filter, Eq. 4.8, was already presented in Chapter 4 and is repeated below (Figure 4.6. As an IIR filter, sampled at 4x the local oscillator clock, it repeats the transfer function at multiples of $f_s = 4f_{LO}$ (9.8 GHz) and would produce aliasing. Fortunately, the rectangular pulse sampling introduces a WIS that works as an anti-aliasing filter, as we can easily observe in the figure.

Another interesting characteristic of this filter can be observed when we plot the 4/4 filter transfer function for three different center frequencies: 3 MHz, 5 MHz, and 10 MHz (Figure 5.14). For all the cases, the filter presents the same quality factor ($Q = 0.5$) with same attenuation of 7 dB at the image and 3 dB at 0 Hz. It suggests a trade-off in the implementation of the filter between distance to the flicker noise corner and selectivity of the filter.

Figure 4.6: Pulse shaping effect in the 4/4 filter transfer function. *(Matlab)*

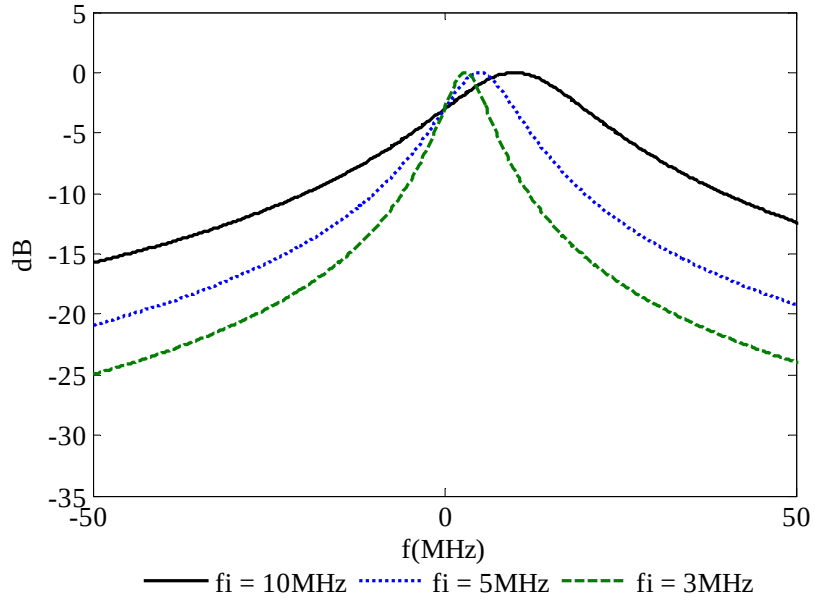


Source: the Author.

$$Q = \frac{f_0}{Bw} \tag{5.14}$$

where f_0 is the center frequency and Bw is the 3 dB bandwidth of the signal.

Figure 5.14: 4/4 filter transfer function. *(Matlab)*



Source: the Author.

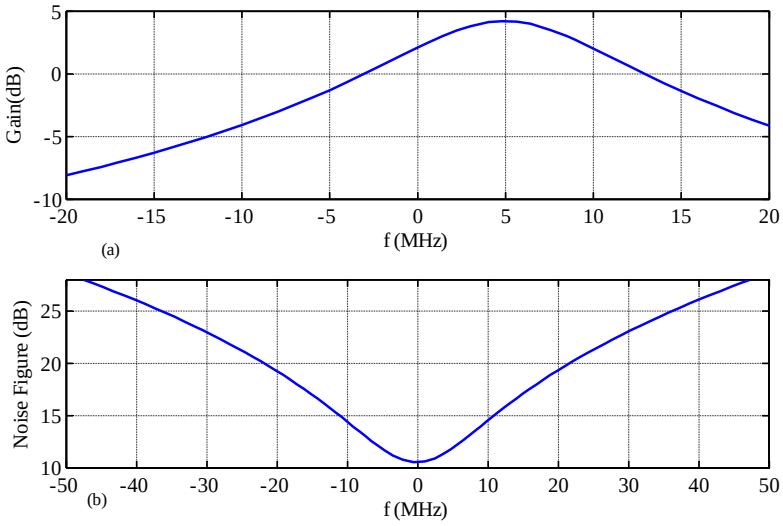
The 4/4 filter implemented operates at full sampling rate ($f_S = 4f_{LO}$) which is around 9.8 GHz. Switches are implemented using simple NMOS rf devices which are sized in order to minimize power consumption while not compromising filter linearity and quality factor.

The quality factor of the filter decreases when its impedance (Eq. 5.12) is not at least $3x$ smaller than the previous transconductor block (MADADI; TOHIDIAN; STASZEWSKI, 2015). Since LNTA output impedance is around $4\,\text{k}\Omega$ (Figure 5.7), a C_R of 100 fF is chosen resulting in $1\,\text{k}\Omega$ input impedance for the filter. C_H of 31 pF is calculated for a 5 MHz IF in Eq. 5.13 and is implemented differentially in order to reduce capacitor size.

According to (MADADI; TOHIDIAN; STASZEWSKI, 2015), in order to maximize linearity, $T_S = 1/f_S$ should be defined between 3τ to 4τ where $\tau = R_{sw}C_R$ is the time constant to charge C_R. Consequently, R_{sw} is calculated as $250\,\Omega < R_{sw} < 350\,\Omega$ with a resulting switch size of $3\,\mu$m x 30 nm from Figure 5.5.

Figure 5.15 present the schematics simulated gain and noise for the desired circuit when programmed for $IF = 5$ MHz. The maximum gain presented in the figure is not representative since the PSS/PAC simulation used a voltage port and consequently there is loading effect of the $50\,\Omega$ RF port, but the transfer function shape gives an indication of the correct transfer function of the filter.

Figure 5.15: Filter 4/4: (a) gain response; (b) noise figure.



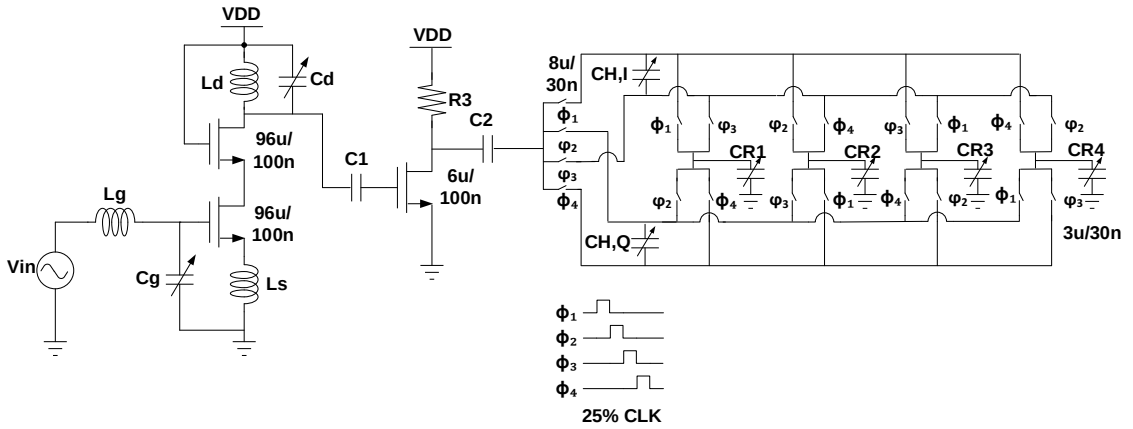
Source: the Author.

5.1.4 Full-rate Operation Section

LNTA, mixer and filter 4/4 have OOB blocking as the main function. Aliasing should be considered carefully as presented in Chapter 4. The full-rate operation section (Figure 5.16), being the first part of the receiver, is also the main responsible for the system noise figure and accounts for 24 dB of gain and 5 dB of noise figure as can be observed in Figure 5.18. It also limits the linearity since the worst linearity of the receiver is presented by the LNTA due to its high gain concentrated in the first part of the two stages (Figure 5.19).

The performance of the full-rate operation section was analyzed using a simplified testbench presented in Figure 5.17. In the testbench, Port1 represents the single-end an-

Figure 5.16: Full-rate Operation Section schematics.

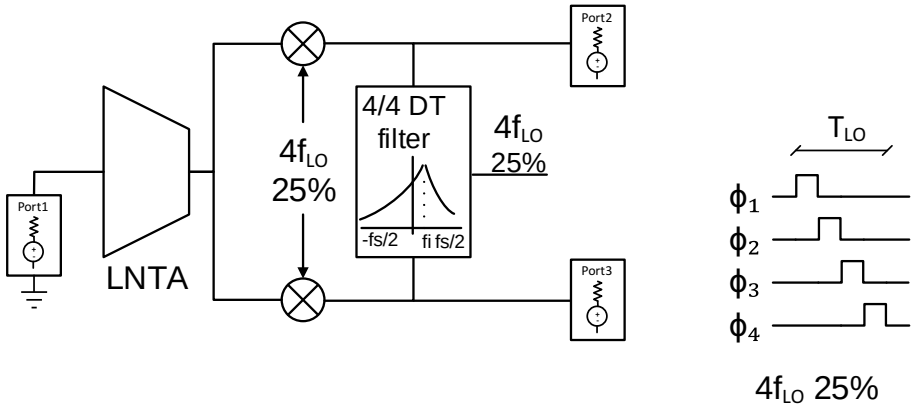


Source: Adapted from KUO et al. (2016).

tenna with $50\,\Omega$ impedance and Port2 and Port3 represent the connection with decimated clock IF stage which is considered with high impedance ($100\,\mathrm{k}\Omega$ differential in the testbench).

Schematic simulation results of gain, noise figure and linearity are presented in figures 5.18a, 5.18b, and 5.19 respectively. Gain was simulated using PSS/PAC, noise figure was simulated using Periodic Noise (PNOISE) and IIP3 was simulated using PSS/PAC analysis from SpectreRF. Gain of the section is composed mainly of LNTA gain (≈ 31 dB) presented before and mixer conversion loss (estimated as -6.9 dB) and accounts for 24 dB, shown in the Figure 5.18a.

Figure 5.17: Full-rate Operation Section simplified testbench.

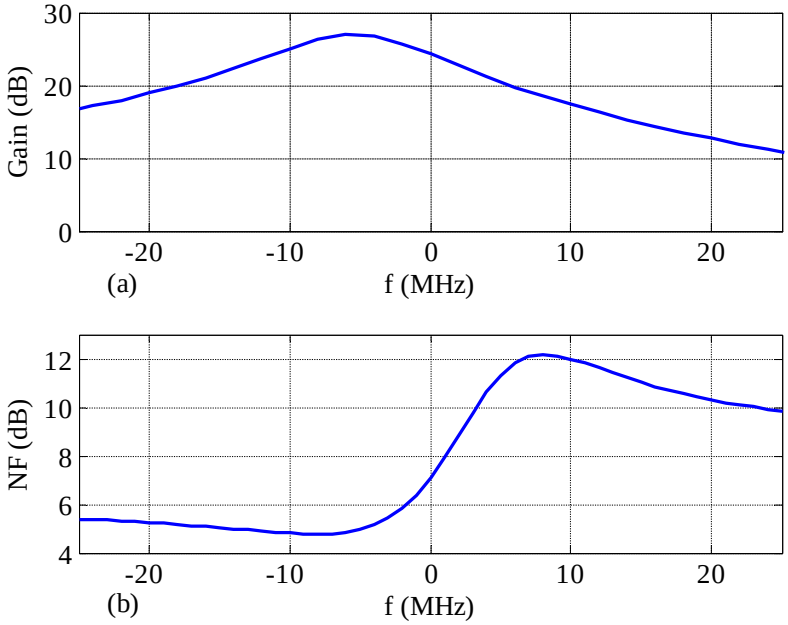


Source: the Author.

In Figure 5.18, the filter is centered in -5 MHz instead of the 5 MHz presented in Figure 5.15. This difference is due to the changing order of the filter phases. In the full receiver design implementation, the lower side band (LSB) was selected, which corresponds to the negative IF frequency.

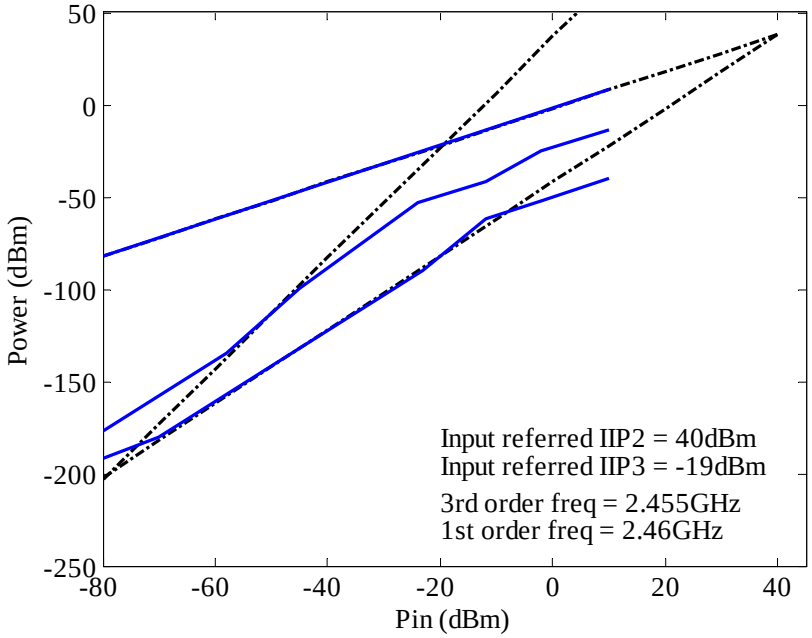
Due to the practical implementation of the LNTA as an ideal current source, the Q of the simulated filter is reduced and can be calculated as 0.42 from the Figure 5.18 and Eq. 5.14.

Figure 5.18: Full-rate Operation Section (a) gain; (b) noise figure.



Source: the Author.

Figure 5.19: Full-rate Operation Section input referred IIP2 and IIP3.

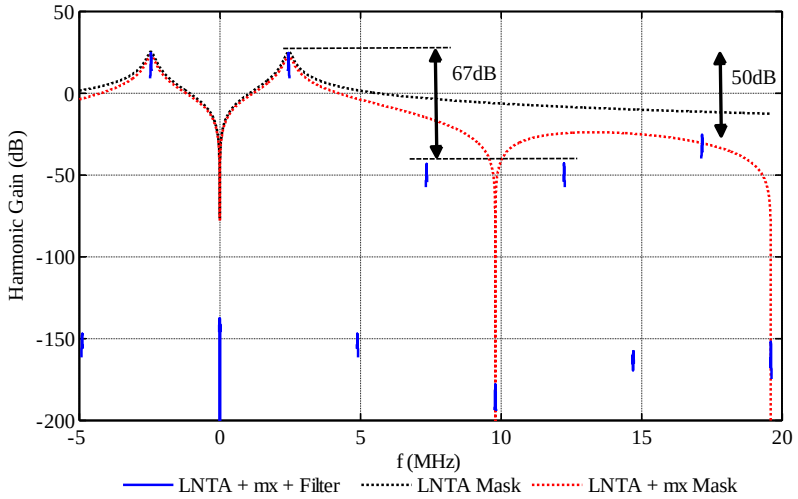


Source: the Author.

Figure 5.20 shows periodic transfer function simulation *in blue*. It indicates that during operation the harmonics will be translated to IF frequency with the gains presented *in blue*. It means that the signals at f_{LO} will be translated with 24 dB of gain, but signals at $3f_{LO}$ and $5f_{LO}$ will be translated with 67 dB below the carrier, and $7f_{LO}$ will be translated with 50 dB of attenuation comparing to the carrier. The $7f_{LO}$ harmonic is not in the scope since it is not considered in the OOB mask proposed in standard specifications (Ta-

ble 3.1). The even harmonics are strongly attenuated as expected in square wave mixers. Black and red dotted curves show Matlab calculations using the LNA and WIS models.

Figure 5.20: Full-rate Operation Section translation gain.



Source: the Author.

5.1.5 Gm Cell

The first block of the IF section (Figure 4.1) is a gain transconductance stage that converts the signal to the current domain preparing for the next filtering stage. Figure 5.21 presents the schematics of the pseudo-differential transconductor amplifier. The transconductor is composed by 4 inverter-like differential stages of the same size connected in parallel. Gain control is realized through 3 bit selection with 4 possible gains of 1.7 dB, 7.1 dB, 10.5 dB and, 12.5 dB at 5 MHz when loaded by a $3.27\,\mathrm{k}\Omega$ input impedance filter, such as the single input impedance predicted for the 4/8 filter and presented in the next section (Table 5.1).

Table 5.1: Gm cell gain and noise figure programming at 5 MHz .

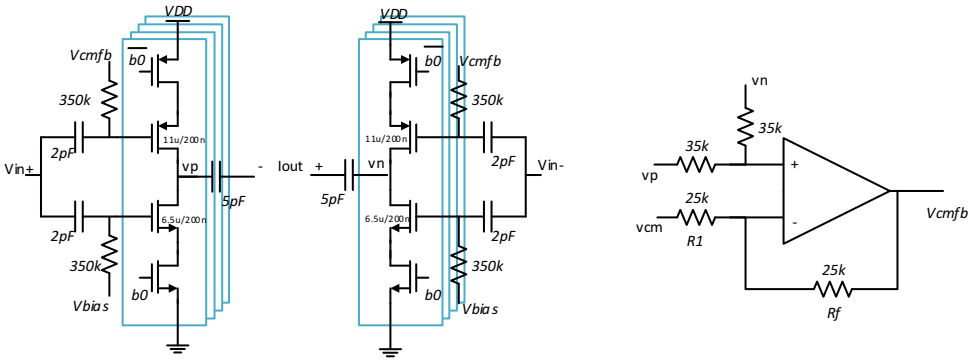
Gm control ($b_2b_1b_0$)	000	001	010	011	100	101	110	111
Gain (dB)	1.7	7.1	7.1	10.5	7.1	10.5	10.5	12.5
Noise figure (dB)	20	17.7	17.7	17.5	17.7	17.5	17.5	15.7

Source: the Author.

Each inverter of the gm cell is biased in moderate inversion ($gm/I_d = 18\,\mathrm{V}^{-1}$) with a current of $12\,\mathrm{uA}$. In order to increase output impedance, gm stage devices are sized with $L = 200\,\mathrm{nm}$.

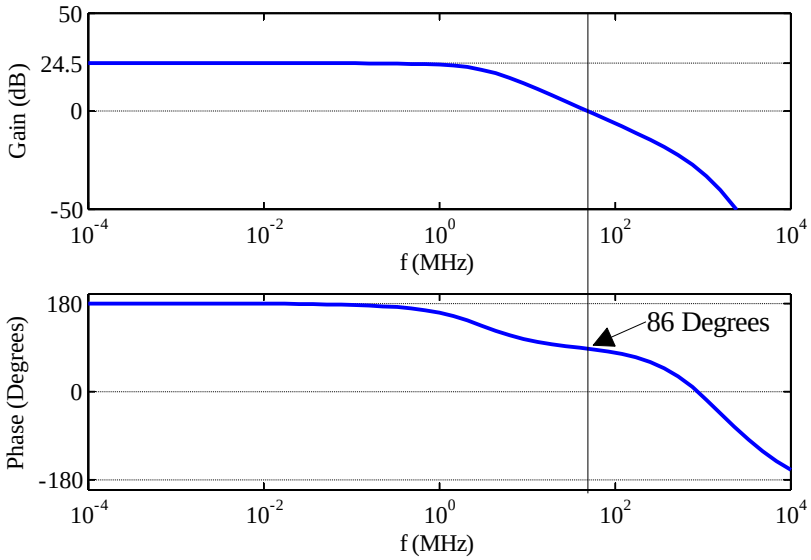
Output common mode is established through the common-mode feedback (CMFB) circuit presented in Figure 5.21. The amplifier is a single-stage differential pair with current-mirror load. The amplifier operates in closed-loop in order to reduce gain with a phase margin of 86^o for the CMFB loop as shown in the schematic stability analysis in Figure 5.22 .

Figure 5.21: Gm cell schematics.



Source: the Author.

Figure 5.22: Gm cell stability analysis.



Source: the Author.

Figure 5.23 and 5.24 show the effective programmable gain obtained by the gm cell with a load of $3.27k\Omega$ and its consequent noise figure.

Figure 5.24 presents the input (Z_{11}) and output impedance (Z_{22}) obtained by the gm cell showing that in higher gain the impedance at 5 MHz is around than $15\,\mathrm{k}\Omega$ (larger than $3.27\,\mathrm{k}\Omega$) which is adequate for the transconductor implementation. Excellent linearity of the gm cell is evidenced by the IIP3 simulation at 10.5 dB gain presented in Figure 5.25.

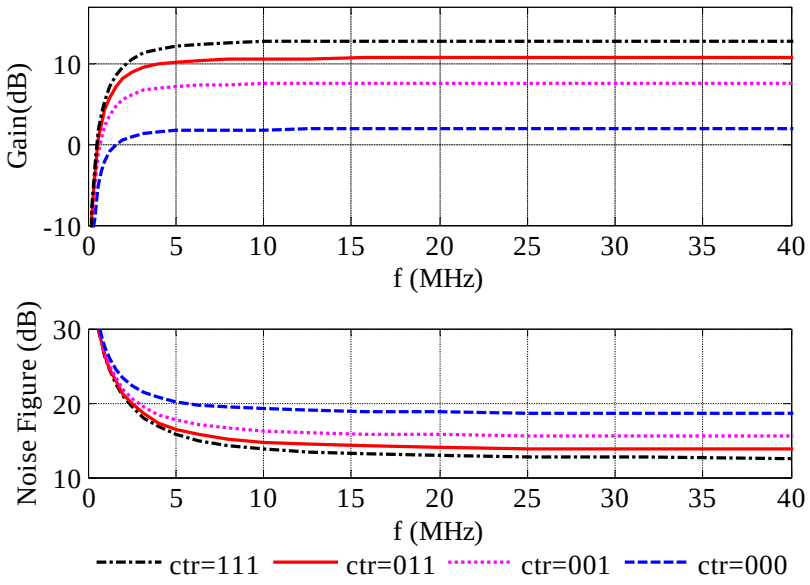
5.1.6 4/8 IQ Filter Design

Second and third filter stages presented in Figure 4.1 are also complex band-pass filters based on the presented charge-sharing principle but with a slightly different architecture.

The 4/8 CS filter (Figure 5.26) has a structure similar to the the 4/4 CS filter presented in Section 5.1.3. The filter is composed by 4 history capacitors (C_H) that share their charges with 8 rotating capacitors (C_R) in 8 different phases. Unlike the 4/4 filter, output and input are separated in the 4/8 filter.

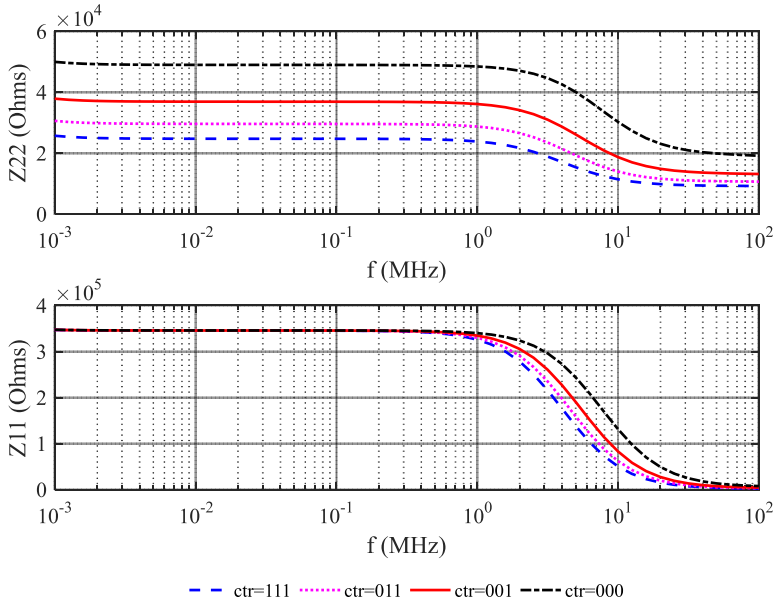
The 4/8 filter transfer function is presented in Eq. 4.10 and 4.11, and compared with

Figure 5.23: Gm cell gain and noise figure.



Source: the Author.

Figure 5.24: Gm cell Z_{11} and Z_{22}.

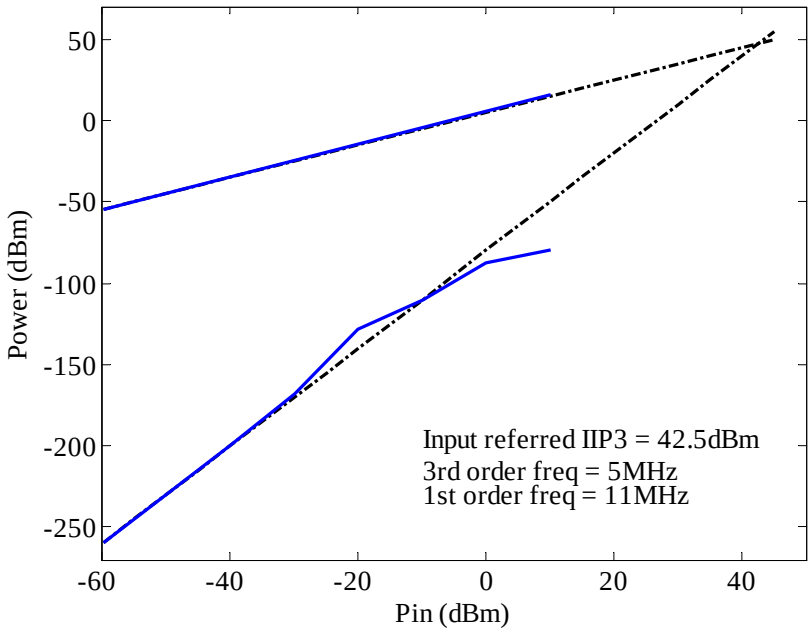


Source: the Author.

the 4/4 filter transfer function in Figure 5.27 for a center frequency of 5 MHz. In the figure, the better selectivity presented by the 4/8 filter is clearly shown with an image rejection improvement of about 5 dB.

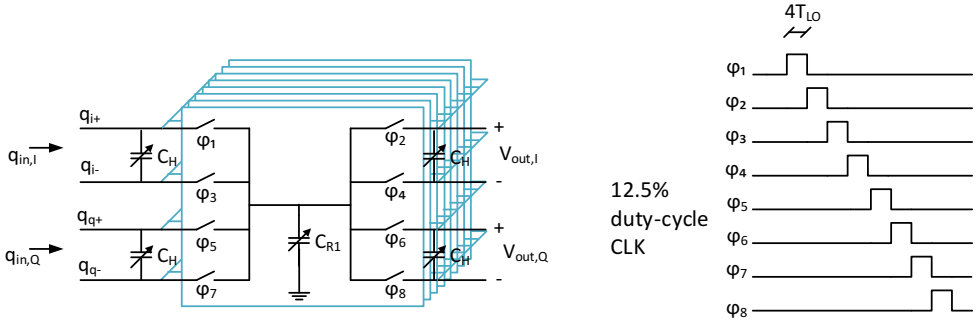
$$H(z) = \frac{V(z)}{Q(z)} = \frac{k}{(1-\alpha z^{-1})^2 - j[(1-\alpha)z^{-1}]^2} \tag{4.10}$$

Figure 5.25: Gm cell IIP3.



Source: the Author.

Figure 5.26: 4/8 filter architecture.



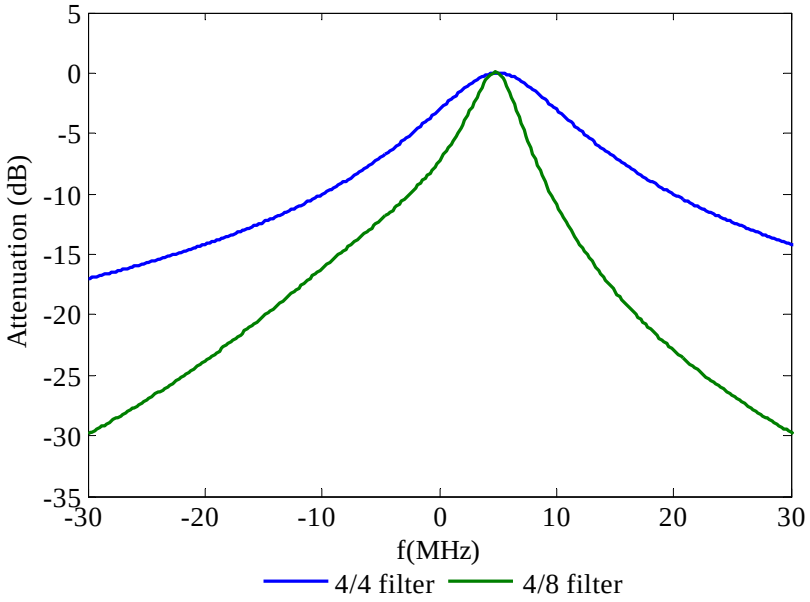
Source: the Author.

$$k = \frac{1}{C_H + C_R}, \ \alpha = \frac{C_H}{C_H + C_R} \tag{4.11}$$

Similar to the 4/4 filter, the input impedance of the 4/8 filter is given by equation 5.15. Since the sampling rate f_s is 16 times smaller in this filter stage a good trade off should be established in the definition of C_R to avoid an excessive increase in Z_0. Previous Gm output impedance should be at least 3xZ_0 to avoid reduction in the quality factor of the 4/8 filter. On the other hand, it is recommended to minimize C_R and consequently C_H size for area constraints as well as to reduce routing parasitics.

$$Z_0 = {}^{1}/_{C_R f_s} \tag{5.15}$$

Figure 5.27: Comparison between 4/4 and 4/8 filter transfer functions. *(Matlab)*

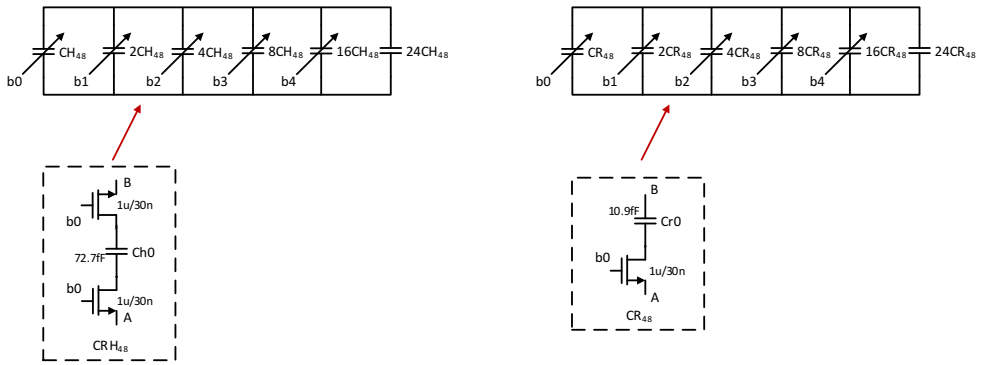


Source: the Author.

Center frequency of the 4/8 filter is given by equation 5.16 (MADADI et al., 2016), α defined in Eq. 4.11. Designed C_R and C_H are 500 fF and 6.65 pF respectively, resulting in an equivalent $Z_0 = 3.27\,\text{k}\Omega$. C_H is implemented differentially in order to reduce capacitor size. Both capacitors are programmable using 5 bits as presented in Figure 5.28 offering flexibility in the selection of the IF frequency from 2 to 11 MHz and input impedance from 2.7 to 6 kΩ.

$$f_c = \frac{f_s}{2\pi} \arctan\left[\frac{(1-\alpha)\sin(\pi/4)}{\alpha + (1-\alpha)\cos(\pi/4)}\right] \tag{5.16}$$

Figure 5.28: $C_H$and C_R capacitor banks.

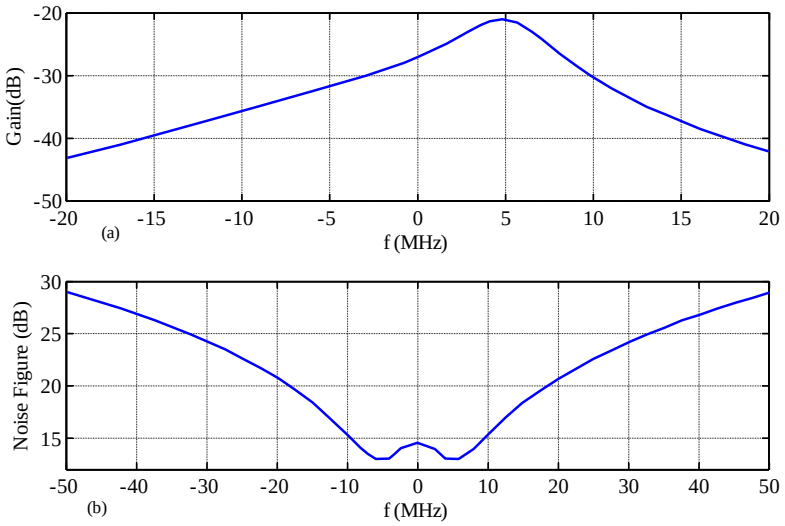


Source: the Author.

Switches of 800 nm x 30 nm presented in Figure 5.26 are designed in a similar way to the 4/4 filter switches presented in Section 5.1.3.

Figure 5.29 present schematics simulation of gain and noise for the proposed 4/8 filter.

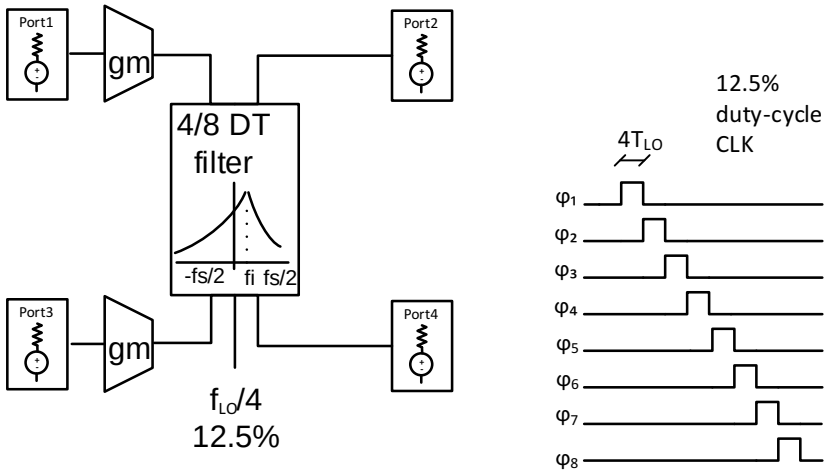
Figure 5.29: Filter 4/8: (a) gain; (b) noise figure.



Source: the Author.

A testbench combining both gm and filter 4/8 was implemented in order to verify the correct integration of blocks (Figure 5.30). Ports 1 and 3 are both $50\,\Omega$ differential since this requirements are necessary for the noise measurements in Cadence. Ports 2 and 4 are high impedance ($100\,\text{k}\Omega$) to simulate next gm + filter chain. The AC coupling capacitors in gm cell were selected as $5\,\text{pF}$ after simulation of both blocks and measurement of gain, image attenuation and attenuation at $8\,\text{MHz}$, shown in Figure 5.31.

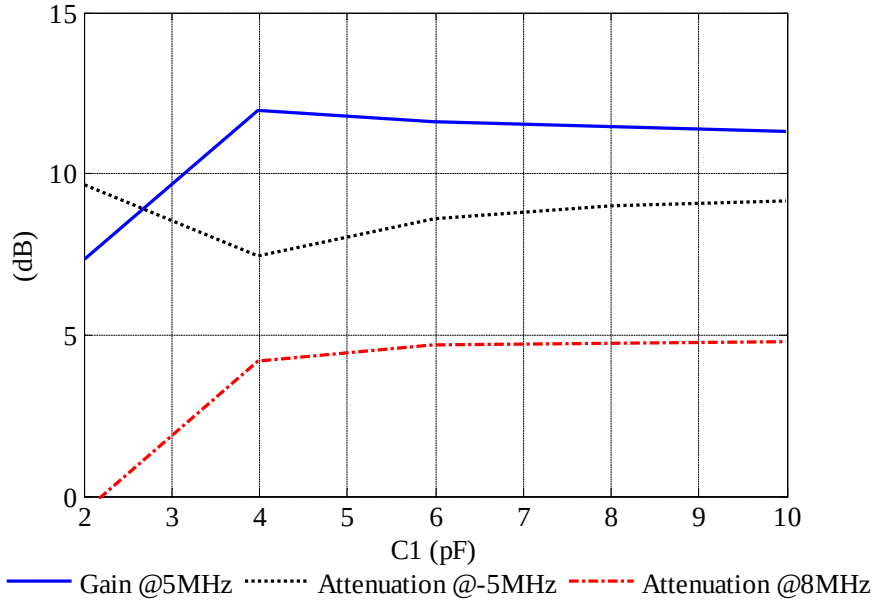
Figure 5.30: Combined Gm and filter 4/8 simplified testbench.



Source: the Author.

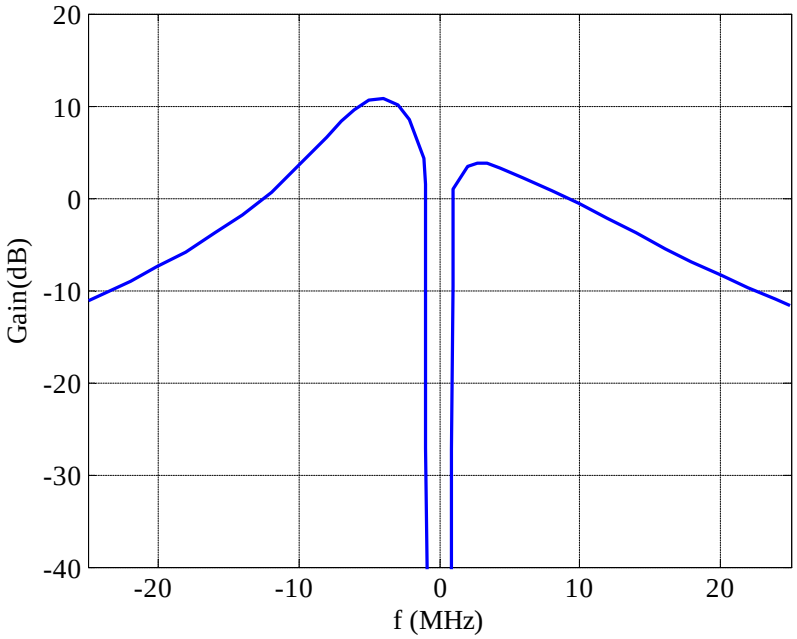
Figure 5.32 and 5.33 present gain and noise curves respectively. The effect caused by AC coupling capacitors can be observed in both curves since they strongly attenuate DC gain and increase noise figure at DC. There is also a reduction in the quality factor of the filter gain when compared with the ideal voltage sources used in Figure 5.29. This effect is mainly occasioned by the reduced output impedance of the gm cells and can be better observed in Figure 5.34 when both simulations are superposed.

Figure 5.31: Gm decoupling capacitor impact.



Source: the Author.

Figure 5.32: Combined Gm and filter 4/8 Gain.

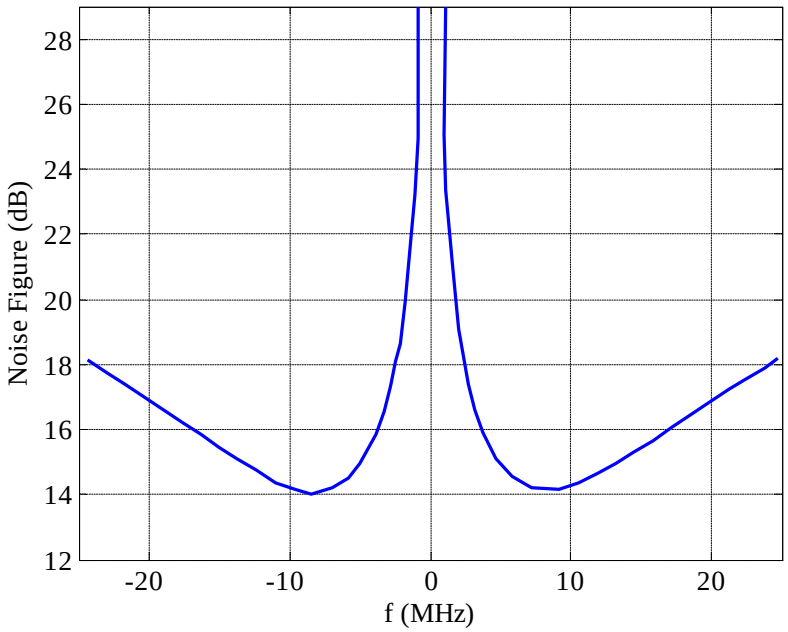


Source: the Author.

5.1.7 Clock Generation

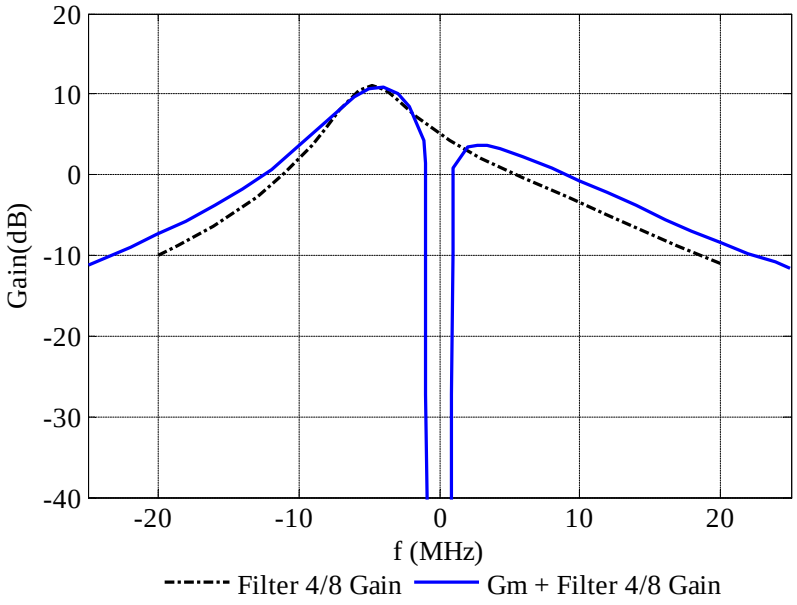
The 25 % and 12.5 % duty-cycle clock phases needed for the DT RX operation are generated in several steps. Clock processing is performed with an input clock of 4.9 GHz and consequently, customized cells were developed due to the high speed requirement.

Figure 5.33: Combined Gm and filter 4/8 Noise Figure.



Source: the Author.

Figure 5.34: Reduction in filter 4/8 quality factor due to Gm output impedance reduction.



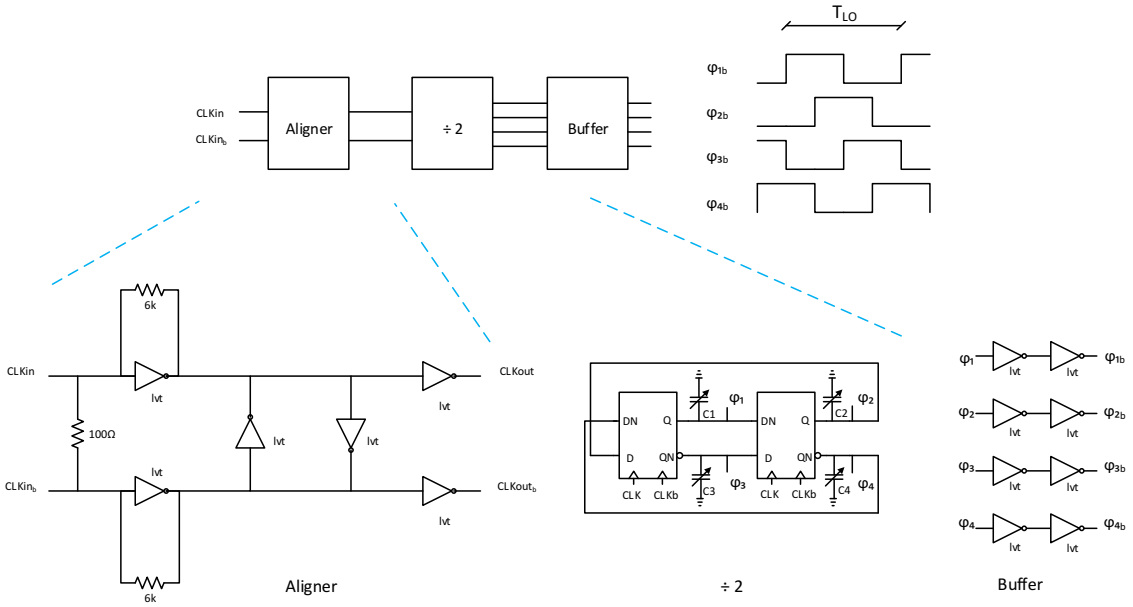
Source: the Author.

These high speed cells use traditional CMOS topologies but with *low Vt* devices available in the technology as proposed by MADADI; TOHIDIAN; STASZEWSKI (2015).

Initially, 50 % differential clocks separated by 90^o are generated in a similar way I and Q clock signals are typically generated in direct conversion receivers, that means by clock division by 2 from a differential clock external to the receiver (Figure 5.35).

Clock aligner presented in Figure 5.35 is only necessary to enable the receiver to be tested alone in the IC. Normally, input clocks would be also generated *in chip* and this block would not be necessary. For this reason, this block is also not accounted for in the receiver power budget. Aligner compensates mismatches in the input signals (coming from *off-chip*) and establishes differential clocks for the processing. A $100\,\Omega$ resistor matches the external differential transmission line network.

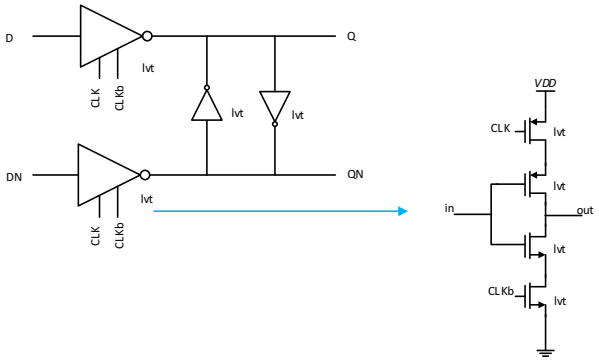
Figure 5.35: High speed 50 % clock generation.



Source: the Author.

Divide-by-2 is composed by D latches in a loop to generate 50 % duty-cycle clocks (φ_1 - φ_4) that are buffered by two-stage customized inverters also presented in Figure 5.35. Capacitors C1 to C4 are introduced to calibrate duty-cycle of the divider. D latch is presented in detail in Figure 5.36. In the D-latch, clocked inverters are followed by back to back inverters that align the complementary edges of the generated square-wave clocks.

Figure 5.36: Customized D latch schematics.

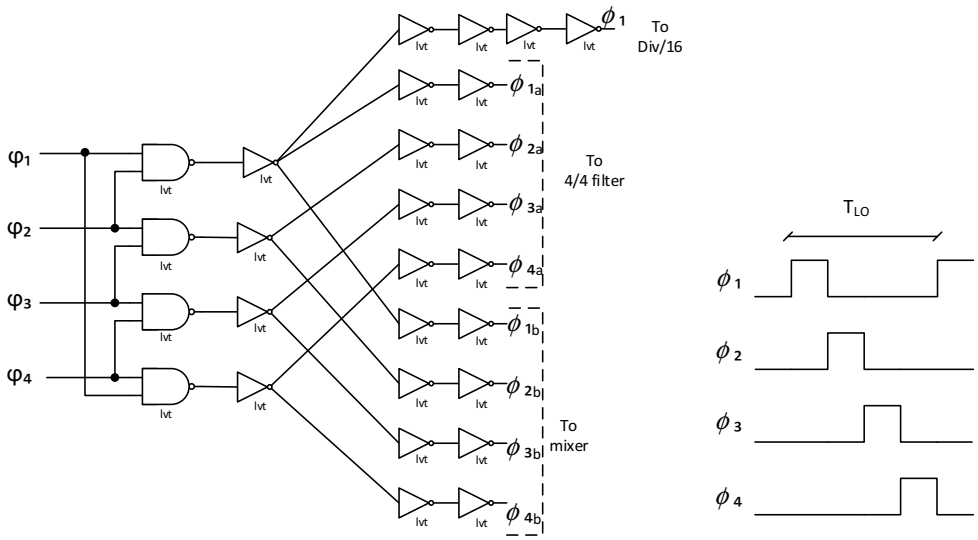


Source: the Author.

The 25 % duty-cycle phases are generated by AND logic as shown in Figure 5.37. Cells are also developed using low Vt customized cells. Phases are separately buffered for mixer and 4/4 filter application. An additional output is buffered to be used in the

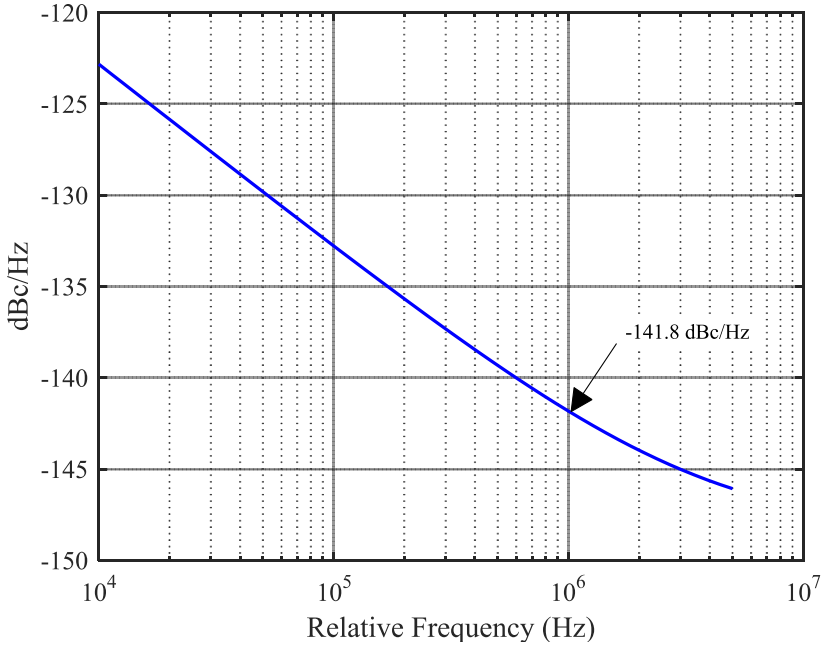
generation of the 12.5 % duty-cycle clocks needed by the 4/8 filters. Phase noise was evaluated in simulation after the 25 % duty-cycle generation to ensure that generation was not affecting input clock quality (Figure 5.38).

Figure 5.37: 25 % duty-cycle generation logic.



Source: the Author.

Figure 5.38: Phase noise after 25 % duty-cycle clock generation.



Source: the Author.

Nominal phase noise of -141.8 dBc/Hz at 1 MHz (Figure 5.38) surpass by far the requirements presented in Table 3.2. Since phase noise after the divider is critical and cannot be correct using programmable capacitors such as the other presented blocks, cor-

ner simulations are presented in Figure 5.39 using PVT corners list presented in Table 5.2. The worst case phase noise of -135 dBc/Hz was found at 27^{o}C, SS and 0.95 V.

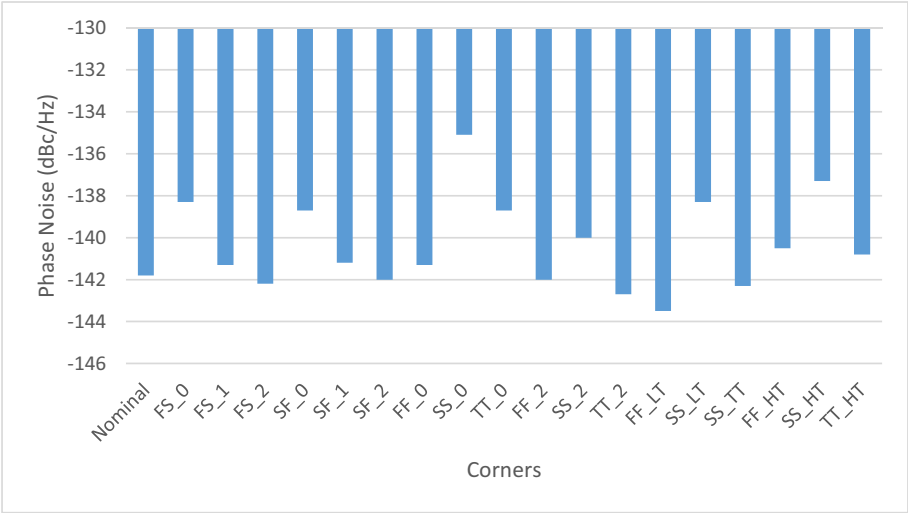
Table 5.2: PVT corners list.

	Nominal	FS_0	FS_1	FS_2	SF_0	SF_1	SF_2	FF_0	SS_0	TT_0
temperature	27	27	27	27	27	27	27	27	27	27
Process	TT	FS	FS	FS	SF	SF	SF	FF	SS	TT
vdd	1.05	0.95	1.05	1.15	0.95	1.05	1.15	0.95	0.95	0.95

	FF_2	SS_2	TT_2	FF_LT	SS_LT	SS_TT	FF_HT	SS_HT	TT_HT
temperature	27	27	27	-40	-40	-40	125	125	125
Process	FF	SS	TT	FF	SS	TT	FF	SS	TT
vdd	1.15	1.15	1.15	1.05	1.05	1.05	1.05	1.05	1.05

Source: the Author.

Figure 5.39: Phase noise corners.



Source: the Author.

The 12.5 % duty-cycle signals are generated using the circuit presented in Figure 5.40. The 25 % buffered signal f_{LO} frequency is initially divided by 4 and subsequently delivered to the 12.5 % waveform generator proposed in (TOHIDIAN; MADADI; STASZEWSKI, 2014). DFFs are initialized with '10000000' using the reset control. This block was developed using only standard cells available in the library. Output phases are individually buffered to be delivered to the 4/8 filters.

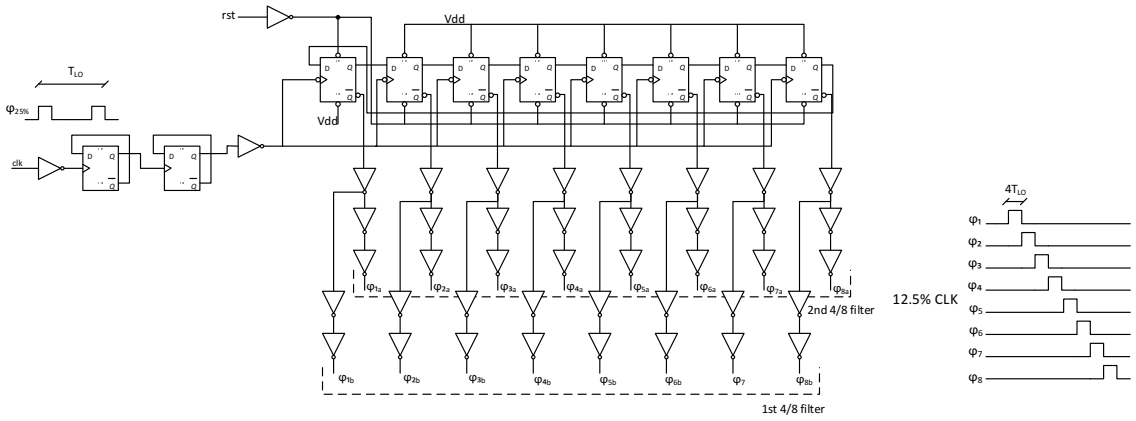
Typical breakdown current consumption and current consumption corners are presented in Figure 5.41, showing a total of 994 uA discounting the aligner in a transceiver implementation. Worst case occurs at 27^{o}C, FF high voltage(1.15 V).

5.1.8 Top Level Simulation Results

Top-level simulation results are presented in this section.

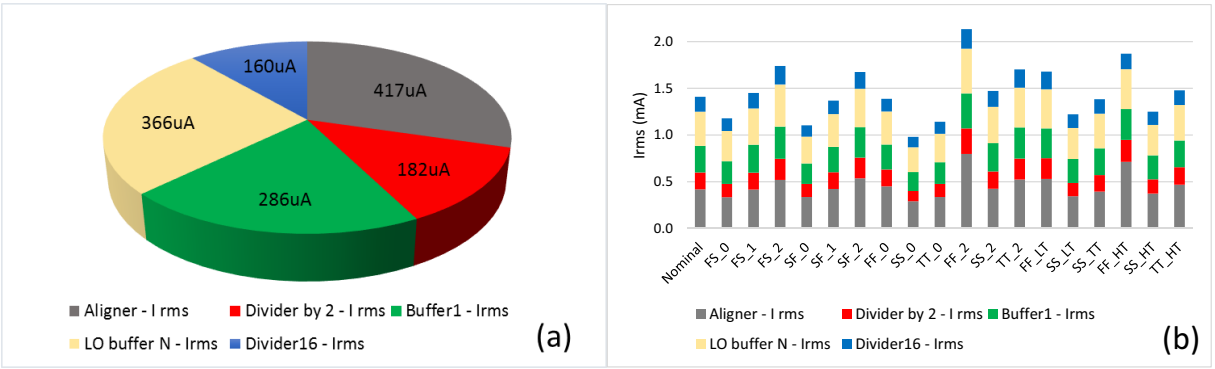
Figure 5.42 shows gain simulation using PSS/PAC analysis of the complete receiver in schematics before last gain stage. Simulation shows the effect of the cascaded filters increase in the selectivity and a resulting gain of 46 dB before the last gain stage. The null

Figure 5.40: Generation of 12.5 % duty-cycle signals.



Source: the Author.

Figure 5.41: Divider current consumption breakdown.



Source: the Author.

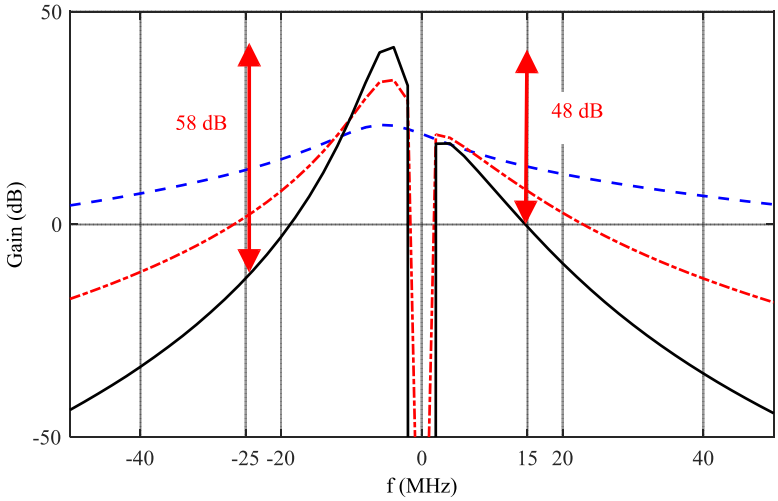
generated by the decoupling capacitors in the gm stages is not clearly defined due to the reduced number of points used in the simulation. The increased selectivity from the first filter (in blue) to the full receiver (in black) is clearly visible in the figure.

Considering a potential 9-bit SAR Dual ADC of 20 MHz sampling-rate application, with a subsequent digital complex demodulation, the receiver at 5 MHz IF would provide 58 dB and 48 dB of protection against aliasing with frequencies -25 MHz and -15 MHz, respectively. According the to the standard, the aliasing protection required at f ¿ =3 MHz is 27 dB + 21 dB, consequently leaving no margin. This could be improved with three different approaches: including an anti-aliasing filter, a current input ADC after Gm with an additional WIS filter, or just by reducing IF to 3 MHz with a consequent increase in the selectivity of the filter.

Figure 5.43 shows the noise figure of the complete receiver simulated using PSS/PNOISE analysis. The value of 5.6 dB predicted by Table 4.2 can be observed in the IF frequency of -5 MHz.

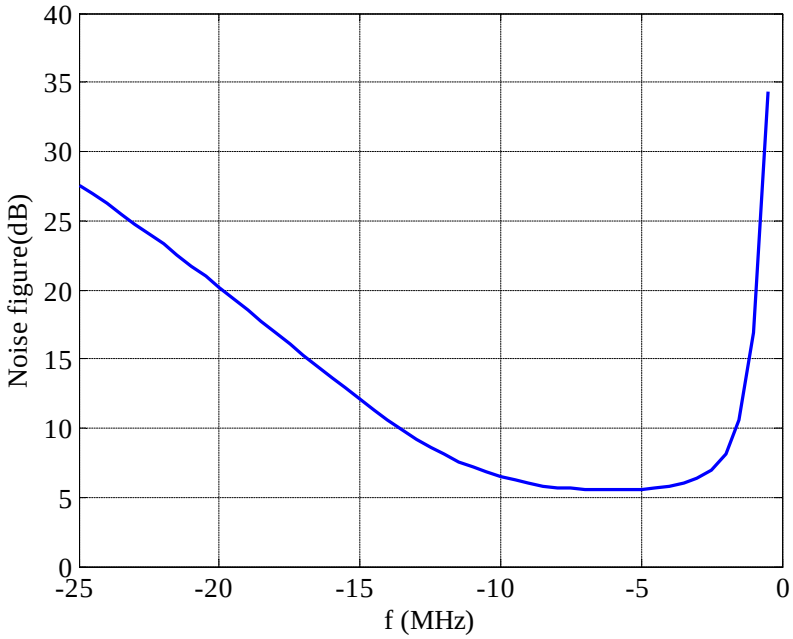
Transient simulation is presented in Figure 5.44. It shows the differential voltage at the output of the filters for a sinusoidal input of -70 dBm with 46 dB of gain. An additional gain of 20 dB is provided by the last stage before ADC, which is not shown in the simulation. Second and third filters are placed after two gm cells that take around 6 μs to operate due to their CMFB circuits.

Figure 5.42: Top-level gain.



Source: the Author.

Figure 5.43: Top-level noise figure.

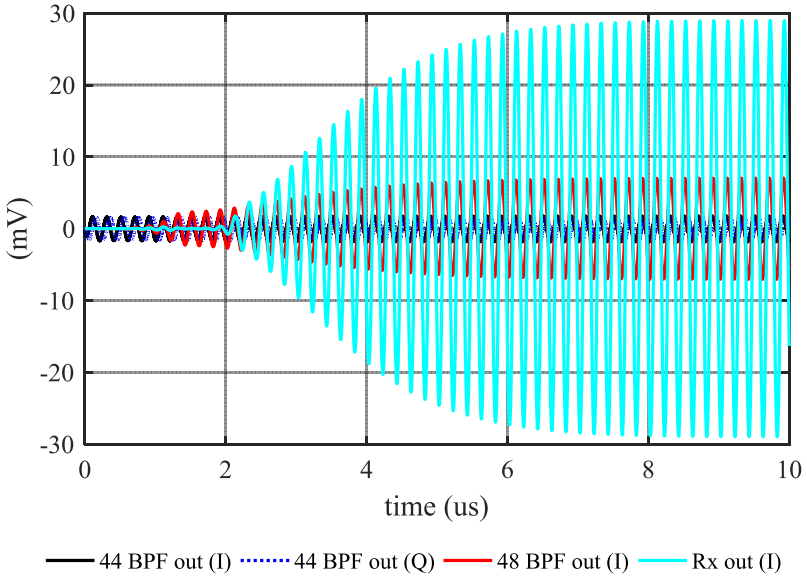


Source: the Author.

5.2 Physical Implementation and Measurements Results

The receiver was implemented in cooperation with Taiwan Semiconductor Manufacturing Company Limited (TSMC), Technical University of Delft (TU-Delft), and University College Dublin (UCD), using TSMC 28nm low power bulk process. As part of the cooperation with TSMC, the physical implementation (layout) of the proposed receiver, as well as the fabrication of the integrated circuit, printed circuit board (PCB) design, and

Figure 5.44: Top-level transient simulation.



Source: the Author.

measurements were performed by TSMC under supervision and guidance of the thesis author. The measurements were performed for one sample using chip-on-board (COB) technology.

Chip Micrograph of the circuit implementation is presented in Figure 5.45 and shows receiver implemented area of 0.65 mm^2 (KUO et al., 2016). Details and guidelines adopted in block-level and top-level layout are included in the appendix.

A gain of 46 dB at the -5 MHz IF with an image attenuation of 26 dB at 5 MHz was obtained in the receiver (Figure 5.46.a), allowing for the 31 dB image rejection required by standard to be easily achieved after complex demodulation in baseband. Simulation results are also included and show a good agreement with the measurements.

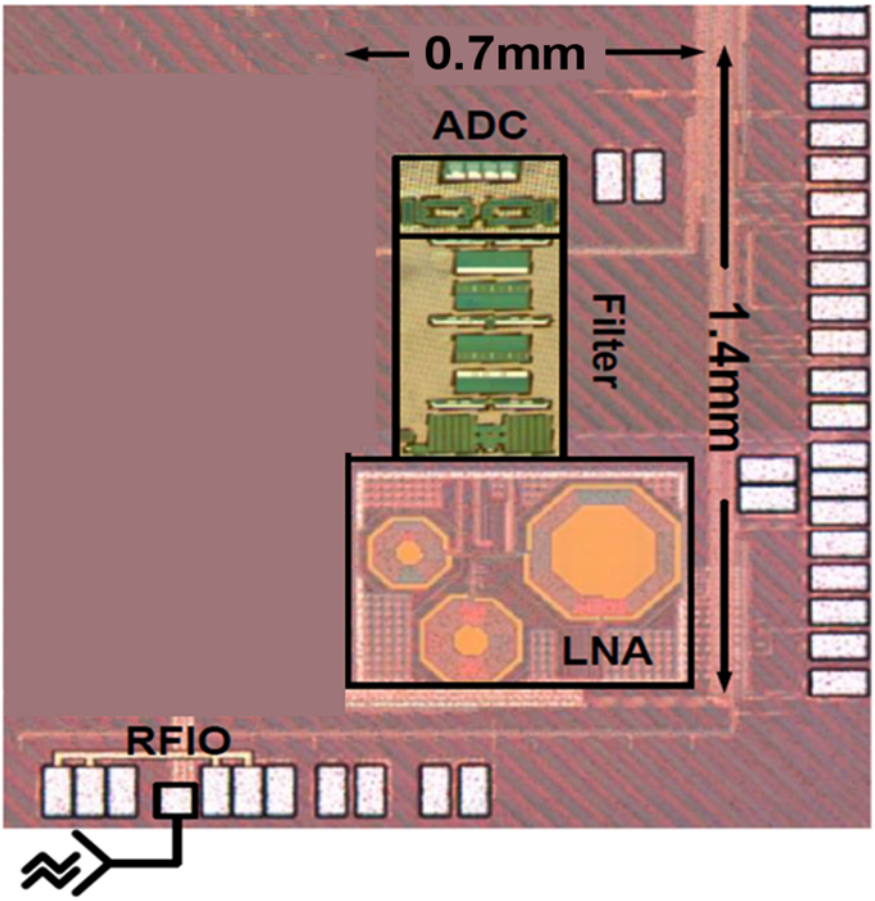
BLE OOB blocking test was performed using Rohde Schwarz R&S®CBTgo test equipment (measurement RCV-LE/CA/04/C). In the test, a BLE signal received at -67 dBm is added to a continuous-wave (CW) signal interferer with power defined by Table 3.1. In Figure 5.46, it is possible to observe that BLE Blocker level surpass standard requirements identified in the BLE mask showing the correct working of the full-rate operation section.

Sensitivity of the receiver was measured using a Vector Signal Generator SMIQ (Rohde Schwarz) and the application software for Bluetooth signals SMIC-K5. The packet error rate (PER) of 30.8% is equivalent to the 0.1% BER (PRUMMEL et al., 2015) and defines the receiver sensitivity. In the test, a BLE signal has its power reduced and PER measured to identify the 30.8% limit. Figure 5.47 shows the PER measurement curve and defines the sensitivity of -95 dBm (KUO et al., 2016).

Functionality of the receiver was verified on several channels covering the complete BLE band. Figure 5.48 shows the receiver worst case figures are 46 dB of gain, 26 dB of image attenuation, 6.5 dB of noise figure, and -19 dBm of IIP3 from the first to the last BLE channel.

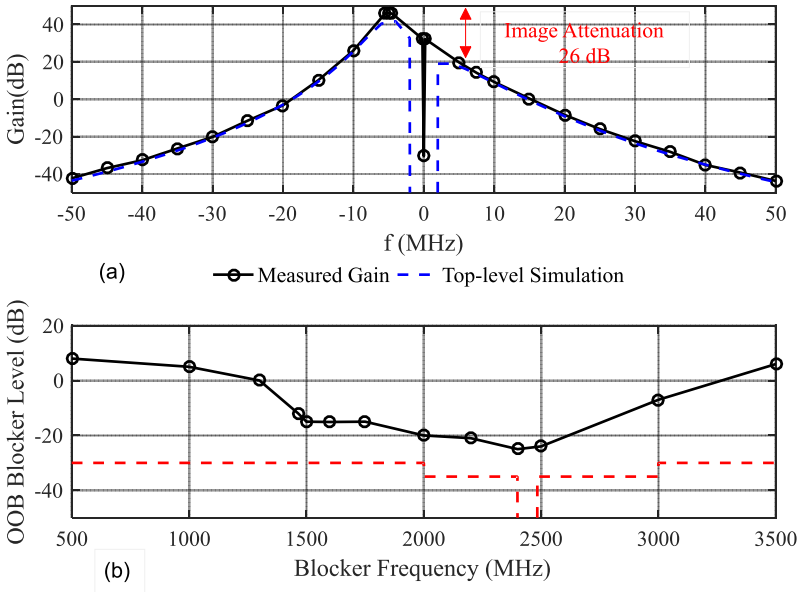
Figure 5.49 presents the measurement of the receiver input matching to the $50\,\Omega$ an-

Figure 5.45: Chip micrograph.



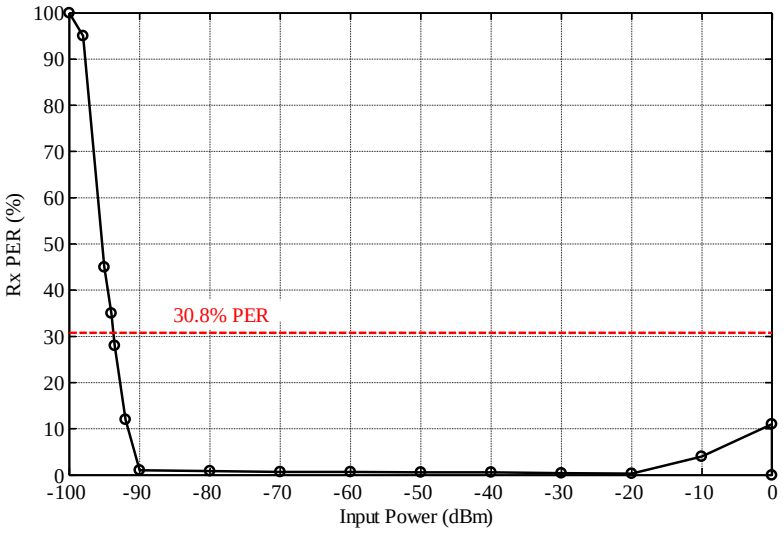
Source: Adapted from KUO et al. (2016).

Figure 5.46: (a) Measured receiver transfer function. (b) Measured OOB blocking test.



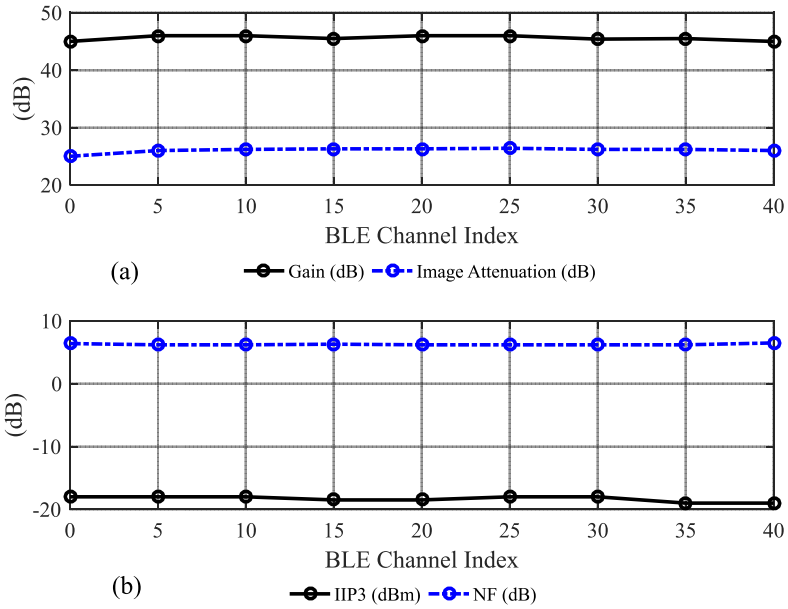
Source: Adapted from KUO et al. (2016).

Figure 5.47: Receiver sensitivity measurement.



Source: Adapted from KUO et al. (2016).

Figure 5.48: (a) Measured channel gain and image attenuation. (b) Measured channel IIP3 and noise figure.

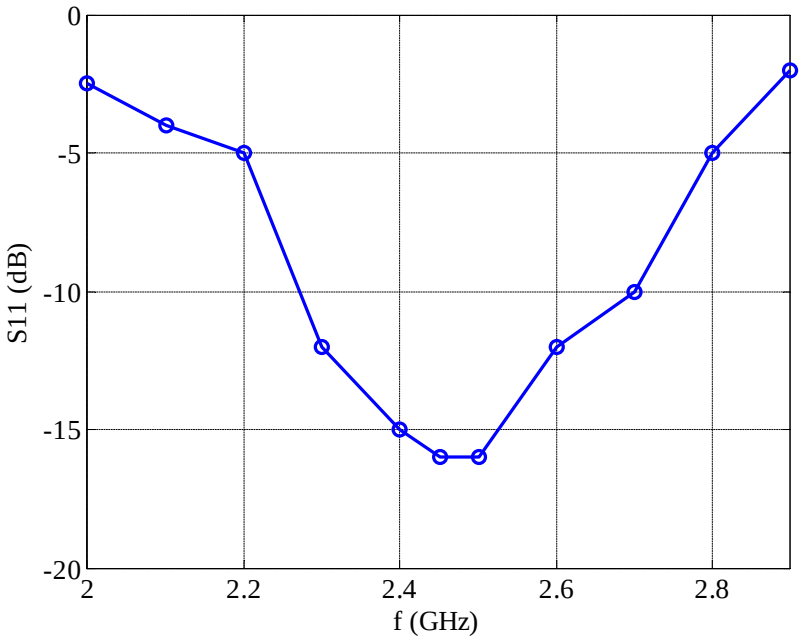


Source: the Author.

tenna showing S_{11}, and consequent return loss, is smaller than -15 dB in the complete band.

Figure 5.50 presents the power consumption breakdown of the receiver. This power breakdown includes all the blocks at the Figure 4.1 except for the clock aligner that was designed and used only for direct receiver measurements (Section 5.1.7). The 9-bit SAR ADC was designed by Guanzhong Huang from University College Dublin (UCD) and the Digital Controlled Oscillator (DCO) that is also accounted for in the breakdown was designed by TSMC(KUO et al., 2016). The complete receiver consumes 2.75 mW at

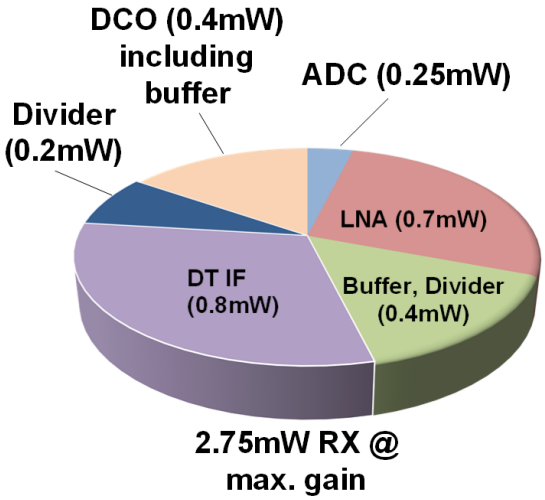
Figure 5.49: S_{11}- input matching measurement.



Source: Adapted from KUO et al. (2016).

maximum gain and is the first discrete-time receiver for BLE with state-of-the-art performance.

Figure 5.50: Typical measured power consumption breakdown of the implemented receiver



Source: (KUO et al., 2016).

5.3 Summary

This chapter presented in detail the block-level design of the first DT receiver for BLE. The implemented circuit in TSMC 28 nm bulk CMOS uses

an area of 0.65 mm^2 and consumes 2.75 mW while achieving state-of-the-art performance, as can be observed in Table 5.3.

Table 5.3: Performance summary and comparison with state-of-the-art Bluetooth Low Energy receivers.

Standard	BLE	Zigbee+BLE +MBAN	BLE	BLE +MBAN	BLE	BLE
Technology	28n	90n	55n	0.12u	0.13u	0.13u (1.0V)
Data rate (MBPS)	1	0.25/1/0.97	1	1	1	1
Noise Figure (dB)	6.5	6	$\sim 6*$	6	15.1	16.5
IIP3 (dBm)	-19	-19	-	-	-15.8	-2.9
Image Reject (dB)	26	35	-	-	30.5	-
Sensitivity (dBm)	-95	-100/-98/-96	-94.5	-96.5	-84.9	-81.4
Consumption (mW)	2.75	3.8	11.2**	6.5	0.6	1.1
Architecture	DT High IF	Sliding IF	DC	Sliding IF	Low IF	No LNA
External components	no	yes	no	yes	yes	no
Reference	This Work	(a)	(b)	(c)	(d)	(e)

$*$ Estimated from paper results.

$**$complete receiver front-end, ADCs, synthesizer, baseband and microprocessor.

(a) (LIU et al., 2013) (b)(PRUMMEL et al., 2015) (c) (WONG et al., 2012) (d) (SELVAKUMAR; ZARGHAM; LISCIDINI, 2015) (e) (MASUCH; DELGADO-RESTITUTO, 2013)

Source: the Author.

6 CONCLUSIONS

This work presented the top-down design of a SAW (Surface Acoustic Wave)-less high-IF (Intermediate Frequency) discrete-time receiver for Bluetooth Low Energy (BLE). This design is the first fully discrete-time receiver for BLE and it is a possible solution for the increasing need of low power architectures for the Internet of Things. The use of discrete-time architectures and complex band-pass filters is presented as a new solution that enables low power consumption and high level of integration.

Starting from the design requirements of continuous time state-of-the-art receivers recently published, system-level considerations are presented and block-level solutions are discussed and designed for TSMC 28nm low-power (LP) bulk complementary metal-oxide-semiconductor (CMOS) process.

The use of fully discrete-time architectures in the implementation of low power receivers is a new and promising subject. The receiver presented, developed, fabricated and measured in this thesis not only has unique features, but also achieves very low power consumption, namely just 2.75 mW including the local oscillator clock generation. Being fully discrete-time, the receiver achieves high performance performance comparable to the best continuous-time receivers for Bluetooth Low Energy found in literature with noise figure of 6.5 dB , sensitivity of -95 dBm, and IIP3 of -19 dBm. The architecture is implemented mainly using passive switched capacitor band-pass filters and pseudo-differential inverter-like transconductors which are amenable to CMOS implementation in newer technologies.

The folding caused by the sampling process at the mixer which normally requires antenna filtering, and the discrete-time implementation entail additional considerations presented in detail in Chapter 4, such as anti-aliasing protection before every filter and analog decimation.

6.1 Summary of Contributions

The main contributions of this thesis are summarized as follows:

- The first discrete-time receiver for BLE was implemented in 28nm CMOS process. Measured results show it achieves state-of-the-art performance without external band-select filters for a power consumption of 2.75 mW.

- A top-down approach to the design of discrete-time receivers based on passive band-pass filters, focusing on the definition of discrete-time transfer functions, sampling rates and early decimation to reduce power consumption is presented.

- Out-of-band linearity is treated at system-level allowing for a BLE receiver implementation without external cumbersome front-end filters. Out-of-band linearity results from a combination of filters defined by LNTA selectivity, WIS implementation of the current-mode sampling mixer, and full-rate implementation of the first highly linear band-pass filter. The implementation that needs no external filter network achieves high quality matching with a return loss smaller than -15 dB.

- *In-band* linearity is achieved using passive discrete-time band-pass filters with high selectivity. In order to reduce power consumption, these passive filters operate at a lower sampling rate. Gain is provided by highly linear inverter-like transconductors operating in moderate inversion. Analog clock decimation implements a moving average filter that offers additional anti-aliasing protection.

- Input impedance of filters and output impedances of LNTA and transconductor stage should be carefully designed in order to avoid reduction of the quality factor of the filters.

6.2 Recommendations for Future Work

The use of the proposed architecture in low power receivers is innovative. It has been previously adopted only for Software Defined Radio and high-performance/ high-power applications. Since this work focused on a proof-of-concept, it opens several possibilities for future work as listed below.

- A detail block-level optimization could be evaluated in order to reduce even further the power consumption.

- A systematic selection of sampling rates and decimation could allow for earlier decimation, at the mixer level, in order to reduce power consumption.

- Implementation of a fully discrete-time receiver without LNA.

- Study of wide-band receivers with a similar discrete-time approach, taking advantage of the WIS filter implementation at the mixer level and of the IF programmability of the discrete-time filters.

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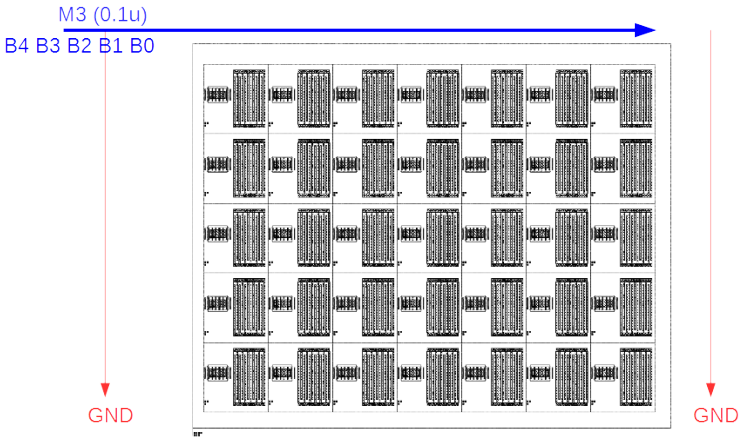
APPENDIX A - LAYOUT CONSIDERATIONS

This appendix presents considerations adopted during layout process.

The design is composed of several binary programmable capacitor banks: at the history and rotating capacitors of the filters, in LNTA adjusting to work over corners, and in the adjustment of the balanced clock input. All the capacitors are metal-oxide-metal (MOM) *lateral capacitors* available in the PDK. Several metal layers are used to increase capacitance density. In the implementation of differential capacitors, the top layers are preferred to reduce parasitic capacitance to the substrate.

Figure A1 presents the rotating capacitor bank of the 4/4 filter. Like the other capacitor banks which are bit-programmed, each capacitor has a switch attached to it. This way layout can be easier, symmetric and hierarchical, and wire capacitance between switch and capacitor can be minimized. In Figure A1, the 5-bit control lines are implemented in metal M3 since they are not sensitive to parasitic resistance or capacitance.

Figure A1: Capacitor Bank CR 4/4 Layout Considerations.

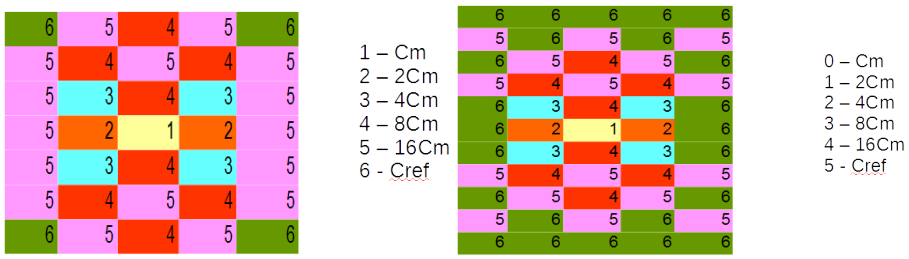


Source: The Author.

Figure A2 presents layout disposition of capacitors Cr and Ch. In order to reduce area there are no capacitor dummies. Also, dummies are less required when using MOM, since capacitance is lateral and internal to the cell. Cref units compose fixed capacitors. The less significant bits are located at the center to minimize variation due to the fabrication process.

Figure A3 presents the layout floorplan of the 4/4 filter. Since it operates in higher frequency, with a clock of 9.8 GHz, the clock lines (Phy1, Phy2, Phy3 Phy4) need to be close to the divider. Additionally, clock lines are routed in higher metal layers with

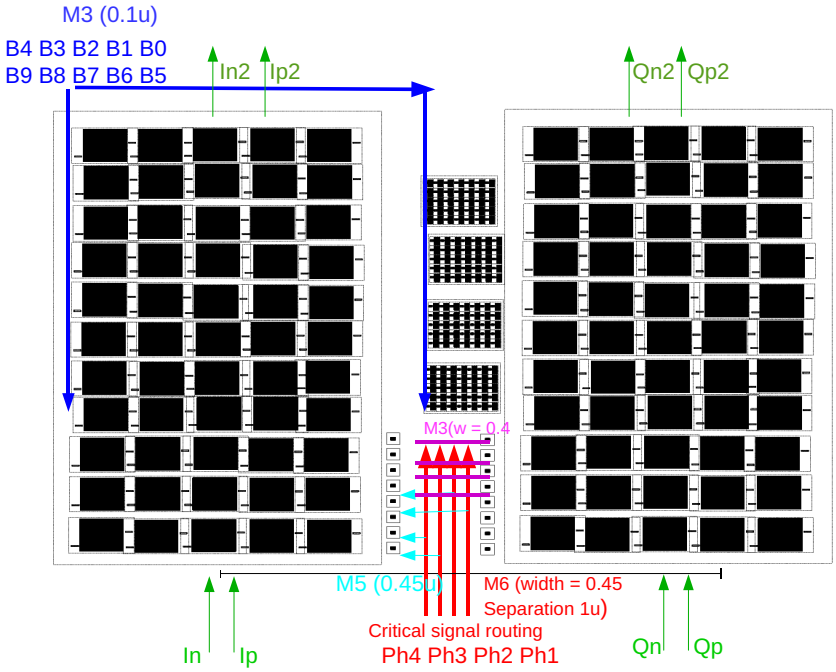
Figure A2: Filter 4/4 Layout Considerations. a) Cr. b) Ch.



Source: The Author.

reduced width since resistance is not a big issue, but capacitance to the substrate needs to be reduced as well as mutual capacitance. Connections between the devices at the center and the smaller Cr capacitor banks needs to be symmetric as much as possible. In, Ip, Qn, and Qp are the direct and quadrature signals received from the mixer at IF frequency. Consequently, these signals are low frequency and not so sensitive to parasitic capacitance.

Figure A3: Filter 4/4 Layout Considerations.

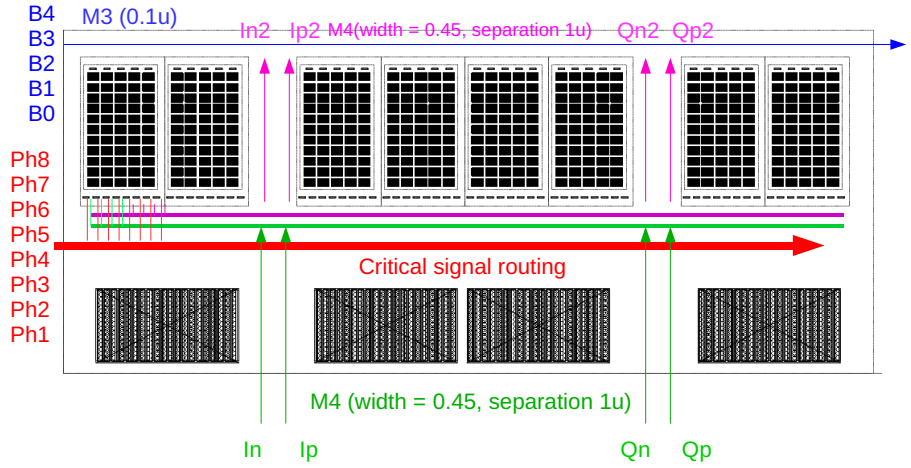


Source: The Author.

Figure A4 presents part of the 4/8 filter floorplan. In the figure, critical routing of clock phases is presented in detail as well as input and output signal connections (In, Ip, Qn, Qp). The 4/8 filter clock phases are less sensitive to routing since the clock rate is around 612 MHz. Nevertheless, the same considerations presented for the 4/4 filter are also applicable. Symmetry of the floorplan can also be observed in Figure A5 as well as the area impact of the differential capacitors Ch. In this technology, layout orientation is very important and designs cannot be rotated, so a detailed floorplan is essential.

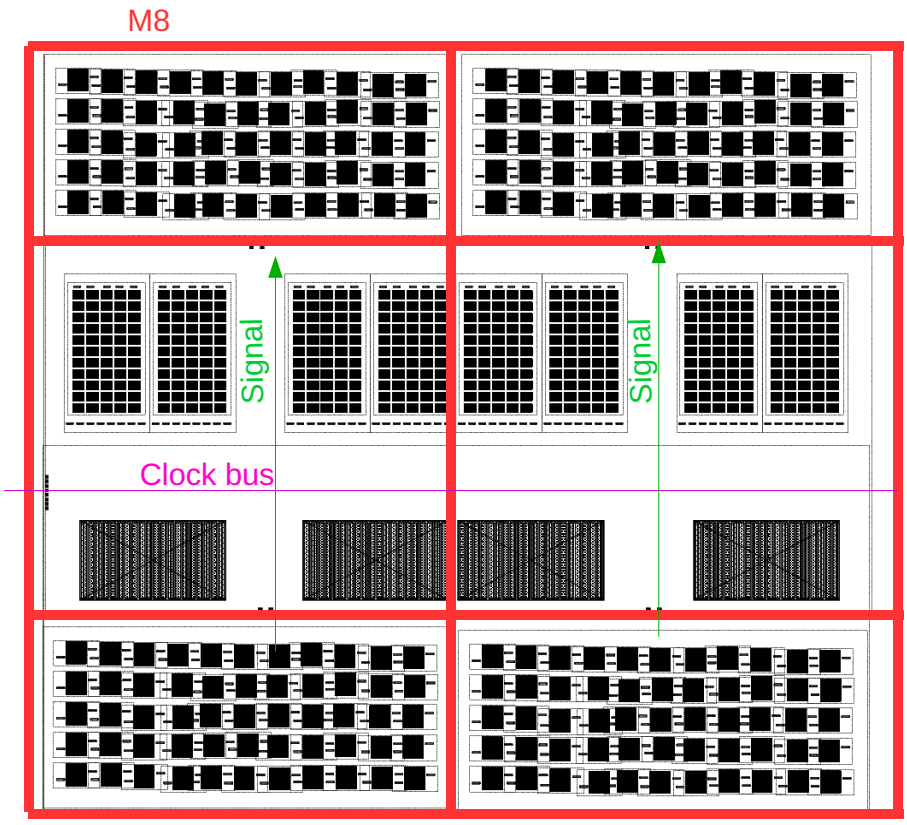
Figure A6 presents layout considerations for the aligner and divider block. Lines connecting the latches in the divider by 2 should have equal lengths and have minimal

Figure A4: Filter 4/8 Layout Considerations.



Source: The Author.

Figure A5: Filter 4/8 Layout Considerations.



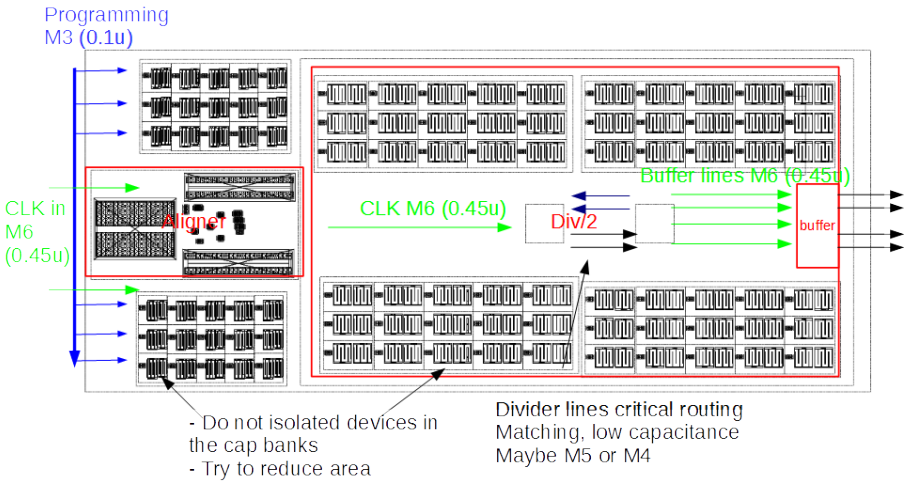
Source: The Author.

parasitic capacitance. High speed clock lines are differential and located in the center of the block. Higher metal layers are used for the high speed clocks.

Figure A7 presents a floorplan showing the position of the high speed clock divider. Separate drivers are used for each clock phase line. Divider is located very close to mixer and filter 4/4 in order to reduce parasitic capacitance of the high speed lines.

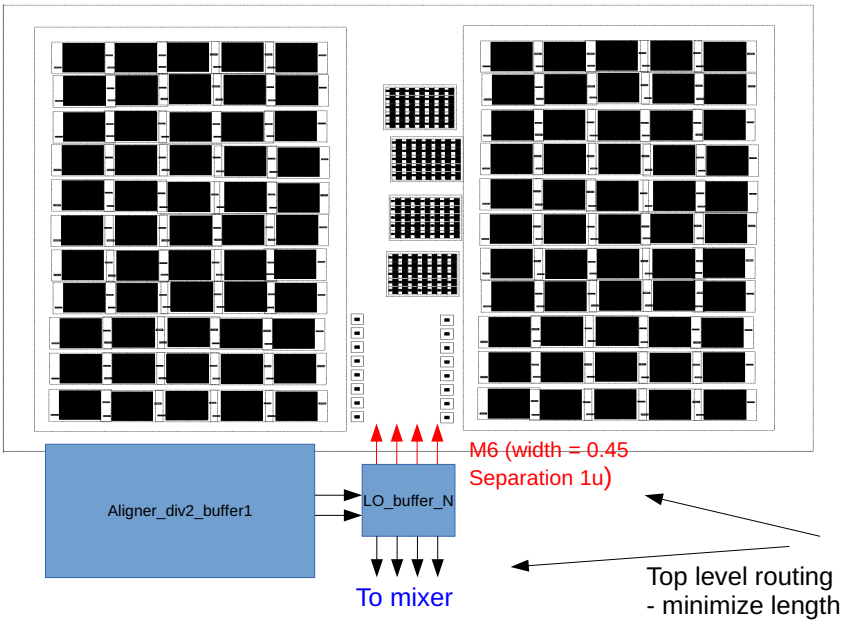
Figure A8 shows the top-level floorplan with the location of divider by 16 - close to the filters 4/8 - and divider by 2 - close to the filter 4/4 and mixer. Every empty space

Figure A6: Aligner Layout Considerations.



Source: The Author.

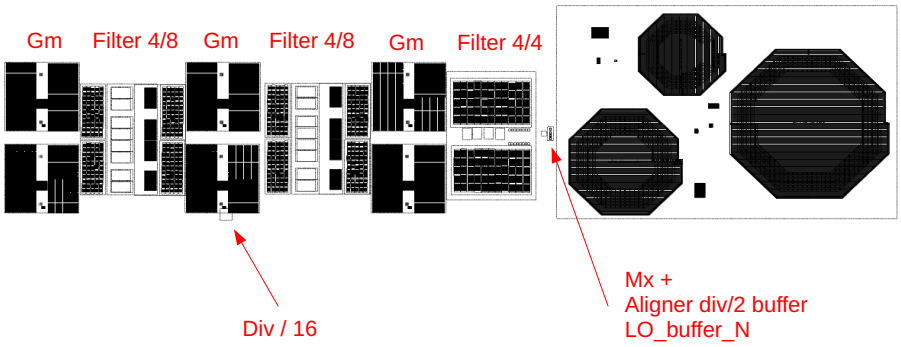
Figure A7: Filter 4/4 and Divider Floorplan.



Source: The Author.

observed around the receiver is used to add capacitors between supply and ground.

Figure A8: Top-level Floorplan Considerations.



Source: The Author.