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Temperature-Compensated Subthreshold CMOS Voltage References for Ultra-Low Power Applications

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“Study hard what interests you the most in the most undisciplined, irreverent and original manner possible.”

— RICHARD FEYNMAN

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ABSTRACT

This work proposes novel temperature-compensated subthreshold voltage references for ultra-low power and ultra-low voltage applications. The core of the proposed circuits is the self-cascode MOSFET (SCM) since it can operate at very low current levels. To reduce the power consumption, self-biasing and zero-V_T leakage biasing schemes are exploited. This resulted in three main structures: a self-biased SCM (SBSCM), a self-biased NMOS load (SBNMOS) and a 3-Transistor (3T) voltage references. For the self-biased structures, the reference voltage generation is achieved by using the SCM with different threshold voltages. Even though these solutions present good performance and low power consumption, the usage of different V_T transistors makes the circuits too sensitive to process variations. To obtain a temperature-compensated voltage reference using the same type of device, we use the reverse short-channel and narrow-width effects of the MOS transistor, where V_T is larger for short/narrow-channel devices. The proposed self-biased circuits were fabricated in 0.18-µm fabrication process while the 3T voltage references were implemented in 0.13-µm process. Measurement results for 24 samples show that the proposed self-biased circuits can operate at 0.45-0.6 V minimum supply voltages, consuming merely 54.8 and 184 pW at room temperature. Without trimming, from 0 to 120 ^{o}C the circuits presented a temperature coefficient of 104 and 495 ppm/^{o}C, while after trimming this values were reduced to 72.4 and 11.6 ppm/^{o}C, respectively. Four versions of the 3T voltage reference were designed. Their post-layout simulation results showed an average voltage reference from sub-kT/q to tens of mV, with a minimum supply voltage of 0.12-0.4 V while operating at power consumption range of fW to pW at 27 ^{o}C. The occupied silicon area of all the proposed circuits is less than 0.002 mm^2. The ultra-low power and ultra-low voltage operation of the proposed circuits make them suitable for extreme power constrained applications.

Keywords: Voltage Reference, Subthreshold, Picowatt, Ultra-Low Voltage, Ultra-Low Power, Integrated Circuit Design, MOSFET.

Referências de Tensão CMOS Compensadas em Temperatura Operando em Subthreshold para Aplicações de Ultra-Baixa Potência

RESUMO

Esse trabalho propõe novas estruturas de referência de tensão compensadas em temperatura e operando em subthreshold para aplicações de ultra-baixa potência e ultra-baixa tensão. O núcleo dos circuitos propostos é o MOSFET self-cascode (SCM) já que o mesmo pode operar a níveis de corrente muito baixos. Para redução do consumo de potência, esquemas de auto-polarização e polarização com o leakage do transistor zero-V_T são explorados. A utilização desses esquemas resultou em três novas estruturas de referência de tensão: SCM auto-polarizado (SBSCM), NMOS como carga ativa auto-polarizado (SBNMOS) e um referência de tensão de 3-Transistores (3T). Para as estruturas auto-polarizadas a geração da referência de tensão é obtida usando o SCM com transistores com threshold (V_T) diferentes. Mesmo essa solução apresentando bom desempenho e baixo consumo de potência, a utilização de transistores com diferentes V_T faz com que os circuitos sejam muito sensíveis a variação de processo. De forma a obter uma referência de tensão compensada em temperatura utilizando o mesmo tipo de dispositivo, nós usamos os efeitos de canal-curto inverso e de canal-estreito do transistor MOS, onde o V_T é maior para dispositivos com canal-curto/estreito, para obter V_Ts distintos. Os circuitos que utilizam o esquema de auto-polarização foram fabricados em tecnologia CMOS padrão de 0.18-µm enquanto as referências 3T foram implementadas em 0.13-µm. Os resultados de medida para 24 amostras mostram que os circuitos auto-polarizados propostos podem operar a tensões de alimentação minimas de 0.45-0.6 V, consumindo apenas 54.8 e 184 pW em temperatura ambiente. Sem calibração, de 0 a 120 °C os circuitos apresentam coeficientes de temperatura de 104 e 495 ppm/°C, enquanto depois da calibração estes são reduzidos para 72.4 e 11.6 ppm/°C, respectivamente. Quatro versões da referência de tensão 3T foram projetadas. Os resultados de simulação pós-layout mostram uma referência de tensão média de sub-kT/q até dezenas de mV, com tensões de alimentação mínimas de 0.12-0.4 V enquanto operam na faixa de consumo de potência de fW-pW. A área de silício ocupada para todos os circuitos propostos é menor que 0.002 mm^2. A operação em ultra-baixa potência e ultra-baixa tensão dos circuitos propostos os faz adequados para aplicações com restrições extremas de consumo de potência.

Palavras-chave: Referência de Tensão, Subthreshold, Picowatt, Ultra-Baixa Tensão, Ultra-Baixa Potência, Projeto de Circuitos Integrados, MOSFET.

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LIST OF ABBREVIATIONS AND ACRONYMS

SCM	Self-Cascode MOSFET
MOSFET	Metal Oxide Field Effect Transistor
MOS	Metal Oxide Semiconductor
SBSCM	Self-Biased Self-Cascode MOSFET
SBNMOS	Self-Biased NMOS Load
3T	3-Transistor
TC	Temperature Coefficient
pW	picowatt
fW	fentowatt
IoT	Internet of Things
BGR	Bandgap Voltage Reference
VR	Voltage Reference
RF	Radio Frequency
BJT	Bipolar Junction Transistor
CTAT	Complementary-to-absolute-temperature
PTAT	Proportional-to-absolute-temperature
LS	Line Sensitivity
PSR	Power Supply Rejection
FoM	Figure of Merit
CMOS	Complementary Metal Oxide Semiconductor
SB	Self-Biased
Non-SB	Non-Self-Biased
ULV	Ultra-Low Voltage
ULP	Ultra-Low Power
WI	Weak Inversion
STI	Shallow Trench Isolation

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1 INTRODUCTION

In this chapter, we contextualize the need for both low power and low voltage building blocks for Internet of Things (IoT) applications. We start defining our motivation and how voltage references with the described characteristics can be applied in such systems. For a better understanding of the building block discussed in this master thesis, the concept of an ideal voltage reference and its expected features are presented. Finally, we state the contributions of this work and the organization of the rest of the thesis.

1.1 Motivation

The advent of the IoT and other low power applications has being a technological booster for the research efforts towards the design of low-power and low-voltage integrated circuits. Portable external and intra-body biomedical devices (SHI et al., 2016; MOHAN et al., 2017), based on energy harvesting systems (BANDYOPADHYAY et al., 2014), and energy-autonomous wireless sensor platforms and nodes (LEE et al., 2013; CHEN et al., 2016) are the main target of such circuits.

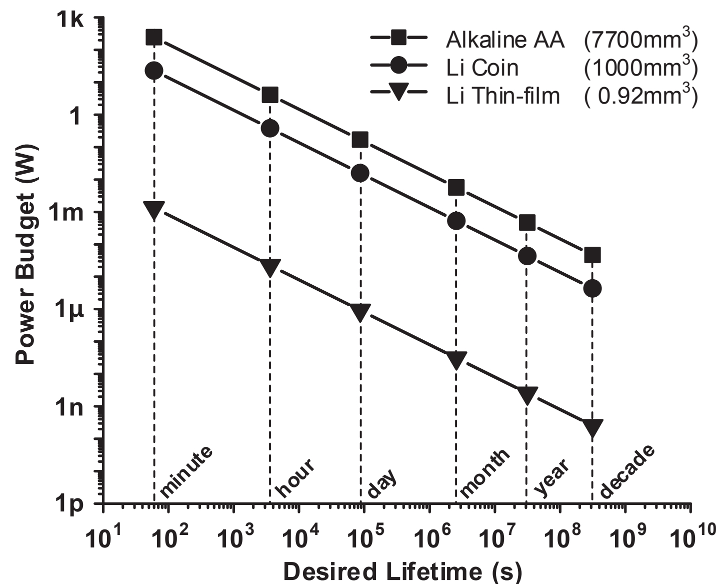


Figure 1.1: Lifetime of various batteries according to the system power consumption (JANG et al., 2015).

While some of these applications can be battery operated, the majority of recently developed solutions require full integration due to their size limitation. Fig. 1.1 shows the

lifetime of 3 types of batteries according to the system power consumption. As shown, if the system has a 10µW power consumption while being powered by a Lithium coin battery it can operate over a decade, but the size of such battery limits the application of the system powered by it. On the other hand, if the same system is powered Lithium thin-film battery, its operation would last just an hour or a day. The operation time of these systems can be increased by combining the battery operation with energy harvesting. By doing so, if the power harvested is large enough, the lifetime of the system will mainly depend on the recharge cycling capability of the battery used.

Based on these limitations, a general purpose sensor platform was proposed in LEE et al. (2013). The proposed platform significantly reduced the volume of the sensor system compared with previous approaches, which implies a larger and exciting range of applications. The whole system has an active power of approximately 50 µW while consuming less than 10 nW in standby. Each layer of the proposed sensor platform has its specific function such as power management, imager, timer, etc. Since the system is powered by a Lithium thin-film battery, the layers must be carefully designed to attain to the extremely limited power budget. As stated before, the operation time is extended by adding an energy harvesting layer, where a 3 nW power can be harvested from a solar cell.

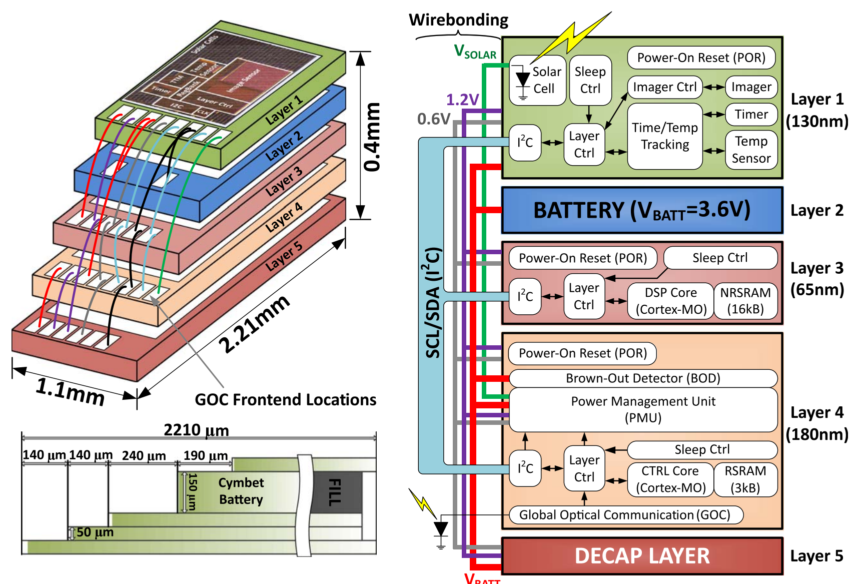


Figure 1.2: Layer structure and block diagram of a mm^3 general-purpose sensor platform (LEE et al., 2013).

In other works, the authors also have demonstrated sensors using the proposed platform, as shown in Fig. 1.3. In OH et al. (2014) a pressure sensor consuming less than 150 nW was demonstrated. A 71 nW temperature sensor was demonstrated in JEONG et al. (2014) and an imager and motion detector consuming 304 nW was presented in KIM et al. (2014). From the power management layer to the temperature sensors and timers, a circuit capable of providing a voltage that is stable in both temperature and supply voltage is needed. Moreover, since the power sources of such sensors are very limited, the voltage reference circuit must operate at both low power and low voltage. Even though the cited works also present solutions to satisfy their systems requirements, there are just a few circuits that can be used in such systems that can operate at sub-nW power consumption

range. And there is still space to improve the power/area efficiency of such low power reference generators.

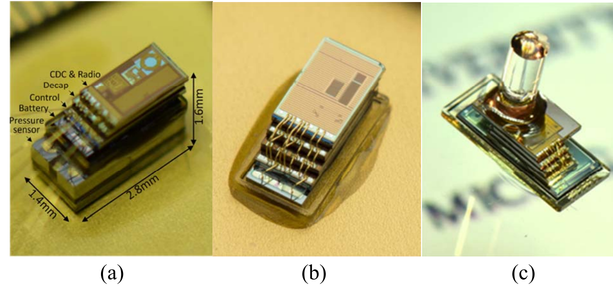


Figure 1.3: Examples for (a) Pressure, (b) Temperature and (c) Image/Motion detection sensors using the mm^3 platform (OH et al., 2014; JEONG et al., 2014; KIM et al., 2014).

Thus, to overcome the lack of different circuit topologies in front of a diverse application range, this thesis focus on the development of novel voltage references structures that can operate at pW power consumption level and can be applied in systems such as the ones previously discussed. Two variants of the same structure in a self-biased manner are presented. Moreover, a simple 3-Transistor (3T) voltage reference capable of providing an adjustable voltage reference within a strict range is also discussed.

1.2 Ideal Voltage Reference

One of the most fundamental building blocks for analog, RF, mixed-signal and also digital circuit applications is the voltage reference, being the so-called bandgap voltage reference (BGR) its most common implementation strategy. The conceptual diagram of an ideal BGR is shown in Fig. 1.4. As shown, the low-temperature sensitivity results when the junction diode (usually implemented as a bipolar transistor or BJT) complementary-to-absolute-temperature (CTAT) behavior is counterbalanced by a proportional-to-absolute-temperature (PTAT) source, resulting in the silicon bandgap voltage as the reference output around 1.23 V.

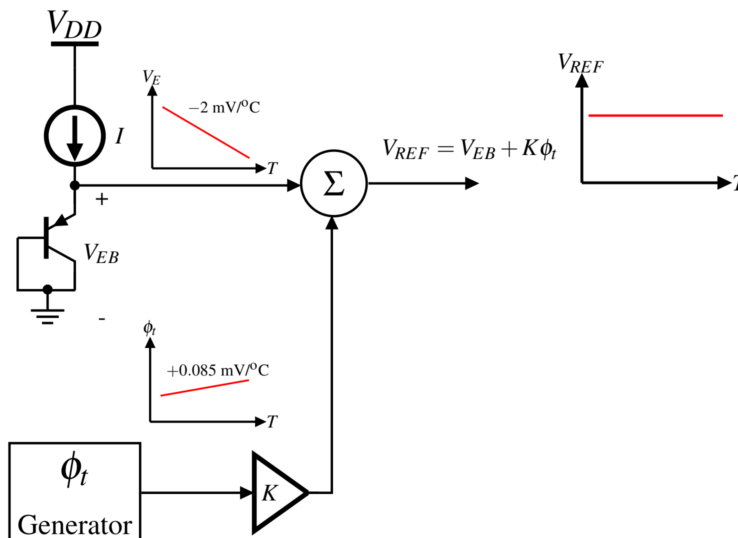


Figure 1.4: Conceptual diagram of an ideal bandgap voltage reference.

1.2.1 Performance Metrics

Ideally, a voltage reference must be independent of supply, temperature and process variations. However, for practical implementations, we must measure how sensitive to these variations a given voltage reference is. With this, the main performance metrics as discussed as follows.

1.2.1.1 Temperature Coefficient

The characteristics of the devices used to achieve the cancellation of temperature dependent terms vary with temperature and are not linear. Thus, it is not possible to reach complete suppression of the temperature dependence. Being so, a parameter that measures how the voltage reference varies with respect to a defined temperature range is the temperature coefficient (TC) and it is usually given in ppm/°C. The TC can be obtained by the following expression

$$\mathrm{TC} = \frac{V_{\mathrm{REFMAX}} - V_{\mathrm{REFMIN}}}{(T_{\mathrm{MAX}} - T_{\mathrm{MIN}})V_{\mathrm{REF27\,^{o}C}}} \times 10^{6} \tag{1.1}$$

where V_{REFMAX} and V_{REFMIN} are the maximum and minimum values for the voltage reference within the $[T_{\mathrm{MAX}} - T_{\mathrm{MIN}}]$ temperature range, and $V_{\mathrm{REF27\,^{o}C}}$ is the voltage reference at room temperature (27 °C).

1.2.1.2 Line Sensitivity

The sensitivity of a reference voltage with respect to supply voltage variations is commonly evaluated through the line sensitivity (LS) parameter. The LS is defined as

$$\mathrm{LS} = \frac{\Delta V_{\mathrm{REF}}}{\Delta V_{DD} \times V_{\mathrm{REF\mu}}} \times 100\% \tag{1.2}$$

with ΔV_{DD} being the V_{DD} range of operation, ΔV_{REF} is the absolute difference of the reference voltage in the V_{DD} range considered and $V_{\mathrm{REF\mu}}$ is the mean value of the voltage reference within the ΔV_{DD} range. The LS is evaluated at a reference temperature, usually 20 °C to 27 °C.

1.2.1.3 Power Supply Rejection

The ability of the voltage reference circuit to reject interferences coming from the supply voltage is given by the Power Supply Rejection (PSR) parameter. The PSR is a function of frequency and is expressed in dB as

$$\mathrm{PSR} = 20\log\left(\frac{V_{\mathrm{REF}}(f)}{V_{DD}(f)}\right) \tag{1.3}$$

where the power supply plus the incoming noise at a particular frequency f is given by $V_{DD}(f)$ and $V_{\mathrm{REF}}(f)$ is the AC coupled voltage reference measured at the output. The behavior of the PSR over a wide range of f can be described as the variation of the voltage reference corrupted by the supply noise (KOK; TAM, 2013).

1.2.1.4 Other Design Considerations

Besides the main performance metrics that must be taken into account while designing a voltage reference circuits, other important specifications must be met and need specific attention. Among these are (KOK; TAM, 2013):

- silicon occupied area
- power consumption
- device mismatch
- trimming ability

Different than the performance metrics discussed in the above subsections, these specifications must the considered in every step. For example, to achieve a given LS specification the high-impedance devices must be adjusted in size, but still, they need to attain to the maximum area available for the circuit, and the maximum mismatch variability allowed in the design.

1.2.2 Figure of Merit

A voltage reference circuit has various performance specifications being represented for a single value for each characteristic, as it was presented in the previous section. This means that is difficult to evaluate how suitable a voltage reference is for a given application when it is compared to other circuits. For this reason, it is important to define a figure of merit (FoM) to provide us a value that represents the overall performance of a given voltage reference.

A FoM that considers the main performance metrics of a voltage reference circuit: temperature range, TC, power, and occupied area was described in WIESSFLECKER et al. (2012), and used for comparison purposes by Prof. Willy Sansen in its Advanced Analog Circuit Design course (SANSEN, 2015). The proposed FoM is given by

$$\text{FoM} = \frac{(T_{\text{MAX}} - T_{\text{MIN}})^2}{\text{TC} \times \text{Power} \times \text{Area}} \tag{1.4}$$

Usually, first-order compensated voltage references present a parabola-like curve across temperature. This means that as the temperature goes far from the reference point, let's say room temperature, the voltage reference becomes more sensitive to temperature. Therefore, the temperature range $(T_{\text{MAX}} - T_{\text{MIN}})$ is squared in order to add value to a wider temperature range of operation. The product between TC, power at room temperature and area, must be as lowest as possible, this means that resistorless solutions will be benefited, while exists a hard trade-off between area and power consumption for circuits based on resistors.

1.3 Contributions of This Work and Organization

In Chapter 2, we start by making a historical review of the voltage reference development. From the concept proposal to the application of a low power voltage reference in the electronic watch, the main advances over the years are discussed. Following this discussion, we focus to the recent developments of low power and low voltage CMOS voltage references. The operation principle and major accomplishments of papers from the last ten years are discussed.

Based on the state-of-the-art discussed, Chapter 3 presents the proposed circuits. Two variants of the same structure are presented: a self-biased self-cascode MOSFET (SBSCM), and a self-biased NMOS (SBNMOS) voltage reference. The combination of a self-biasing scheme with the usage of high-V_T transistors results in both circuits operating

at pW power consumption range while operating at 0.45-0.6 V minimum supply voltage. The voltage reference generation of the proposed SBSCM and SBNMOS are mainly defined by the distinct V_T of 1.8 V and 3.3 V transistors. This lead to circuits more sensitive to process variations. To attenuate the process variability, we also propose another voltage reference based on the self-cascode, but instead of using different V_T devices, the V_T difference is obtained by exploiting the reverse short-channel effect (RSCE). The circuit is biased by the leakage current of a native transistor (zero-V_T), resulting in a 3-Transistor (3T) voltage reference. Due to its simplicity, the circuit can operate at minimum supply voltages of 0.12-0.4 V while consuming just a few fW to pW.

The simulation and measurement results of the proposed circuits are presented in Chapter 4. The SBSCM and SBNMOS were fabricated in a standard 0.18-µm CMOS process, while the 3T voltage references were fabricated in 0.13-µm. Measurement results of 24 for the circuits fabricated in 0.18-µm are presented. Four different versions of the 3T circuits are designed to show how versatile the proposed solution is. Comparison results shows that the proposed SB-VRs presented 47.5× and 7.75× power and area improvement, respectively, with the best FoM performance when compared to Non-self-biased (Non-SB) solutions. Besides presenting the highest FoM, the 3T VRs versions also presented the lowest minimum supply voltage, silicon area, and power consumption when compared to all works used for comparison purposes.

Finally, Chapter 5 presents the conclusion of this work where the main contributions and applications for future works are discussed.

2 INTEGRATED VOLTAGE REFERENCES

This chapter aims to present the historical evolution of the temperature-compensated voltage references and their state-of-the-art. For such, a group of papers that the author considers relevant for the development of this thesis is discussed.

2.1 Historical Overview

The first concept of a temperature-compensated bandgap voltage reference was proposed by HILBIBER (1964). In its ISSCC paper, Hilbiber shows that different discrete NPN bipolar transistors (BJT) present different magnitudes of both V_{BE} and dV_{BE}/dT, and that the variation of the current density for the same device also has the same effect. Thus, by taking the difference of such V_{BE} values, a PTAT source can be generated. The scheme of the proposed reference concept is shown in Fig. 2.1, where by adjusting the bias currents $I_{1,2}$ and the number of series BJT diodes r and m the first order temperature dependence of the silicon bandgap voltage can be eliminated. Therefore, a voltage reference of 1.25 V is achieved. Although Hilbiber presented a new voltage reference standard, his proposed scheme used discrete devices and thus was not suitable for integrated applications.

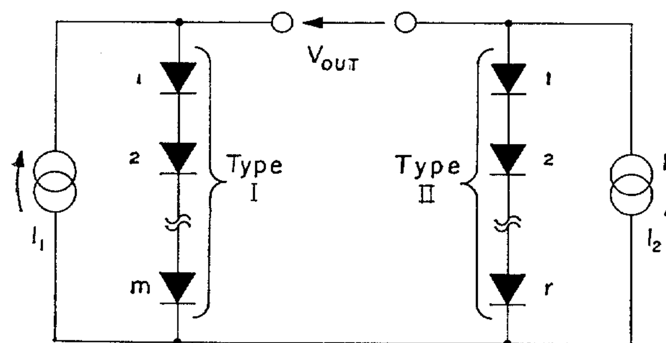


Figure 2.1: Scheme of the voltage reference concept proposed by HILBIBER (1964).

In the early 60's, a common approach to achieve a temperature-compensated voltage reference was with the usage of zener diodes. But their breakdown voltage, around 5 to 6 V, also impose a lower limit for the minimum input voltage of regulators. Attained to this need, the first practical implementation of an integrated BGR was proposed by WIDLAR (1971), which was based on the concept of Hilbiber. The simplified schematic of the circuit proposed by Widlar in shown in Fig. 2.2. In the circuit, Q_1 operates with a current density about 10 times the one of Q_2, and the ΔV_{BE} between Q_1 and Q_2 appears across R_3.

Q_3 is defined as the gain stage that regulates the output voltage through a current feedback loop at the output node.

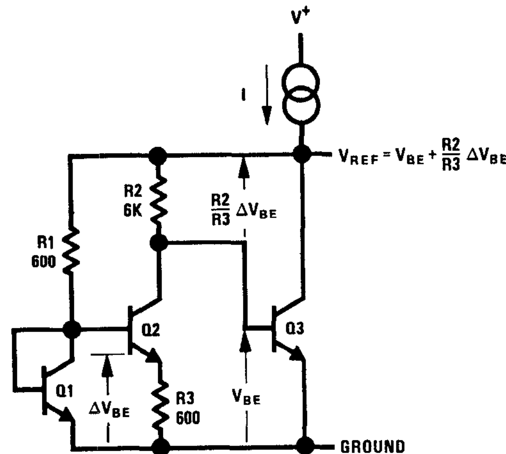


Figure 2.2: First practical bandgap voltage reference proposed by WIDLAR (1971).

Two years later, KUIJK (1973) proposed another structure of a temperature-compensated bandgap voltage reference. The schematic of the proposed circuit is shown in Fig. 2.3. In Kuijk's circuit, the operational amplifier forces $V_{BE1} = I_2R_3 + V_{BE2}$ making that ΔV_{BE} appears across R_3 resulting I_2 proportional to ΔV_{BE}. The temperature behavior of the BJT diode D_1 can be temperature compensated by adjusting the R_1, R_2 and R_3 values. Thus, for an optimal first-order compensation, the circuit provides at its output the bandgap voltage as the reference.

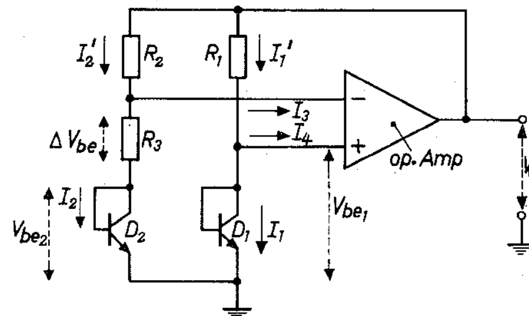


Figure 2.3: Bandgap voltage reference proposed by KUIJK (1973).

Aiming the development of low-power circuits for the electronic watch at the CEH (Centre Electronique Horloger or "Watchmakers Electronic Center") founded in 1962, Eric Vittoz pioneered the weak inversion (WI) MOSFET operation (or subthreshold operation) for analog CMOS, providing a model directly applicable to hand-design (VITTOZ; FELLRATH, 1977). In their paper, Vittoz and Neyroud presented current references and a quartz oscillator scheme operating in WI with a sub-µW power consumption, demonstrating the reliability of WI operation.

The first bandgap voltage reference operating at such region was presented by TSIVIDIS; ULMER (1978). The authors observed that a PTAT voltage source could be realized through the $I_D - V_G$ exponential characteristics of the MOS transistor operating in WI. This was demonstrated by taking the difference between the gate-to-source voltage

of two MOS transistor in WI with different current densities (I_D/S). An unbalanced differential pair was used to perform the difference function of the two MOS transistors. By arranging more transistors in series, the PTAT term is adjusted to perform the temperature compensation. The final implementation of the proposed WI bandgap voltage reference is shown in Fig. 2.4.

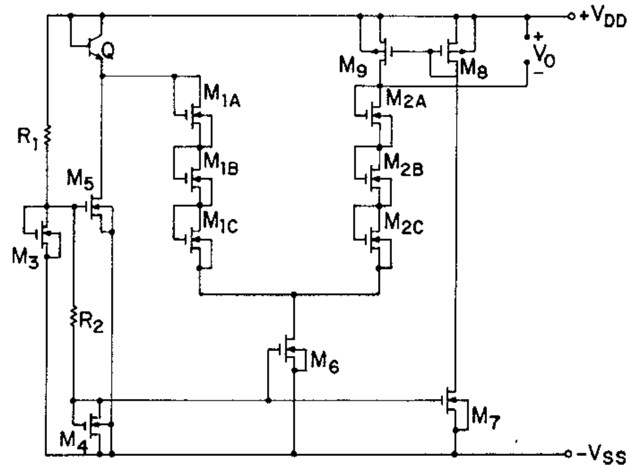


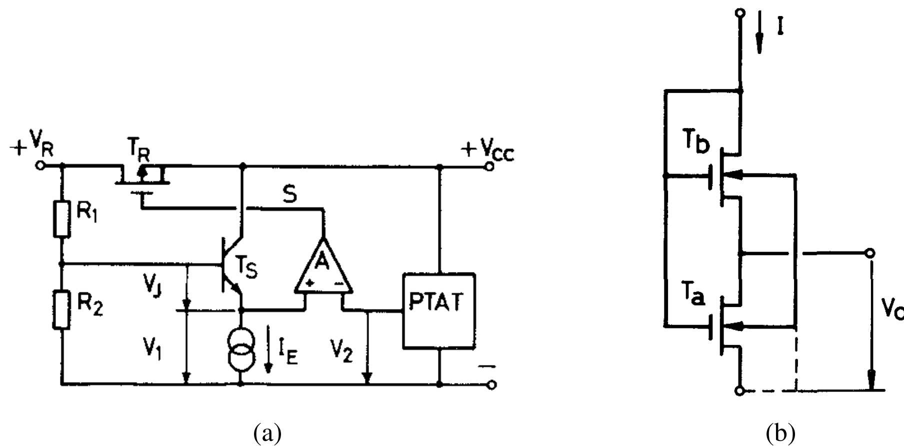
Figure 2.4: Bandgap voltage reference proposed by TSIVIDIS; ULMER (1978).

As Vittoz stated on VITTOZ (2008), the electronic watch also needed auxiliary circuits which, among them, was a circuit to detect the end of the battery life. Thus, a precise low-power bandgap voltage reference was required to be implemented in CMOS. Even though having transistors operating in WI, the circuit proposed by TSIVIDIS; ULMER (1978) operates with a 10 V supply while consuming 16 μA, making it not suitable for the electronic watch application. Thus, a low-voltage bandgap voltage reference was proposed by VITTOZ; NEYROUD (1979). The block diagram of the proposed circuit is presented in Fig. 2.5. As shown in the block diagram in Fig. 2.5(a), the bandgap voltage reference is achieved by combining the base-emitter voltage of the BJT with series self-cascode PTAT voltage generators composed of MOS transistors operating in WI (Fig. 2.5(b)). The proposed circuits could operate at minimum supply voltages of 1.3 V while consuming less than 1 μW. Resistors R_1 and R_2 are used as a gain factor to adjust V_R as proportional to $V_J + V_1$.

Another bandgap voltage reference proposed aiming the electronic watch application was the one described in OGUEY; GERBER (1980). Different than previous approaches that were mainly based on the BJT the author exploited bi-doped poly process, where the same type of transistor with opposite types of gate doping present different threshold voltages. Thus, by setting the threshold voltage difference of two NMOS transistors as the bandgap voltage, a circuit that provides at output their gate-to-source voltage difference is implemented. Using this principle, the authors proposed two bandgap reference circuits being one providing a positive and the other a negative bandgap voltage reference. The proposed negative voltage reference is shown in Fig. 2.6.

Without compensation, the circuit presented a TC of 300 ppm/°C, while by adjusting the currents at T_1 and T_2 branches the bandgap voltage reference can be temperature-compensated and reaches a TC of ±30 ppm/°C. This circuit can operate at a minimum supply voltage of 1.5 V while consuming only 0.2 μW.

The 1.25 V output voltage of the BGRs proposed until the beginning of 80's and the



(a) (b)

Figure 2.5: Block diagram of the bandgap voltage reference (a) and PTAT voltage generator (b) proposed by VITTOZ; NEYROUD (1979).

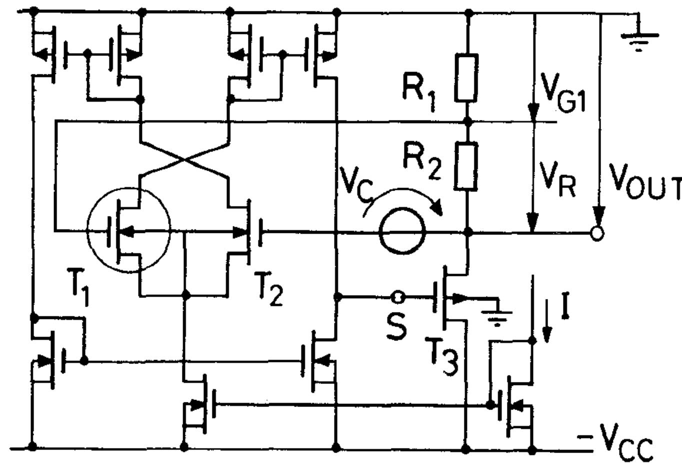


Figure 2.6: Negative bandgap voltage reference proposed by OGUEY; GERBER (1980).

mid-90's puts a lower limit for the minimum supply voltage, implying that they cannot operate with power supplies lower than 1.5 to 1.8 V. Thus, due to V_{DD} downscaling of the CMOS technology, the usage of such BGRs were somehow impractical. To solve this problem, a sub-1 V supply and sub-bandgap voltage reference was proposed by BANBA et al. (1999).

The circuit that was proposed by BANBA et al. (1999) is mainly based on the conventional BGR proposed by WIDLAR (1971). The proposed structure is shown in Fig 2.7. In this circuit the OPAMP forces $V_b = V_a$, by doing so a CTAT current flows through R_2 defining $I_{2b} = V_{f1}/R_2$, while a PTAT current flows through R_3 with this current given by $I_{2a} = \Delta V_f/R_3$. Therefore, by adjusting the gains of the PTAT and CTAT generated currents at this branch, a reference current is given by $I_2 = I_{2a} + I_{2b}$. The reference current is then mirrored to a resistor branch to generate the reference voltage V_{REF}. Thus, the proposed voltage reference can provide a wide range of output values that will depend on the current I_3 and the output resistor R_4 with $V_{REF} = I_3 R_4$, therefore allowing sub-bandgap output and sub-1 V power supply.

Until the early 00's the BGRs and sub-BGRs were mainly composed of MOS transistors, OPAMPs and resistors, where the resistors played a major role in the occupied

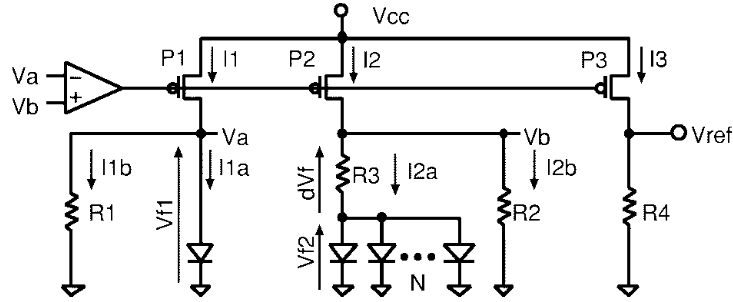


Figure 2.7: Sub-1 V and sub-bandgap voltage reference proposed by (BANBA et al., 1999).

silicon area, reflecting on the cost of the proposed solutions. To solve this, BUCK et al. (2002) proposed a BGR without resistors based only on MOS transistors and diodes. The circuit proposed by Buck is shown in Fig. 2.8.

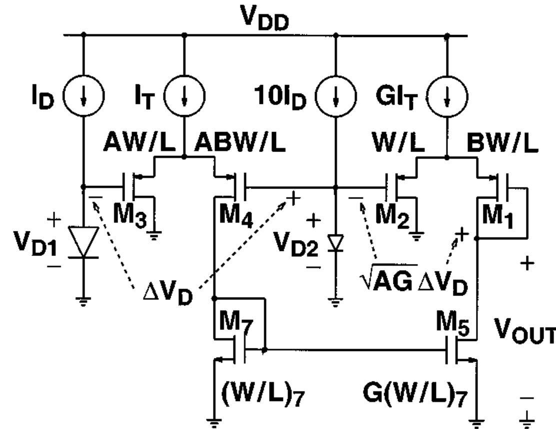


Figure 2.8: Bandgap voltage reference without resistors proposed by (BUCK et al., 2002).

The proposed circuit can be simply described as the combination of unbalanced voltage-to-current transducers (TORRANCE; VISWANATHAN; HANSON, 1985) where the temperature behavior of the diode D_1 can be temperature-compensated by adjusting the current gain $\sqrt{AG}$, which is the gain of the PTAT term of the BGR.

Even though BGRs and sub-BGRs present adequate performance for many applications, their BJT-based arrangement still limits their minimum current consumption and supply voltage, which is not desirable for low power and low voltage applications. In contrast, as discussed, MOSFET subthreshold operation (VITTOZ; NEYROUD, 1979) can offer an interesting alternative for both low power and low voltage operation. In the next section, we discuss the recent advances of resistorless and BJT-less voltage references that operate at low power and low voltage.

2.2 State-of-The-Art of Low Power and Low Voltage CMOS Voltage References

This section aims to present the recent advances in the development of low power voltage references in CMOS technology. Papers published in the last ten years in relevant

journal and conferences were selected. The following sections will discuss the main ideas and contributions of each paper. The focus of the discussion are solutions that operate at sub-1 V supply voltage and are at pW and nW power consumption range.

2.2.1 NMOS Diode in Strong Inversion

In VITA; IANNACCONE (2007) a resistorless CMOS voltage reference operating at sub-1 V supply voltage while consuming less than 100 nW is proposed. This is done by exploiting the different V_T MOS transistors characteristics in both saturation and sub-threshold operation.

Let us first define the I-V characteristics of an NMOS transistor in strong inversion:

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{2.1}$$

where μ is the electron mobility in the channel, C_{ox} is the oxide capacitance per unit area, V_{th} is the threshold voltage, λ is the channel length modulation coefficient, and W and L are the channel width and length, respectively.

The schematic of the proposed circuit is shown in Fig. 2.9. Now, consider that the active load at output stage provides a voltage reference as

$$V_{REF} = V_{th10} + \sqrt{\frac{2I_0}{k_{10}}} \tag{2.2}$$

where $k_{10} = \mu C_{ox}(W/L)_{10}$. As (2.2) shows, the temperature coefficient of V_{REF} is dependent of three factors: the first order dependence of V_{th} with respect to temperature, the μ temperature dependence and that from the bias current I_0.

As presented in the same paper, the V_{th} dependence with respect to temperature is given by

$$V_{th} = V_{th}(T_0) - K_{t1}(T - T_0) \tag{2.3}$$

where T is the absolute temperature, T_0 is the reference temperature (usually room temperature) and K_{t1} is the first order V_{th} temperature slope. Thus, through this definition, it is possible to note that for perfect of the mobility and threshold temperature dependence, the generated bias current must be given as $I_0 \propto \mu(T)T^2$, and that is provided by the current generator presented in Fig. 2.9.

In the proposed circuit, transistors M_1-M_4 are the core of the I_0 current generation and M_5-M_8 form the current mirrors that guarantee the same current flowing in all the branches. The generated current is then mirrored through M_9 to the active load M_{10}. M_1 and M_3 are 5-V NMOS transistors with V_{th} of 0.7 V, while all other transistors are 3.3-V transistors being the NMOS V_{th} around 0.5 V. By using devices with different threshold voltages it is possible to simultaneously bias them in weak (5 V transistors) and strong (3.3 V transistors) inversion. The drain current in weak inversion can be approximated as

$$I_D = \mu C_{ox} V_T^2 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{th}}{mV_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{2.4}$$

where $V_T = kT/q$ is the thermal voltage, m is the subthreshold slope factor and I_D of (2.4) becomes independent of the drain-to-source voltage for $V_{DS} > 3 \sim 4V_T$.

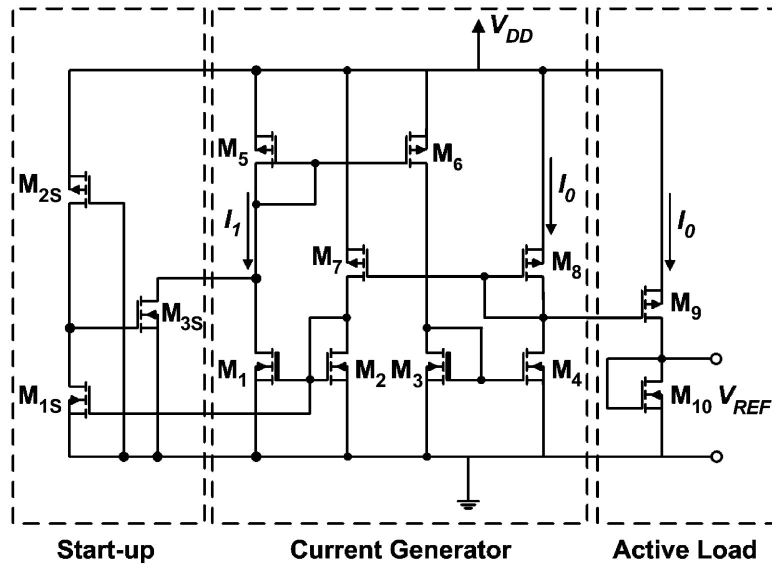


Figure 2.9: Sub-1 V supply voltage reference proposed by VITA; IANNACCONE (2007).

Now, through expressions (2.1) and (2.4) the current generated by the proposed circuit considering all transistors saturated is given by

$$I_0 = \frac{\mu C_{ox} W_4/L_4}{2(N-1)^2} m^2 V_T^2 \ln^2\left(\frac{W_3/L_3}{W_1/L_1}\right) \tag{2.5}$$

where $N = \sqrt{(W_4/L_4)/(W_2/L_2)}$. By replacing (2.5) into (2.2) the generated voltage reference is finally given by

$$V_{REF} = V_{th10} + \frac{mV_T}{N-1}\sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}}\ln\left(\frac{W_3/L_3}{W_1/L_1}\right) \tag{2.6}$$

Thus, the proposed circuit provides at output a temperature-compensated voltage reference with complete suppression of both V_{th} and μ temperature dependences. The authors fabricated the circuit in a standard 0.35 µm CMOS process and tested 20 samples from the same batch. Experimental results showed a mean voltage reference of 670 mV. The circuit operated at a minimum supply voltage of 0.9 V while consuming 36 nW. From 0 to 80 °C the circuit presented a small TC of 10 ppm/C°C. Besides not using any resistors, at the time this circuit was one of the first to operate at supply voltage below 1 V while achieving nW power consumption.

2.2.2 Sub-bandgap Reference with Different Threshold Transistors

Using transistors with different oxide thickness rather than different implants to obtain different threshold voltages, YAN; LI; LIU (2009) proposed two sub-bandgap voltage references. The schematic of the proposed circuits is shown in Fig. 2.10. In both cases, output voltage is the difference between the gate-to-source voltages of the thick and thin NMOS devices and its given by

$$V_{REF} = V_{gs,tk} - V_{gs,tn} = V_{th,tk} - V_{th,tn} + \frac{nkT}{q}\ln\left(\frac{t_{ox,tk}(W_{tn}/L_{tn})}{t_{ox,tn}(W_{tk}/L_{tk})}\right) \tag{2.7}$$

For both versions, the output voltage is independent of the temperature dependence of the bias current. A resistorless current reference (OGUEY; AEBISCHER, 1996) is used to bias the proposed circuits.

(a)

(b)

Figure 2.10: Circuits proposed in YAN; LI; LIU (2009).

The proposed circuits provided at the output mean voltage references of 96.6 and 108.9 mV. Temperature coefficients of 9.2-11.4 ppm/°C were obtained. Both operate with a minimum supply voltage of 1.1 V and consume less than 30 nA. Even though the core of both versions can operate at low voltages, the usage of the resistorless current reference based on an NMOS transistor in triode makes sub-1 V supply operation not feasible. But still, its power consumption was less than that obtained from VITA; IANNACCONE (2007).

2.2.3 NMOS Diode in Weak Inversion

In MAGNELLI et al. (2011) an MOS-only voltage reference with all transistors operating in weak inversion is explored to minimize both power consumption and supply voltage. The simplified scheme of the voltage reference proposed by the authors is pre-

sented in Fig. 2.11.

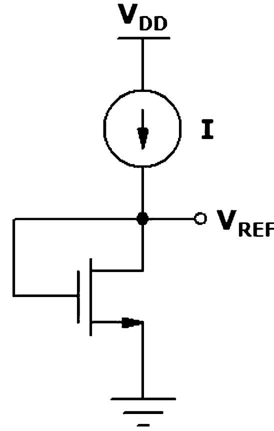


Figure 2.11: Simplified scheme of the voltage reference proposed by MAGNELLI et al. (2011).

Through the expression of the drain current in weak inversion, the voltage reference provided by the circuit is given by

$$V_{REF} = V_{GS} = V_{th} + mV_T \ln\left(\frac{I_D}{S\mu V_T^2}\right) \tag{2.8}$$

Different than what was done in VITA; IANNACCONE (2007), which presents a temperature compensated NMOS load in strong inversion, the authors observe that for (2.8) to be temperature compensated while operating in weak inversion, i.e. $V_{REF} < V_{th}$, the drain current I_D must have the following temperature dependence

$$I_D(T) = \alpha\mu T^2 \exp\left(\frac{AT+B}{CT}\right) \tag{2.9}$$

where A, B and C are constant with temperature. Thus, by setting the term B/C as a negative constant, the condition of $V_{REF} < V_{th}$ for the NMOS load to be operating in subthreshold can be guaranteed.

The electrical configuration that provides such temperature-compensated voltage reference is shown in Fig. 2.12. The circuit is composed of a self-biased current source, an NMOS active load, and a start-up circuit. Transistors M_1-M_7 form the current source, M_9 and M_{10} the voltage reference generation core, and transistors M_{1S}-M_{7S} compose the start-up. All the transistors operate in weak inversion with M_2 and M_{1S} high-V_{th} and the rest of the transistors being standard V_{th} ones. From M_1-M_3 we have

$$V_{GS2} = V_{GS1} + V_{GS3} \tag{2.10}$$

From their drain current operating in weak inversion, the generated current I_1 is given by

$$I_1 = Q^{1/\Sigma_m}\mu \exp\left(-\frac{\Delta V_{th}}{V_T \sum_m}\right) \tag{2.11}$$

where $\Delta V_{th} = V_{th1} + V_{th3} - V_{th2}$, $Q = a^{m_2-m_3}(S_3^{m_3}S_1^{m_1}/S_2^{m_2})$, $\sum_m = m_1 + m_3 - m_2$ and $a = S_7/S_5$. As one can see, the current reference architecture generates a current in the

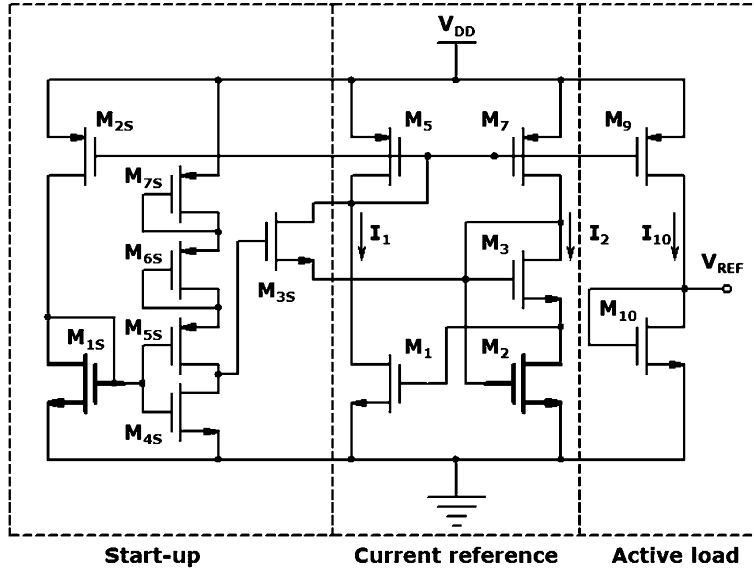


Figure 2.12: Electrical configuration proposed by MAGNELLI et al. (2011).

form of (2.9). Then, the generated current is mirrored into the NMOS active load with a current gain of $I_{10}/I_1 = S_9/S_5 = c$. Therefore, since M_{10} operates in weak inversion, form (2.8) and (2.11), the generated voltage reference is given by

$$V_{REF} = V_{th10} + m_{10} V_T \ln \left(Q^{1/\Sigma_m} \frac{c}{S_{10}} \right) - \frac{m_{10}}{\Sigma_m} \Delta V_{th} \tag{2.12}$$

The temperature dependence of the reference voltage is mainly dependent on the thermal behavior of V_T and V_{th}. According to the temperature dependence of V_{th} and setting $\partial V_{REF}/\partial T = 0$, the optimal S_{10} ratio can be expressed as

$$S_{10} = \frac{Q^{1/\Sigma_m}/C_{ox10}}{\exp\left[\frac{q}{kT_0}\left(\frac{1}{\Sigma_m}(K + k_{t2,3}V_{BS3}) - \frac{k_{t1,10}}{m_{10}}\right)\right]} \tag{2.13}$$

where $K = k_{t1,1} + k_{t1,3} - k_{t1,2}$ ($k_{t1,i}$ and $k_{t2,i}$ are the threshold voltage temperature coefficients of the i-th transistor).

Hence, by satisfying (2.13), and considering that $m_{10}/\Sigma_m \approx 1$ and $k_{t1,1} \approx k_{t1,2} \approx k_{t1,3} \approx k_{t1,10}$, a simplified expression for V_{REF} can be obtained as

$$V_{REF} = V_{th,HVT}(T_0) - V_{th,SVT}(T_0) \tag{2.14}$$

Therefore, the proposed circuit provides at its output a voltage reference that is approximately the difference between the threshold voltage of a high-V_{th} (HVT) and a standard-V_{th} (SVT).

The proposed circuit provides a mean voltage reference about 263.5 mV while operating at a minimum supply voltage of 0.45 V. From 0 to 125 °C its TC is about 142 ppm/°C, and a line sensitivity of 0.44 %/V from 0.45 to 2 V supply. Due to its very low minimum supply voltage and an all-subthreshold configuration, the proposed circuit consumes only 2.6 nW, which is a remarkable reduction compared with prior works.

2.2.4 Picowatt 2-Transistor Voltage Reference

A voltage reference capable of operating at a minimum supply voltage of 0.5 V while consuming units of pW was proposed in SEOK et al. (2012). As shown in Fig. 2.13, the proposed circuit was a breakthrough on the design of voltage references since it presented a 1000× and 10× less power and area, respectively, when compared to prior voltage references. The ultra-low power consumption is achieved by avoiding operational amplifiers and transistors operating in strong inversion. As a result, a very simple structure composed only of 2 transistors (2T) is proposed.

Figure 2.13: Power and area comparisons present in SEOK et al. (2012).

The schematic of the 2T voltage reference is shown in Fig. 2.14. The proposed circuit is composed of a zero-V_T transistor (M_1) and a regular thick-oxide I/O (M_2). Both transistors operate in weak inversion and are saturated.

	W_1/L_1	W_2/L_2
0.13µm	3.3/60	1.5/60
0.18µm	7/20	8/20
65nm	14/1.2	27/0.6

Figure 2.14: Schematic of the proposed 2T voltage reference (SEOK et al., 2012).

Thus, through the definition of the subthreshold current, their drain currents will be given by

$$I_{D1} = \mu_1 C_{ox1} \frac{W_1}{L_1} (m_1 - 1) V_T^2 \exp\left(\frac{-V_{REF} - V_{th1}}{m_1 V_T}\right) \tag{2.15}$$

$$I_{D2} = \mu_2 C_{ox2} \frac{W_2}{L_2} (m_2 - 1) V_T^2 \exp\left(\frac{V_{REF} - V_{th2}}{m_1 V_T}\right) \tag{2.16}$$

Since $I_{D1} = I_{D2}$, the voltage reference will be simply

$$V_{REF} = \frac{m_1 m_2}{m_1 + m_2}(V_{th1} - V_{th2}) + \frac{m_1 m_2}{m_1 + m_2} V_T \ln\left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right) \tag{2.17}$$

where both first and second terms are either PTAT or CTAT. Thus, by properly sizing M_1 and M_2, a temperature-compensated voltage reference can be achieved. To design the circuit for low power and low LS, the channel length of both transistors are set to the maximum allowed by the process design rules. By doing so, the optimal ratio between the two transistors width can be obtained by setting $\partial V_{REF}/\partial T$ = 0, which leads to the following equation

$$\left(\frac{W_1}{W_2}\right)_{opt} = \frac{\mu_2 C_{ox2} L_2}{\mu_1 C_{ox1} L_1} \exp\left(\frac{q}{k}(C_{V_{th2}} - C_{V_{th1}})\right) \tag{2.18}$$

where q is the charge of an electron, k is the Boltzmann's constant and $C_{V_{th}}$ is the first order temperature coefficient of the threshold voltage. The transistors sizes for each process used to design the circuit is also shown in Fig. 2.14. One drawback of such reference is the minimum limit for V_{REF} to guarantee that M_2 is saturated. As stated by the authors, this value is around 170-200 mV.

The circuit was fabricated in 0.18-µm, 0.13-µm, and 65 nm processes, but the main results are presented as the obtained from the 0.13-µm runs. The measurements results of the 0.13-µm showed an average TC of 62 ppm/^{o}C across 49 samples. PSR is measured to be -67 dB at 100 kHz with a 0.8 pF output capacitance. The power consumption of the 2T voltage reference is 2.22 pW at 0.5 V supply voltage and 20 ^{o}C, and reaches a maximum of 243 pW at 3 V and 80 ^{o}C. The LS from 0.5 to 3 V is about 0.033 %/V.

From the two runs in 0.13-µm, the average output voltage was 176.1 mV and 176.7 mV, with standard deviations of 1.5 mV and 1 mV, respectively. Within the -20 to 80 ^{o}C temperature range the average TCs from the two runs were 56 and 67 ppm/^{o}C with standard deviations of 31 and 49 ppm/^{o}C. To minimize the output voltage spread while meeting a specific TC constraint, the authors also proposed a trimming scheme for the 2T circuit. The trimmable version of the 2T voltage reference is shown in Fig. 2.15. The correlation between TC and output voltage was obtained by measuring the TC for all possible trimming combinations. With this, the authors targeted a TC of less than 50 ppm/^{o}C with the lowest output voltage spread. Also, a one temperature point (80 ^{o}C) trimming is investigated to minimize the time associated with it. Across 25 dies, the trimming reduces the spread of TC and output voltage by 9.6× and 9.8×, respectively, when compared to pre-trimming results.

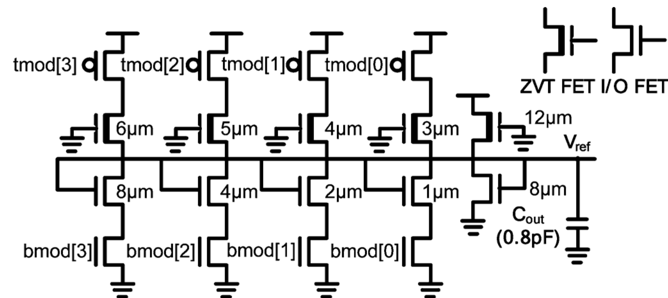


Figure 2.15: Schematic of trimmable 2T voltage reference (SEOK et al., 2012).

2.2.5 Sub-kT/q Voltage Reference

The ultra-low power voltage references discussed so far were mainly based on the usage of transistors with different threshold voltages to generate the output voltage. The use of such different devices might lead to a wider spread of both TC and output voltage, due to distinct doping process for each device. In ALBANO et al. (2015) the dependence of the threshold voltage with transistor dimensions is exploited to obtain a threshold voltage difference. By doing so, the authors were capable of providing a sub-kT/q output voltage while operating at a minimum supply voltage of 150 mV.

The schematic of the 2T structure used in ALBANO et al. (2015) is shown by Fig. 2.16. In this approach M_1 and M_2 are standard transistors, different than SEOK et al. (2012) which uses a native one to implement M_1.

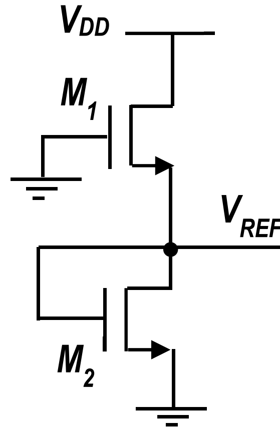


Figure 2.16: 2T structure used in ALBANO et al. (2015).

Since both transistors operate in weak inversion, from expression (2.4), their drain currents are given by

$$I_1 = \mu_{n1} C_{ox1} \left(\frac{W}{L}\right)_1 V_T^2 \exp\left(-\frac{V_{REF}+V_{TH1}}{n_1 V_T}\right) \times \left(1 - \exp\left(-\frac{V_{DD}-V_{REF}}{V_T}\right)\right) \tag{2.19}$$

$$I_2 = \mu_{n2} C_{ox2} \left(\frac{W}{L}\right)_2 V_T^2 \exp\left(-\frac{V_{REF}+V_{TH2}}{n_1 V_T}\right) \times \left(1 - \exp\left(-\frac{V_{REF}}{V_T}\right)\right) \tag{2.20}$$

Since the design uses MOSFETs of the same type, we have $C_{ox1} \approx C_{ox2} = C_{ox}$ and $n_1 \approx n_2 = n$. Transistor M_1 implements a current source to bias the M_2 load, this means that for it to be saturated $V_{DD} > 4V_T + V_{REF}$ condition must be guaranteed. By assuming this, the following expression is obtained

$$\ln\left[\left(\frac{W}{L}\right)_R \frac{\mu_{n1}}{\mu_{n2}}\right] = \frac{2V_{REF}+\Delta V_{TH}}{nV_T} + \ln\left(1 - \exp\left(-\frac{V_{REF}}{V_T}\right)\right) \tag{2.21}$$

where $(W/L)_R = (W/L)_1/(W/L)_2$ and $\Delta V_{TH} = V_{TH1} - V_{TH2}$. But to obtain an explicit solution for V_{REF}, a linear approximation of the logarithmic term has to be done

$$\ln\left(1 - \exp\left(-\frac{V_{REF}}{V_T}\right)\right) \approx A + B\frac{V_{REF}}{V_T} \tag{2.22}$$

Being A and B the two fitting parameters, which are dependent on the chosen interval of V_{REF}. Since the design goal is to provide a sub-kT/q output voltage, the internal of V_{REF} is set as $V_T/2$ to V_T, which leads to $A \approx$-1.35 and $B \approx$0.92 as fitting parameters.

By considering the threshold voltage temperature dependence given by expression (2.3), the optimal $(W/L)_R$ ratio obtained from $\partial V_{REF}/\partial T$=0, and that the threshold voltage temperature coefficient can be neglect at room temperature, the following expression for the temperature-compensated voltage reference is obtained

$$V_{REF} \approx \frac{V_{TH2}(T_0) - V_{TH1}(T_0)}{2 + nB} \tag{2.23}$$

To obtain a threshold voltage difference using the same types of transistors, the threshold voltage dependence concerning transistor dimensions is explored, as presented in Fig. 2.17. This shows that a significant V_{TH} difference between small and long channel devices can be obtained and that V_{TH} is almost independent of the channel width for $W > 30$ µm.

In SEOK et al. (2012), the output voltage was stated to be around 0.75ΔV_{TH}. In the case of ALBANO et al. (2015), because M_2 operates in triode, the $2 + nB$ term lowers even more the output voltage for a given ΔV_{TH}. Which might be a problem if the ΔV_{TH} is too small.

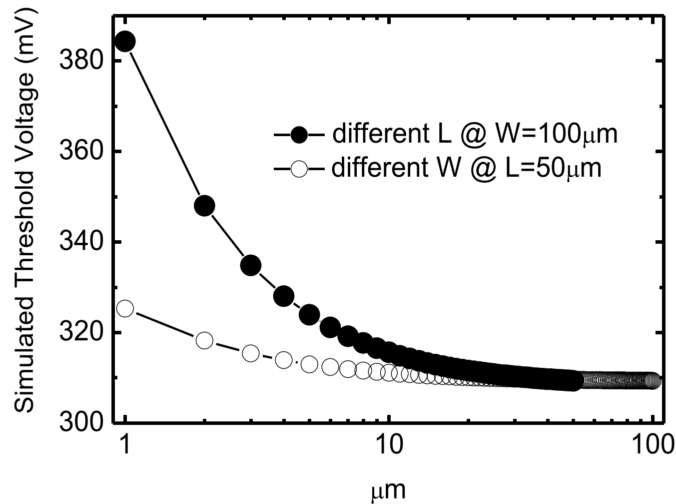


Figure 2.17: Dependence of the threshold voltage with respect to transistor dimensions (ALBANO et al., 2015).

From Fig 2.17 and using L_1=25µm and L_1=2 µm, the authors obtained a ΔV_{TH} of ~39 mV, which means that V_{REF} will be around 18 mV. It is important to note that in SEOK et al. (2012) the output voltage was stated to be around 0.75ΔV_{TH}. In the case of ALBANO et al. (2015), due to the fact that M_2 operates in triode, the $2 + nB$ (of (2.23)) term lowers even more the output voltage for a given ΔV_{TH}. Which might become a problem if the obtained ΔV_{TH} is too small.

The circuit was designed in a 0.18-µm process, and 60 samples from two runs were measured. The total occupied silicon area is about 1200 µm^2. The mean voltage reference at 25 ^{o}C is 17.69 mV. Due to its low output reference value, the circuit starts to operate at a minimum supply voltage of 150 mV. The average measured TC is 1462.4 across 0 to 120 ^{o}C temperature range. For V_{DD} from 0.15 to 1.8 V the circuit presented an LS of

2.03 %/V, indicating that by using M_2 operating in triode can worsen V_{REF} supply voltage dependence. It consumes just 26.1 pW at room temperature and minimum supply voltage. With its 150 mV operation, this work has the lowest minimum supply voltage presented in the literature.

2.2.6 Resistorless Bulk-Driven Voltage Reference

In ZHU; HU; WANG (2016) a voltage reference based on a bulk-driven technique was proposed. The simplified scheme of the presented circuit is shown in Fig. 2.18. The three transistors that compose the circuit operate in subthreshold to reduce power consumption. M_1 and M_2 form the self-cascode MOSFET, and M_3 defines the bulk voltage of M_1.

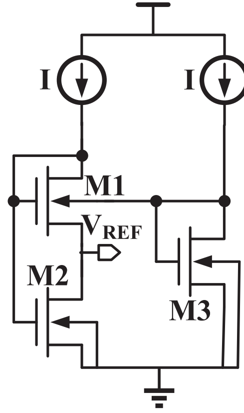


Figure 2.18: Simplified scheme of the voltage reference proposed in ZHU; HU; WANG (2016).

Considering that M_3 is saturated, its gate-to-source voltage will be given by

$$V_{GS,M_3} = V_{th,M_3} + nV_T \ln\left[\frac{I}{\mu C_{OX}(n-1)(W/L)_{M_3}V_T^2}\right] \tag{2.24}$$

The dependence of V_{th} with respect to source-to-bulk voltage (V_{SB}) is defined as

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right) \tag{2.25}$$

where V_{th0} is the threshold voltage with zero body bias, γ is the body effect constant, Φ_F the Fermi potential and V_{SB} the source-to-bulk voltage of a MOSFET.

The voltage reference is defined as $V_{REF} = V_{GS,M_2} - V_{GS,M_1}$. By considering threshold voltage variation including the effect of M_3, the voltage reference can be expressed as

$$V_{REF} = \gamma\left(\sqrt{2\Phi_F} - \sqrt{2\Phi_F + V_{REF} - V_{GS,M_3}}\right) + nV_T \ln\left(\frac{K_1}{K_2}\right) \tag{2.26}$$

In summary, the proposed structure uses an additional branch (M_3) to reduce the V_{th} of M_1, this way the SCM provides at its output voltage that is approximately the ΔV_{th} between transistors M_1 and M_2. But as shown by (2.24), V_{GS,M_3} is dependent on the bias current I, and so the bias current V_{DD} dependence will have direct impact on V_{REF} supply voltage variation. Therefore, the PSR of V_{REF} will be mainly determined by the variation of I with respect with V_{DD}.

To achieve a high PSR and low line sensitivity reference voltage without any amplifiers or adding cascode transistors, the authors proposed the circuit presented in Fig. 2.19.

The circuit architecture consists of: a start-up circuit, an I_N current generator, an I_P current generator, a current subtraction output stage and a current subtraction body bias circuit. To implement I_N and I_P current sources, the authors proposed a resistorless bulk-driven current reference, where by applying a voltage to the triode operated transistors (M_5 and M_{15} in Fig. 2.19)) the minimum supply voltage of operation can be reduced. But still, both I_N and I_P generator are very dependent on V_{DD} variations. To not transfer this dependence to V_{REF} and consequently worsen the PSR, a current subtraction stage is used to make V_{REF} almost independent on supply voltage variations.

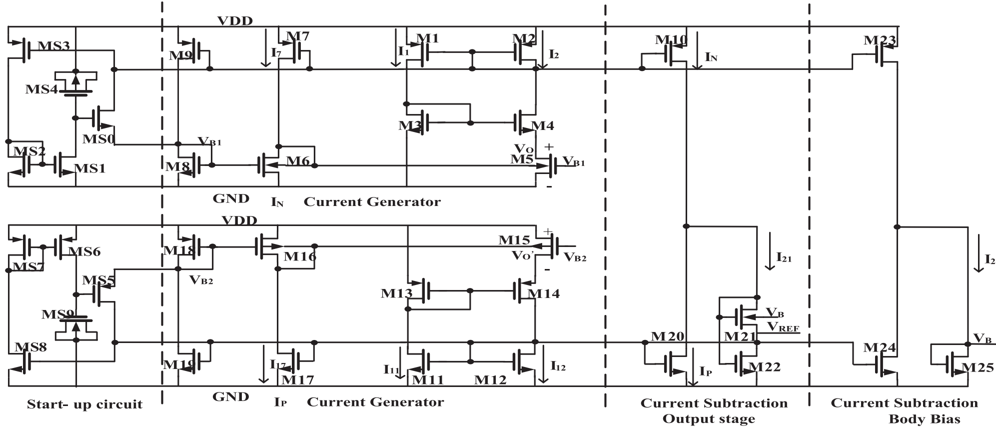


Figure 2.19: Core of the voltage reference proposed by ZHU; HU; WANG (2016).

The circuit was implemented in a standard 0.18-µm 1.8 V CMOS process. The occupied silicon is 0.0132 mm^2. Measurement results for 50 samples showed an average TC of 24.6 ppm/°C without trimming, while this value increases to 59.4 ppm/°C after trimming in the temperature range between -40 to 85 °C. An average V_{REF} of 118.4 mV is obtained. Through the proposed trimming circuit, the spread (σ/μ) of V_{REF} can be reduced from 4.5 % to 0.58 %. The circuit starts to operate at a minimum supply voltage of 0.45 V. From 0.45 to 1.8 V the average LS is 0.033 %/V. The power dissipation of the circuit is 15.6 nW at 0.45 V power supply and room temperature.

2.2.7 PMOS-Only Trim-Free Voltage Reference

The process sensitivity of V_{th} based voltage references is expected to be larger than other approaches due to distinct doping process. Therefore, post-fabrication trimming is required to attenuate such variation. This leads to a more occupied area and a time consuming task that is the trimming of each sample. In DONG et al. (2016) a PMOS-only voltage reference was proposed. By using only PMOS transistors, the circuit is less sensitive to process variations. Its simplified schematics is shown by Fig. 2.20. M_1 is an equivalent of a forward-biased diode and provides its leakage to bias the PMOS diode M_2.

The current I_R, which is equal to the current of M_1 and M_2 is given by

$$I_R = \mu_p C_{OX} \frac{W_1}{L_1} n V_T^2 \exp\left(\frac{0 - V_{th1}}{mV_T}\right) = \mu_p C_{OX} \frac{W_2}{L_2} n V_T^2 \exp\left(\frac{0 - V_{REF} - V_{th2}}{mV_T}\right) \quad (2.27)$$

M_3 and M_4 are used to generate the required body-voltage for M_1. M_4 also forms a

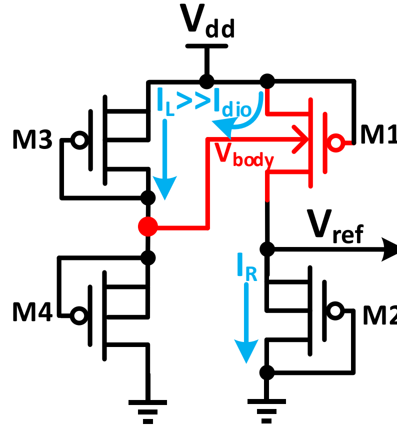


Figure 2.20: Simplified circuit of the proposed voltage reference (DONG et al., 2016).

forward-biased diode, while M_3 is a diode equivalent. The current I_L can be expressed as

$$I_L = \mu_p C_{OX} \frac{W_3}{L_3} n V_T^2 \exp\left(\frac{V_{body} - V_{DD} - V_{th3}}{mV_T}\right) = \mu_p C_{OX} \frac{W_4}{L_4} n V_T^2 \exp\left(\frac{0 - V_{th4}}{mV_T}\right) \quad (2.28)$$

Meaning that the combination of M_3 and M_4 provides a body-voltage that tracks V_{DD} as it increases, thus making the V_{BS} voltage of M_1 constant as V_{DD} increases. The V_{DD} tracking is shown in Fig. 2.21. Through the dependence of V_{th} with V_{SB} presented in (2.25), (2.27) and (2.28) expressions, the voltage reference is given by

$$V_{REF} = \gamma\left(\sqrt{2\Phi_F - mV_T \ln\left(\frac{W_4 L_3}{W_3 L_4}\right)} - \sqrt{2\Phi_F}\right) + mV_T \ln\left(\frac{W_1 L_2}{W_2 L_1}\right) \quad (2.29)$$

Since the all four transistors are the same type of PMOS, their V_{th} difference comes only from body effect, leading to a reference voltage ideally independent of V_{th} process variations. As mentioned by the authors, mismatch variability can be neglect by upsizing all devices that compose the proposed circuit.

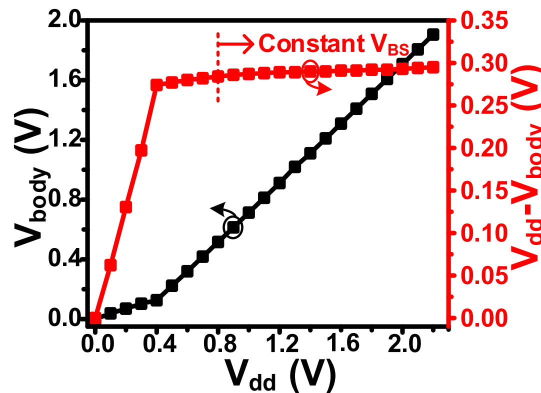


Figure 2.21: Body-voltage tracking as supply voltage increases (DONG et al., 2016).

Measurement results for 60 samples from 3 different runs in a 0.18-µm CMOS process were presented. Temperature coefficients from 48-104 ppm/°C, 55-124 ppm/°C and 56.1-117 ppm/°C were obtained for the typical, fast and slow wafers, respectively. Without any

trimming, the mean value of the voltage reference was 986.2 mV with a standard deviation of 2.6 mV, representing a 0.26 % variation. Considering all three runs, the coefficient of variation is 1.9 %. It presented an LS of 0.38 %/V from 1.2-2.2 V power supply. At room temperature and minimum supply voltage, an 114 pW power consumption was achieved. The voltage reference proposed in this work occupies an area of 0.0048 mm^2.

2.2.8 Nanopower Constant Inversion Level Voltage Reference

In Figure 2.22(a), a simple way to obtain a voltage reference is shown. In this case, as was already shown in VITA; IANNACCONE (2007), an NMOS active load is biased by a current generator with some definite temperature dependence. By adjusting the TC of I_{BIAS} at a point where mobility and threshold voltage temperature dependence are mutually compensated, also known as zero-temperature coefficient (ZTC) point (FILANOVSKY; ALLAM, 2001), a temperature stable V_{REF} can be obtained. We could also say that to obtain such V_{REF} the NMOS active load has to be biased with a constant inversion coefficient across temperature.

Recently, a voltage reference based on this concept was proposed in LUONG et al. (2017). The majority of prior voltage references based on the ZTC generate their bias current by using resistor-based solutions. This leads to an increase in power consumption or occupied area. To avoid this, the authors proposed the usage of a resistorless current reference (CAMACHO-GALEANO; GALUP-MONTORO; SCHNEIDER, 2005). The schematic of this current source is shown in Fig. 2.22(b), which is a specific current (I_{SQ}) extractor. This circuit is a resistorless version of the beta-multiplier current source, where the resistor is replaced by the SCM (M_3-M_4) operating in triode.

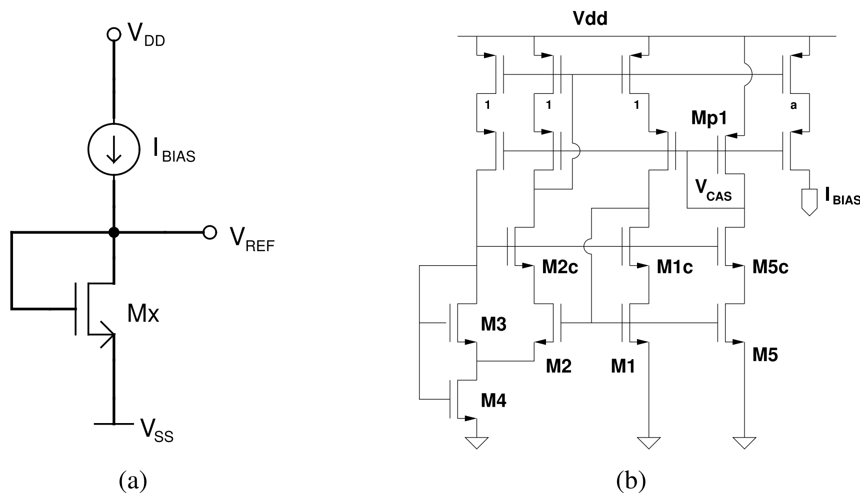
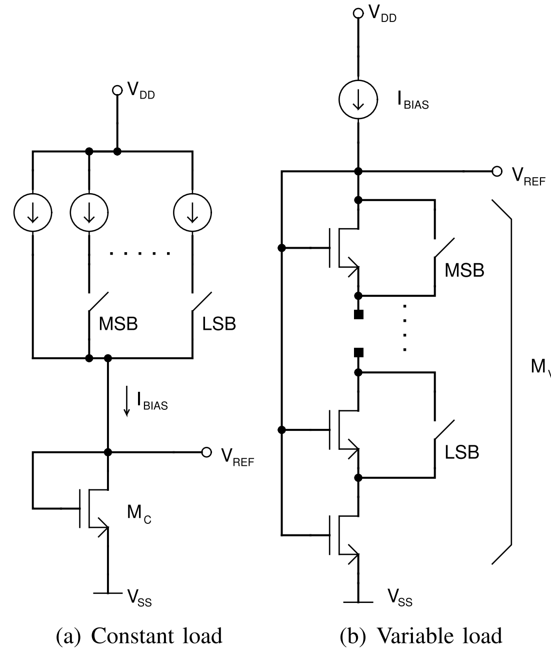


Figure 2.22: Typical MOSFET-based voltage reference (a) and the current source used in LUONG et al. (2017) to implement such voltage reference (b).

To compensate for fabrication TC variations, the authors also presented two types of trimming schemes: using a constant load and trimming the bias current, or the opposite. The simplified schematic of these schemes is presented in Fig. 2.23. A well-defined trimming design methodology based on the inversion coefficient and trimming method were also presented.

The authors presented measurement results of 5 samples from a single batch of a standard 0.35-μm CMOS process. An average V_{REF} of 710 mV was obtained for both



(a) Constant load (b) Variable load

Figure 2.23: Simplified trimming schemes (LUONG et al., 2017).

constant and variable load versions. After TC trimming, in the -20 to 80 ^{o}C temperature range these circuits presented average TCs of 26 and 21 ppm/^{o}C, respectively. The total occupied areas of the constant and variable load were 0.054 and 0.068 mm^2, respectively. Even though the proposed circuits provide a good resistorless solution to provide a reference voltage for mature technologies, its voltage reference spread is still too large ($\sim \sigma/\mu = 12.3$ %) for a single batch.

2.2.9 Subthreshold Voltage Reference with Scalable Output Voltage

The aforementioned subthreshold works discussed so far mainly provide sub-bandgap (<1.2 V) reference voltages, which might limit the operation of analog building blocks related to large supply voltages. An ultra-low power scalable subthreshold voltage reference capable of providing a reference voltage around 1.2 V while consuming tens of pW was proposed by LEE; SYLVESTER; BLAAUW (2017).

The schematic of the circuit proposed in this work in shown by Fig.2.24. The higher V_{REF} compared to the subthreshold circuits discussed in this thesis is the result of stacking four diode-connected PMOS transistors. Meaning that the output voltage is scalable depending on the number of PMOS transistor stacked. In the schematic, transistor M$_{NX}$ are zero-V_{th} used as a current source for the PMOS transistors, M$_{CX}$ are digital switches for trimming process, and M$_{PX}$ compose the PMOS stacked transistors.

The same current flow through M$_{NX}$ and M$_{PX}$:

$$\begin{aligned} I &= \mu_1 C_{OX1}\frac{W_1}{L_1}(m_1-1)V_T^2\exp\left(\frac{-V_{REF}/N - V_{th1}}{m_1 V_T}\right) \\ &= \mu_2 C_{OX2}\frac{W_2}{L_2}(m_2-1)V_T^2\exp\left(\frac{V_{REF}/N - |V_{th2}|}{m_2 V_T}\right) \end{aligned} \tag{2.30}$$

where N is the number of stacked PMOS transistors M$_{PX}$, W_1 is the sum of the channel

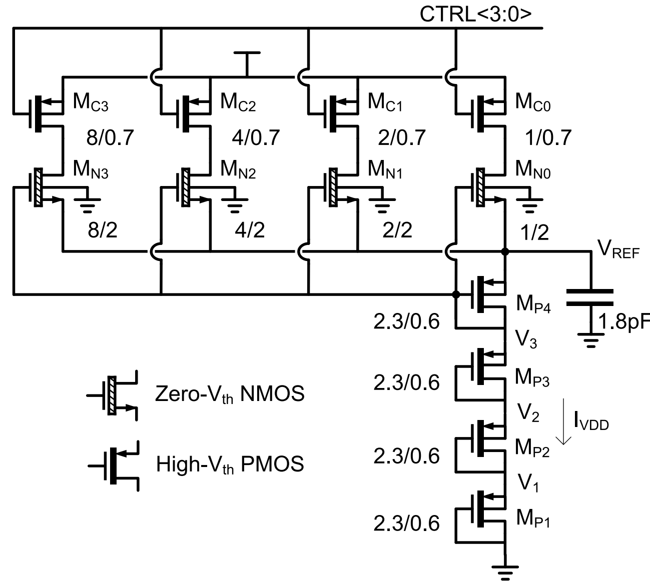


Figure 2.24: Circuit diagram of the voltage reference proposed in LEE; SYLVESTER; BLAAUW (2017).

width of all M_{NX} and L_1 their channel length. W_2 and L_2 are M_{PX} size. Therefore, V_{REF} can be obtained as:

$$V_{REF} = N\left\{\left(\frac{m_1|V_{th2}|-m_2V_{th1}}{m_1+m_2}\right)+\left(\frac{m_1m_2V_T}{m_1+m_2}\right)\ln\left(\frac{\mu_1 C_{OX1}\frac{W_1}{L_1}(m_1-1)}{\mu_2 C_{OX2}\frac{W_2}{L_2}(m_2-1)}\right)\right\} \tag{2.31}$$

As usual, the optimal ratio between M_{NX} and M_{PX} size is obtained by setting $\partial V_{REF}/\partial T = 0$, which gives

$$\left(\frac{W_1/L_1}{W_2/L_2}\right)_{\text{optimal}} = \frac{\mu_2 C_{OX2}(m_2-1)}{\mu_2 C_{OX2}(m_2-1)}\exp\left(\frac{q}{k}\left(\frac{1}{m_1}\cdot\frac{\partial V_{th1}}{\partial T}-\frac{1}{m_2}\cdot\frac{\partial V_{th2}}{\partial T}\right)\right) \tag{2.32}$$

The voltage reference is designed taking into account the trade-off between the current flowing through the parasitic diodes formed by the n-well and p-sub of PMOS transistors, and diode sizes. This is because the ratio of current that flows through these parasitic diodes can be larger than $I_{V_{DD}}$, which results in TC degradation. From the simulation, the circuit can provide a reference voltage between 0.32 to 2.11 V with around 0.3 V step, depending on the number of stacked PMOS transistors, while maintaining TC less than 20 ppm/^{o}C.

The proposed circuit was fabricated using a 0.18-µm CMOS process. Sixth samples from 3 different runs were measured. The voltage references showed an average TC of 22.5 ppm/^{o}C and 3σ inaccuracy of $\pm$2.47% from 0 ^{o}C to 100 ^{o}C. After one-point room temperature trimming the 3σ inaccuracy can be reduced by 2.5$\times$. The circuit can operate from 1.4-3.6 V power supply while presenting LS of 0.31 %/V. The average reference voltage is 1.25 V while it consumes 35 pW at room temperature and 1.4 V supply.

2.3 Performance Summary of the State-of-The-Art

The performances of the reference generators discussed in this thesis are summarized in Table 2.1. Throughout the years these circuits were proposed to provide solutions aiming the ever increasing demand of battery-operated and self-sustained applications.

From Table 2.1 one can see that the constraints of low power and low voltage of such applications can be satisfied. This comes from the fact that solutions operating at sub-0.5 V supply voltages while at pW power consumption range were already developed. When the TC, power and occupied area of these solutions are compared, circuits based on the leakage current (SEOK et al., 2012; ALBANO et al., 2015; DONG et al., 2016; LEE; SYLVESTER; BLAAUW, 2017) presents better performance, as shown through FoM results. Sub-100 mV reference generators can lead to power and area efficient voltage-to-current converters and temperature sensors. But since leakage based voltage references are mainly based on a threshold voltage difference that drops across a diode connected MOS transistor, their capacity to provide such low output voltage is, at a certain point, limited, due to minimum voltage required for the device to be saturated. Additionally, by using transistors with different threshold voltages leads to increase the output voltage process sensitivity. From these circuits the only exception is (ALBANO et al., 2015), where it provides a sub-kT/q VR. But its circuit degrades LS and very low output voltage limits its application range.

Different than the leakage based solutions, the circuits presented in VITA; IANNACCONE (2007); YAN; LI; LIU (2009); MAGNELLI et al. (2011); ZHU; HU; WANG (2016); LUONG et al. (2017) are based in a current reference generator and a voltage reference core, which leads to a larger occupied area and power consumption. In this thesis, we refer to theses circuits as non-self-biased (Non-SB), i. e., an additional active current source is needed to generate the output voltage. Although presenting these drawbacks, Non-SB solutions are still needed when a current generator is necessary to bias subsequent blocks. Thus, this kind of solution is still largely used.

Table 2.1: Summary of Recent Published Low Power CMOS Voltage References

Specification	[1]	[2]	[3]	[4][a]	[5]	[6]	[7][a]	[8][a]	[9][a]
Technology (µm)	0.35	0.35	0.18	0.13	0.18	0.18	0.18	0.35	0.18
V_{DD} (V)	0.9-4	1.1-4	0.45-2	0.5-3	0.15-1.8	1.2-2.2	0.45-1.8	0.9-3	1.4-3.6
V_{REF} (mV)	670	96.6	263.5	176	17.69	986.2	118.41	713	1.25
Temp. Range (^{o}C)	0-80	-20-80	0-120	-20-80	0-120	-40-85	-40-85	-20-80	0-100
TC (ppm/^{o}C)	10	11.4	142	29	1462	124	59.4	26	31
LS (%/V)	0.27	0.09	0.44	0.036	2.03	0.38	0.033	0.3	0.31
PSR@100Hz (dB)	-47	-60	-45	-51	-64	-42	-50.3	-	-41
Power (pW)	36,000	22,000	2,600	29.5	26.1	114	15,600	2,900	35
Area (mm^2)	0.045	0.0189	0.045	0.0093	0.0012	0.0048	0.0132	0.054	0.0025
FoM[b] (^{o}C^3/W$\times$mm^2)	0.0004	0.002	0.0007	1.25	0.315	0.23	0.0013	0.0025	3.7

[a]After trimming; [b]$\times 10^{21}$;
[1] VITA; IANNACCONE (2007); [2] YAN; LI; LIU (2009); [3] MAGNELLI et al. (2011);
[4] SEOK et al. (2012); [5] ALBANO et al. (2015); [6] DONG et al. (2016);
[7] ZHU; HU; WANG (2016); [8] LUONG et al. (2017); [9] LEE; SYLVESTER; BLAAUW (2017);

Therefore, by exploring the circuits presented in the literature, the next chapter presents voltage reference solutions to improve the design of both Non-SB and leakage based so-

lutions. Where the focus of these designs are sub-1 V operation and sub-nW power consumption.

3 PROPOSED CMOS VOLTAGE REFERENCES

Based on the study of the state-of-the-art previously discussed, this chapter aims to present novel ultra-low voltage and ultra-low power voltage references. The proposed circuits are mainly based on the threshold voltage (V_T) differences of 1.8 and 3.3 V MOSFETs and also by exploiting the V_T dependence with the device dimensions W and L. Detailed design methodologies for the proposed circuits are presented.

3.1 Unified Current-Control Model

Since the circuits under study are based on subthreshold MOSFET operation aiming for low power consumption, a transistor model appropriate for weak inversion region must be used. According to the Unified Current Control Model (UICM) (SCHNEIDER; GALUP-MONTORO, 2010), the drain current of a MOSFET can be described as the superposition of a forward (I_F) and a reverse (I_R) current components

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{3.1}$$

where $I_S = I_{SQ}S$, S is the transistor aspect ratio W/L and W and L are the channel width and length, respectively. The inversion coefficients i_f and i_r are the forward and reverse normalized currents; $I_{SQ} = \mu C'_{ox} n \frac{\phi_t^2}{2}$ is the sheet normalization current, which is process related, μ represents the carrier mobility, n the subthreshold slope factor, C'_{ox} is the gate capacitance per unit area, and $\phi_t = kT/q$ the thermal voltage. The relationship between the normalized currents and voltages is given by

$$\frac{V_G - V_T - nV_{S(D)}}{n\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{3.2}$$

where V_G, V_S and V_D are the gate, source and drain voltages referenced to the bulk terminal, and V_T is the threshold voltage.

From expressions (3.1) and (3.2), the drain current of a large channel NMOS transistor operating in WI ($i_f \ll 1$) is given by

$$I_D = 2eI_S \exp\left(\frac{V_G - V_T}{n\phi_t}\right)\left[\exp\left(\frac{-V_S}{\phi_t}\right) - \exp\left(\frac{-V_D}{\phi_t}\right)\right] \tag{3.3}$$

in which, for $V_D \geq 3 \sim 4\phi_t$ the drain current becomes almost independent of the drain voltage expressed inside the brackets in (3.3).

3.2 Self-Biased Voltage References

From the previously presented state-of-the-art study, we can note that for the low power voltage references proposed so far are biased by an additional current reference, or by the leakage current of a device. For the first case the usage of an additional current reference can limit the minimum supply voltage and also increase the power consumption. While the voltage references for the second case provide a good alternative to significantly reduce the power consumption (nW to pW), they do not provide a good solution when it comes to simultaneously bias subsequent blocks through NMOS and PMOS current mirrors. Therefore, in this section self-biasing schemes are explored in order to reduce the power consumption of the voltage reference core while having a proper control of the generated current.

3.2.1 Operation Principle

The simplified circuit schematics of the proposed voltage references are shown Fig 3.1. In both cases, the SCM is composed by transistors with different threshold voltages: M_2 is a high-V_T transistor (3.3 V) and M_3 is the standard one (1.8 V). The presented threshold values are related to the target process used for prototyping.

3.2.1.1 Self-Biased Self-Cascode Voltage Reference

As Fig. 3.1(a) shows, V_{REF1} is generated through the SCM. The SCM, in turn, is biased by two current branches that allows independent control of the inversion coefficient of M_2 and M_3. The generation of a voltage reference through the SCM is a good choice for low power since it can operate at very low current levels.

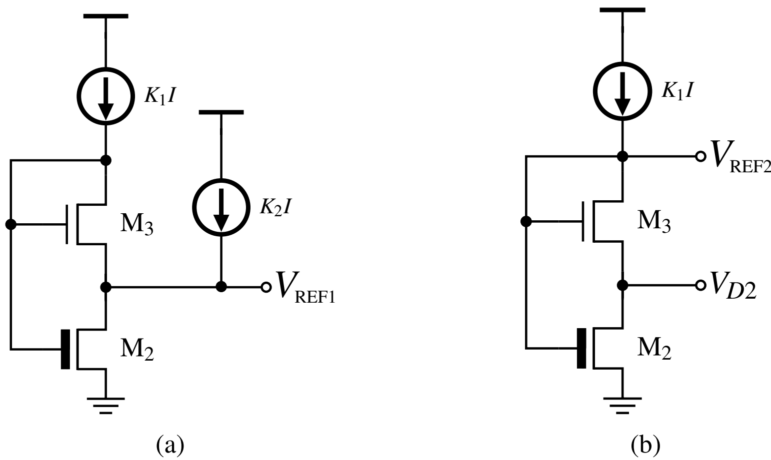


Figure 3.1: Simplified scheme of the proposed voltage references.

Usually, the bottom transistor of the self-cascode (M_2) is considered to be in triode. However, since the value of $V_{\text{REF1}}(V_{D2})$ is expected to be much greater than $4\phi_t$, M_2 is considered to be saturated in both cases of Fig. 3.1. The drain currents in Fig. 3.1(a) can be estimated through (3.1)-(3.2). Supposing that M_2 and M_3 are saturated ($i_{r2,3} = 0$), both operate in WI ($i_{f2,3} \ll 1$) and, with all voltages referenced to their bulk terminals, which are connected to ground, they can be written as

$$I_{D2} = 2eI_{S2}\exp\left(\frac{V_{G2} - V_{T2}}{n_2\phi_t}\right) \tag{3.4}$$

$$I_{D3} = 2eI_{S3}\exp\left(\frac{V_{G3} - V_{T3}}{n_3\phi_t} - \frac{V_{REF1}}{\phi_t}\right) \tag{3.5}$$

Since $I_{D2} = (K_1 + K_2)I$, $I_{D3} = K_1 I$ and $V_{G2} = V_{G3}$, the voltage reference of Fig. 3.1(a) is given by

$$V_{REF1} = \frac{V_{T2} - V_{T3}}{n_3} + \frac{\phi_t}{n_3}\ln\left(\frac{I_{S3}^{n_3}(K_1 + K_2)^{n_2}}{I_{S2}^{n_2}K_1^{n_3}}\right) + \frac{n_2 - n_3}{n_3}\phi_t \ln\left(\frac{I}{2e}\right) \tag{3.6}$$

Therefore, the SCM of Fig. 3.1(a) provides an output voltage reference that is mainly defined by the difference between the threshold voltages of the 3.3 V and 1.8 V transistors. The second component is PTAT and depends on geometric and process parameters only. Additionally, it can also be seen that a last PTAT component is added which depends on the bias current (I) and results from the difference of subthreshold slope factors (n) of transistors with different threshold voltages.

For the SCM to operate with the lowest current as possible, the bias current I is derived from the SCM output voltage itself through a feed-back path. Hence, this circuit version is called a self-biased self-cascode MOSFET (SBSCM) voltage reference.

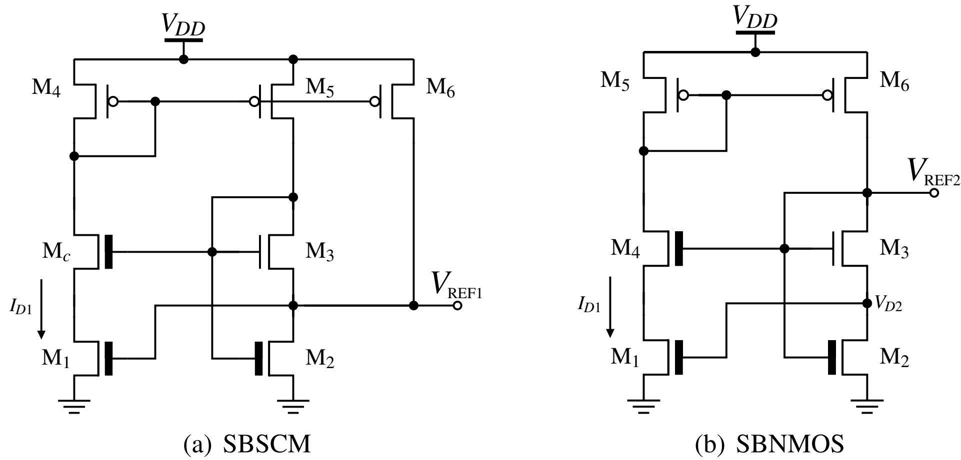


Figure 3.2: Schematic of the proposed self-biased voltage references.

The schematic of the proposed SBSCM voltage reference is shown in Fig. 3.2(a) where M_2 and M_3 compose the SCM, and M_1 defines the reference current I_{D1}. The SBSCM uses a high-V_T (3.3 V) transistor for M_1 since the target is low bias current. The PMOS transistors form the current mirror and define the current ratios $K_1 = S_5/S_4$ and $K_2 = S_6/S_4$. Additionally, paths K_1 and K_2 provide an alternative way for a trimming scheme to compensate TC for fabrication variations, as it will be presented in the next sections. The M_c transistor implements a cascode current source that can be used to improve the line sensitivity (LS) at the cost of increasing the minimum supply voltage, making its usage dependent on the target performance. In the fabricated version of the SBSCM the core generated current is simply the drain current of M_1 without the use of M_c.

The core generated current of the proposed circuit is simply the drain current of M_1

$$I_{D1} = 2eI_{S1}\exp\left(\frac{V_{REF1} - V_{T1}}{n_1\phi_t}\right) \tag{3.7}$$

By replacing (3.7) in (3.37), and defining $\varepsilon = 1 - \frac{n_2 - n_3}{n_1 n_3}$, the SBSCM generated voltage reference is now given by

$$V_{\mathrm{REF1}} = \frac{V_{T2} - V_{T3}}{n_3 \varepsilon} + \frac{\phi_t}{n_3 \varepsilon} \ln \left(\frac{(K_1 + K_2)^{n_2} I_{S3}^{n_3} I_{S1}^{n_2 - n_3}}{I_{S2}^{n_2} K_1^{n_3}} \right) + \left(\frac{n_3 - n_2}{n_1 n_3 \varepsilon} \right) V_{T1} \quad (3.8)$$

The threshold voltage has a approximately linear negative dependence on temperature that can be expressed as (TSIVIDIS, 1987)

$$V_T(T) = V_T(T_0) - \alpha_{V_T}(T - T_0) \quad (3.9)$$

where $V_T(T_0)$ is the threshold voltage at room temperature and α_T is the first derivative of the threshold voltage with respect to temperature.

Replacing (3.9) in (3.8) and setting $\frac{\partial V_{\mathrm{REF1}}}{\partial T} = 0$, the optimal ratio between S_3 and S_2 of M_3 and M_2, respectively, can be expressed as

$$\left(\frac{S_3^{n_3}}{S_2^{n_2}} \right)_{\mathrm{OPT}} = \frac{K_1^{n_3} I_{SQ2}^{n_2}}{I_{SQ3}^{n_3} (K_1 + K_2)^{n_2} I_{S1}^{n_2 - n_3}} \times \exp \left[\frac{q}{k} \left(\frac{n_1(\alpha_{V_{T2}} - \alpha_{V_{T3}}) - (n_2 - n_3)\alpha_{V_{T1}}}{n_1} \right) \right] \quad (3.10)$$

From expressions (3.8)-(3.10) the temperature compensated voltage reference is given by

$$\begin{aligned} V_{\mathrm{REF1}} = {} & \frac{V_{T2}(T_0) - V_{T3}(T_0)}{n_3 \varepsilon} + \left(\frac{n_3 - n_2}{n_1 n_3 \varepsilon} \right) V_{T1}(T_0) \\ & + T_0 \left(\frac{n_1(\alpha_{V_{T2}} - \alpha_{V_{T3}}) - (n_2 - n_3)\alpha_{V_{T1}}}{n_1 n_3 \varepsilon} \right) \end{aligned} \quad (3.11)$$

As shown by (3.11) the proposed SBSCM provides at its output a reference that is mainly defined by the difference between threshold of the 3.3 V and the 1.8 V transistors, since the α_T term is negligible at room temperature.

3.2.1.2 Self-Biased NMOS Load Voltage Reference - SBNMOS

With the expression of the SBSCM in hands, the analysis of the SBNMOS output (V_{REF2}) can be simplified. As Fig. 3.1(b) shows, the NMOS load voltage V_{REF2} is simply voltage V_{G2}, which is

$$V_{\mathrm{REF2}} = V_{T2} + n_2 \phi_t \ln \left(\frac{K_1 I_1}{2 e I_{S2}} \right) \quad (3.12)$$

The temperature behavior of (3.12) can be compensated since its first term is CTAT and its second, PTAT.

Fig. 3.2(b) presents the complete circuit where the NMOS load is the SCM composed transistor (M_2 and M_3) biased in WI. Besides, M_1 defines the bias current, M_4 acts as a cascode to shield M_1 from supply voltage variations, and transistors M_5 and M_6 act as a current mirror thus defining $K_1 = S_6/S_5$. The necessity of using the cascode transistor M_4 lies on the fact that the LS of V_{REF2} is directly dependent on the LS of the current source.

From the circuit of Fig. 3.2(b), through expressions (3.4)-(3.12), considering $V_{D2} = V_{\mathrm{REF1}}$ with $K_2 = 0$, and knowing that $I_{D2} = K_1 I_{D1}$, $V_{G2} = V_{G3} = V_{\mathrm{REF2}}$, $\beta = \frac{n_2}{n_1 n_3}$ and $\gamma = n_2 + \beta(n_2 - n_3)$, the provided output voltage is given by

$$V_{\text{REF2}} = V_{T2}(\beta+1) - \beta(V_{T3} + n_3\varepsilon V_{T1}) + \phi_t \ln\left(\frac{K_1^{\gamma} I_{S1}^{\gamma} I_{S3}^{\frac{n_2}{n_1}}}{I_{S2}^{n_2(\beta+1)}}\right) \quad (3.13)$$

Considering the linear approximation of V_T presented by (3.9) and replacing it into (3.13), and again setting $\frac{\partial V_{\text{REF2}}}{\partial T} = 0$, the optimal S_2 ratio for temperature compensation can be expressed by

$$S_{2\text{OPT}} = \frac{(K_1 I_{S1})^{\frac{\gamma}{n_2(\beta+1)}} I_{S3}^{\frac{1}{n_1(\beta+1)}}}{I_{SQ2}} \times \exp\left(\frac{q}{k}\left[\frac{\alpha_{V_{T2}}(\beta+1) - \beta(\alpha_{V_{T3}} + n_3\varepsilon\alpha_{V_{T1}})}{n_2(\beta+1)}\right]\right)^{-1} \quad (3.14)$$

Thus, by satisfying (3.14) and neglecting the α_{V_T} terms at room temperature, the temperature compensated V_{REF2} is now expressed as

$$V_{\text{REF2}} = V_{T2}(T_0)(\beta+1) - \beta\left[V_{T3}(T_0) + n_3 V_{T1}(T_0)\right] \quad (3.15)$$

Since the generated current (I_{D1}) also depends on M_2, the output reference voltage is expected to depend more than once on its threshold voltage V_{T2}, as represented in the first term of (3.15). Thus, the proposed circuit provides a reference voltage that depends on threshold voltages of M_1, M_2 and M_3, being V_{T2} the major contributor.

It is important to notice that, for expressions (3.10) and (3.14), if $\mu_1 \approx \mu_2 \approx \mu_3 \approx \mu$ is considered, temperature dependent terms $\left(\mu\frac{\phi_t^2}{2}\right)$ of the specific currents (I_{SQ}) cancel each other. For this reason, the I_{SQ} temperature dependency is not considered in this analysis.

3.2.2 Design Considerations

3.2.2.1 Current Consumption Minimization

As depicted in Fig. 3.2(a) the total current consumed by the SBSCM circuit is given by

$$I_{\text{DD1}} = I_{D1}(1 + K_1 + K_2) \quad (3.16)$$

Since ratios S_3 and S_2 set a fixed temperature compensated reference voltage and its value is applied to the gate of M_1, the generated current will be defined only by ratio S_1. Therefore, the current consumption can be minimized by setting S_1 to the smallest possible ratio ($W_{\text{MIN}}/L_{\text{MAX}}$), at the cost of temperature coefficient degradation, and also by reducing K_1 and K_2 current gains. To further reduce I_{D1} the third branch can be eliminated ($K_2 = 0$) and thus temperature compensation can be made by increasing S_3/S_2. In this case, the trade-off between power consumption and $M_{2,3}$ area will depend on the threshold voltage temperature slope (α_T).

The total current consumption of the SBNMOS circuit (Fig. 3.2(b)) is simply (3.16) with $K_2 = 0$. It is straightforward that the reduction of the bias current I_{D1} depends on the reduction of both S_1 and V_{D2}, which can be reduced by increasing S_2 while reducing S_3. Yet this strategy is not practical since the S_2 ratio for optimal temperature compensation defined by (3.14) implies that S_2 must also be reduced for a $S_{1,3}$ reduction. So for a small S_1 ratio, S_3 ratio must increase to reduce the current consumption while keeping a reasonable temperature coefficient.

3.2.2.2 Minimum Supply Voltage

Proper operation of the proposed circuits under the assumptions made in the previous sections requires the definition of a minimum supply voltage. This value is set to the minimum voltage needed to make both circuits as independent as possible to V_{DD} variations. In order to satisfy this condition, the saturation of the MOSFETs must be guaranteed. A MOS transistor is said to be saturated in subthreshold operation when its drain-to-source voltage is greater than 3 to 4 times the thermal voltage, i.e., $V_{DS} \geq 3 \sim 4\phi_t$. Hence, in SBSCM without M_c, we have

$$V_{DD1\text{MIN}} = \max\{\overbrace{V_{DS5} + V_{DS3} + V_{\text{REF1}}}^{8\phi_t\,+\,250\text{ mV}}, \overbrace{V_{DS6} + V_{\text{REF1}}}^{4\phi_t\,+\,250\text{ mV}}\} \tag{3.17}$$

Considering that the drain-to-source voltage (V_{DS}) of all transistors must be at least $4\phi_t$ and that from (3.8) the roughly expected voltage reference value is around 250 mV, the resulting minimum supply voltage will be around 450 mV according to (3.17). This value could be further reduced if using devices with closer V_T value, thus reducing V_{REF1}.

From (3.13), the expected value for the SBNMOS voltage reference is around 390 mV. Approaching the issue as previously, the minimum supply voltage of the SBNMOS would simply be $V_{\text{REF2}} + 4\phi_t$. From measurement results, the observed minimum supply voltage was 0.6 V (Section 4.2.1). This is because V_{REF2} depends directly on the minimum supply voltage of I_{D1}. Therefore, the minimum supply voltage for the SBNMOS will have an additional of $4\phi_t$ from that expected by only considering the voltage drop paths.

3.2.2.3 Sensitivity to Supply Voltage Variations

The optimization of the LS lies on the minimization of ΔV_{REF}. Therefore, for both circuits of Fig. 3.2 this can be done by reducing currents gains K_1 and K_2 (the last one only for the SBSCM).

The line sensitivity of SBSCM can be substantially reduced (around 10× or more) by adding the transistor M_c at the cost of increasing the minimum supply voltage from 0.45 V to 0.6 V. M_c acts as a cascode device with an output impedance much larger than that of M_1. Accordingly, M_c shields M_1 from supply voltage variations thus improving the LS. The simulation results of the TC sensitivity with respect to V_{DD} for the SBSCM with and without M_c are shown in Fig. 3.3. Typical simulations of the SBSCM without M_c present a TC of 7 ppm/°C at minimum supply voltage (0.45 V) while the maximum TC is less than 70 ppm/°C at 3.3 V. The addition of M_c results in a TC lower than 10 ppm/°C for all voltage supply range at the cost of increasing the minimum V_{DD} to 0.6 V.

The channel length modulation was neglected in circuit design since this effect is not relevant for MOS transistors operating in subthreshold, where drain output impedance depends mainly on drain-induced barrier lowering effect (DIBL). DIBL is significantly reduced by increasing the channel length so the high impedance transistors (SBSCM: M_1, M_5 and M_6; SBNMOS: M_1, M_4 and M_6) were designed with large L in order to minimize the LS of the proposed circuits.

3.2.2.4 Sizing for Optimal Temperature Compensation

Fig. 3.4 represents the simulated TC as function of transistor ratios for both SBSCM and SBNMOS. Simulation was performed by proper sizing all other transistors besides M_2 and varying its W/L ratio.

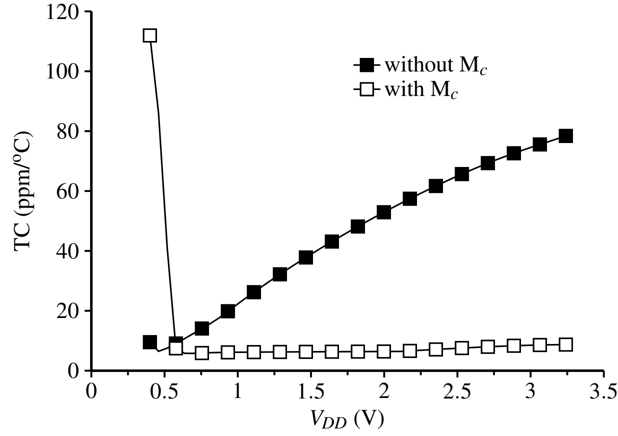


Figure 3.3: Comparison of the TC supply voltage dependence with and without M_c transistor.

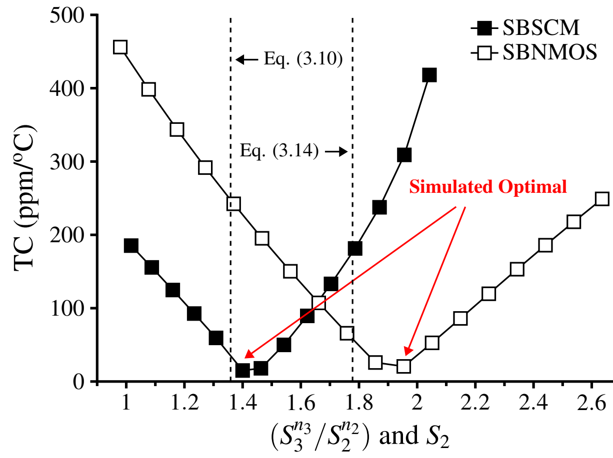


Figure 3.4: Transistor sizing for optimal TC.

The calculated optimum ratios of (S_3^{n3}/S_2^{n2}) (for SBSCM) and S_2 (for SBNMOS) are 1.34 and 1.78 respectively, as predicted by (3.10) and (3.14). As can be seen in Fig. 3.4 the simulated optimal ratios of the same parameters are 1.4 and 1.92 respectively. The proximity between calculated and simulated values validates the proposed approach. Taking into account the previous considerations as well as layout regularity, the proposed circuits were sized as presented in Table 3.1.

Table 3.1: Transistor sizes for SBSCM and SBNMOS.

Transistor	**Sizes (μm/μm)**	
	SBSCM	**SBNMOS**
M_1	1/10	4×4/10
M_2	2×8/10	2×9.6/10
M_3	2×11/10	4/2
M_4	2×6/10	2×4/10
M_5	2×6/10	2×5/10
M_6	4×6/10	2×5/10

3.3 3-Transistor Voltage Reference

So far the majority of subthreshold voltage references presented in the literature, and also the previously proposed circuits, presented solutions mainly based on the usage of transistors with different threshold voltages. Distinct V_T devices have different fabrication processes, their V_T process sensitivity related to one another is large. Thus, this also increases the sensitivity of the generated voltage reference to process variations. To attenuate this problem, in this section we explore the dependence of V_T with the transistor dimensions on obtaining distinct V_T using devices of the same type. These phenomena are also known as reverse short-channel (RSC) and narrow-width (NW) effects.

3.3.1 V_T Dependence on Device Dimensions

In traditional CMOS technologies, short-channel effect (SCE) is a phenomenon where there is a V_T roll-off as the channel length of a transistor is reduced. This causes an increase of the drain-induced barrier lowering (DIBL) and consequently reducing the output impedance of the device. Since in more advanced technologies this effect may be critical, for NMOS transistors, highly doped p^+ regions, also known as HALO implants, are added at the drain and source boundaries to compensate their non-uniformity,. This reduces the depletion layer at these regions and thus reducing the control of the drain (source) over the channel. However, a counter effect of adding the HALO implants is a V_T roll-up as the channel length decreases (LU; SUNG, 1989). This phenomena is known as the reverse short-channel effect (RSCE).

Figure 3.5(a) presents RSCE for three different nodes and shows how the effect increases as the technology scales (KIM et al., 2007). The RSCE can be explained as illustrated in Fig. 3.5(b). The channel doping is non-uniform: highly doped at drain/source regions and lightly doped at center. This means that for smaller channel lengths the average channel doping is higher, resulting in a V_T increase. As the distance between the HALO implants increases, by consequence of increasing the channel length, surface doping level across the channel is reduced, and therefore reducing the threshold voltage (KIM et al., 2007).

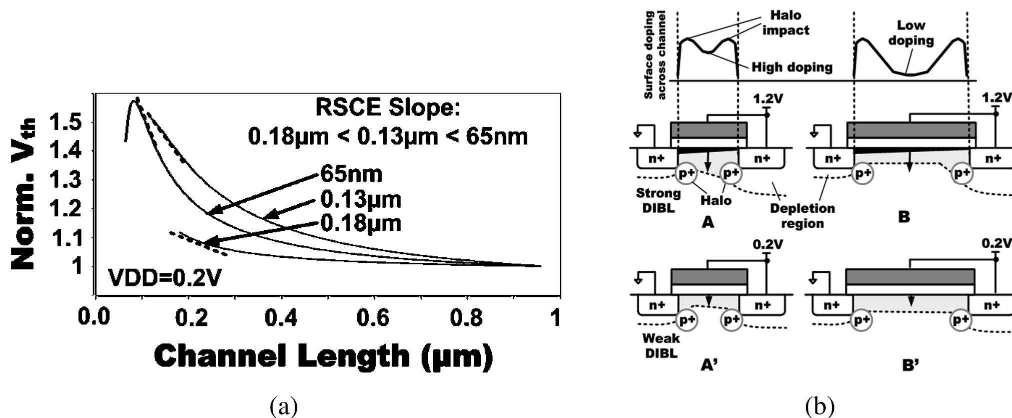


Figure 3.5: (a) V_T dependence with respect to the channel length and (b) surface doping across the channel to illustrate the RSCE (KIM et al., 2007).

Additionally, these technologies also present V_T dependence with respect to width variation. This effect is mainly defined by the transistor isolation used in the process (LOCOS or STI). For LOCOS isolation the same V_T roll-up as the channel width decreases

appears, known as the narrow-channel effect (NWE) (WANG, 1978). This happens because for narrower channels the fringing fields cause gate-induced depletion region to spread outside the channel. Meaning that there is more charge at the body depletion region, thus translating into a V_T increase for a channel width decrease. The STI presents the inverse effect, and there is a V_T roll-up as the channel width increases, also known as the inverse narrow-width effect (INWE) (AKERS, 1986). The INWE happens due to the high electric fields created at corners of STI, which leads to the formation of inversion charges.

3.3.2 Circuit Description

The voltage reference schematic is presented in Fig. 3.6(a). The proposed circuit is formed by the self-cascode MOSFET (SCM) M_1-M_2 biased by a current source I_{LOAD}, the reference voltage V_{REF} is obtained from the difference between the gate-to-source voltages of the SCM structure.

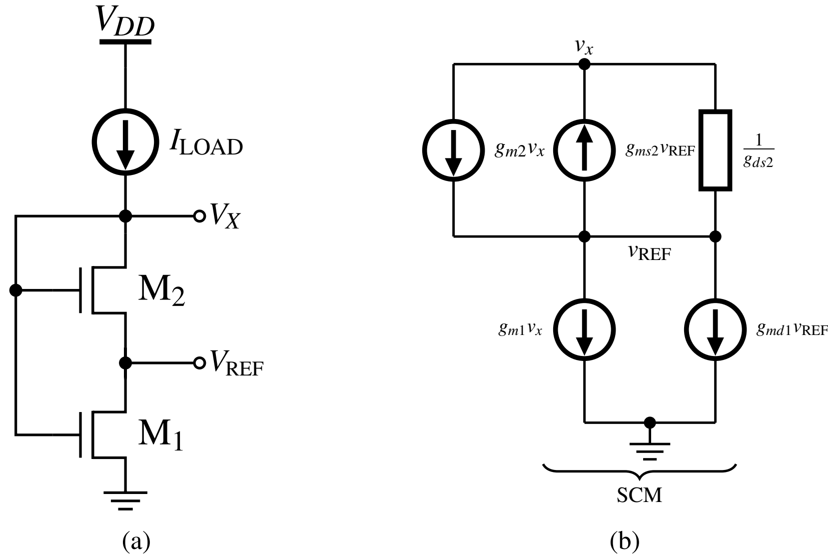


Figure 3.6: (a) Simplified circuit of the voltage reference; (b) Equivalent circuit of the self-cascode MOSFET (SCM) M_1-M_2.

Knowing that for the SCM transistor M_1 can be in triode, while M_2 must be saturated, by applying (3.3) for both transistors (M_1 and M_2) we have

$$I_{D1} = 2eI_{S1}\left[\exp\left(\frac{V_X - V_{T1}}{n_1\phi_t}\right) - \exp\left(\frac{V_X - V_{T1} - n_1V_{\text{REF}}}{n_1\phi_t}\right)\right] \tag{3.18}$$

$$I_{D2} = I_{S2}\exp\left(\frac{V_X - V_{T2} - n_2V_{\text{REF}}}{n_2\phi_t}\right) \tag{3.19}$$

From Fig. 3.6 we have $I_{D1} = I_{D2}$, and since we are using the same type of transistors $n_1 = n_2$ can be assumed. Thus, a general expression for V_{REF} can be obtained as

$$V_{\text{REF}} = \phi_t \ln\left[1 + \frac{I_{S2}}{I_{S1}}\exp\left(\frac{V_{T1} - V_{T2}}{n\phi_t}\right)\right] \tag{3.20}$$

Considering that $\ln(1+x) \to \ln(x)$ for $x \gg 1$, a simplified expression for V_{REF} is obtained as

$$V_{\text{REF}} = \frac{V_{T1} - V_{T2}}{n} + \phi_t \ln\left(\frac{I_{S2}}{I_{S1}}\right) \tag{3.21}$$

By replacing the previous definition of the temperature dependence of V_T with respect to temperature given by (3.9) into (3.21), we have

$$V_{\text{REF}} = \frac{V_{T1}(T_0) - V_{T2}(T_0)}{n} + \frac{(\alpha_{V_{T2}} - \alpha_{V_{T1}})(T - T_0)}{n} + \frac{kT}{q} \ln\left(\frac{I_{SQ2}S_2}{I_{SQ1}S_1}\right) \tag{3.22}$$

By setting $\partial V_{\text{REF}}/\partial T = 0$, a value of S_2/S_1 for optimal temperature compensation can be expressed as

$$\left(\frac{S_2}{S_1}\right)_{\text{OPT}} = \frac{I_{SQ1}}{I_{SQ2}} \exp\left[\frac{q}{k}\left(\frac{\alpha_{V_{T1}} - \alpha_{V_{T2}}}{n}\right)\right] \tag{3.23}$$

From (3.23) and (3.22), and neglecting the α_{V_T} terms at room temperature, the temperature compensated V_{REF} is given by

$$V_{\text{REF}} = \frac{V_{T1}(T_0) - V_{T2}(T_0)}{n} \tag{3.24}$$

Therefore, (3.24) gives us a reference voltage equal to the difference of V_T ($V_{T1} > V_{T2}$) from the transistors of the SCM (M_1-M_2) over the subthreshold slope factor n. In order to guarantee a low temperature coefficient (TC), the variation of α_{V_T} for different V_Ts should be minimum, and S_2/S_1 is the ratio of transistors (M_1-M_2) which are limited by the maximum transistor area. This constraints will be used during the design procedure.

3.3.3 PSR Analysis and Enhancement of V_{REF}

3.3.3.1 PSR Analysis

Considering the small signal equivalent of the SCM depicted in Fig. 3.6(b), the PSR of the V_{REF} is given by

$$\text{PSR} = \frac{v_{\text{ref}}}{v_{dd}} = \frac{v_x}{v_{dd}} \cdot \frac{v_{\text{ref}}}{v_x} \tag{3.25}$$

where (3.25) represents the voltage transfer function between the supply voltage (v_{dd}) and the reference voltage (v_{ref}) is conveniently split into two transfer functions: v_x/v_{dd} and v_{ref}/v_x, which are the supply voltage contributions of the current load (I_{LOAD}) and the self-cascode MOSFET to the reference voltage.

The voltage reference becomes insensitive to supply variations when v_x/v_{dd} or in turn v_x/v_{dd} and v_{ref}/v_x are minimized. The value v_{ref}/v_x is calculated using the equivalent of Fig. 3.6(b), yielding

$$\frac{v_{\text{ref}}}{v_x} = \frac{g_{m2} - g_{m1} + g_{ds2}}{g_{ms2} + g_{ds2} + g_{md1}} \approx \frac{g_{m2} - g_{m1}}{g_{ms2}} \tag{3.26}$$

where g_m, g_{ms} and g_{ds} are the gate, source transconductance and drain conductance, respectively. This expression is defined for a specific design value of the voltage reference.

Fig. 3.7 shows the circuit of I_{LOAD}, it can be implemented using a PMOS or NMOS transistor acting as a current source, in this case we are considering both transistors saturated, the circuit design will be discussed later. The value of v_x/v_{dd} is calculated from its

small-signal analysis and yields to

$$\left(\frac{v_x}{v_{dd}}\right)_{\text{PMOS}} \approx \frac{g_{ms}}{g_{ds}} \vee \left(\frac{v_x}{v_{dd}}\right)_{\text{NMOS}} \approx \frac{g_{ds}}{g_{ms}} \tag{3.27}$$

Since, $g_{ms} > g_{ds}$, v_x/v_{dd} is higher than one for a PMOS, worsening the PSR, leading us to discard this current load. On the other hand, for an NMOS is lower than one, which is desired to improve the PSR.

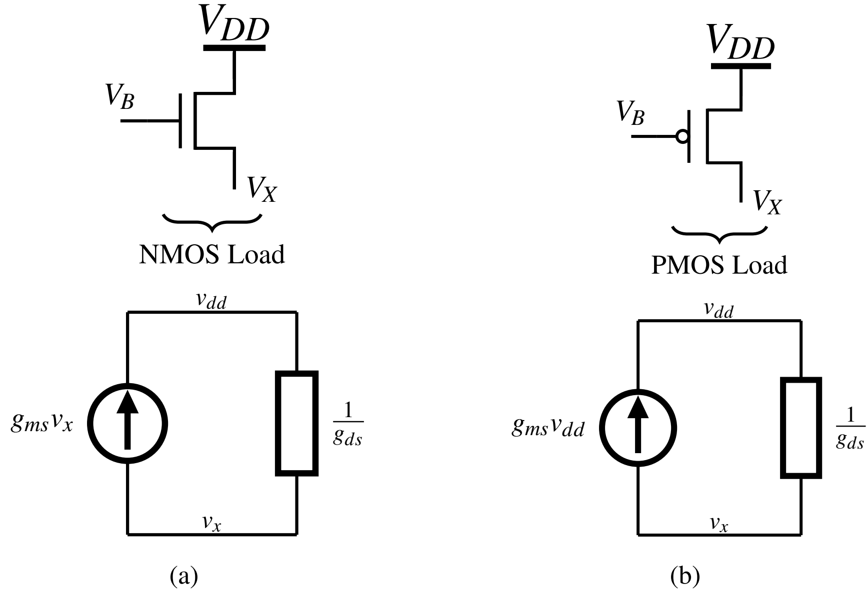


Figure 3.7: PMOS and NMOS implementation of I_{LOAD} of Fig. 3.6(a). V_B is constant bias voltage.

Taken into account that the voltage reference circuit is working in weak inversion and the gate voltage of the NMOS of Fig. 3.7 is ($V_B < V_{DD}$), we have two options for V_B:

- For the case $V_B = V_X$, v_x/v_{dd} is increased from g_{ds}/g_{ms} to g_{ds}/g_{mb}, Fig. 3.8(a).
- For the case $V_B = 0$ V, v_x/v_{dd} remains the same as (3.27), Fig. 3.8(b).

From the two previous cases, $V_B = 0$ V is chosen for presenting the lowest v_x/v_{dd} to guarantee the highest PSR. Therefore, the SCM is biased with the leakage current of the I_{LOAD}, resulting in an NMOS with a large or small area depending on its current density (I_D/W). Since I_{LOAD} only acts as a current source, its design is constrained to obtain the bias current of the SCM for the lowest achievable area. Fig. 3.9 shows the different current densities of the available transistors for $V_{GS} \leq 0$ V, the lower I_D/W of the standard-V_T or low power-V_T transistors will yield larger areas in contrast to the zero-V_T or low-V_T transistors. Due to this fact, the last ones will be used to design I_{LOAD} and will be covered in the following subsection.

3.3.3.2 PSR Enhancement with zero-V_T MOSFETs

Special attention has been given to the properties of the zero-V_T transistor due to its high drive capability at low voltages (GALUP-MONTORO; SCHNEIDER; MACHADO, 2012). Since $V_T \approx 0$ V, a zero-V_T transistor with a gate voltage equal to or lower than 0 V can be saturated with a small value of drain-to-source voltage, $V_{DS} \approx 100$ mV. Fig.

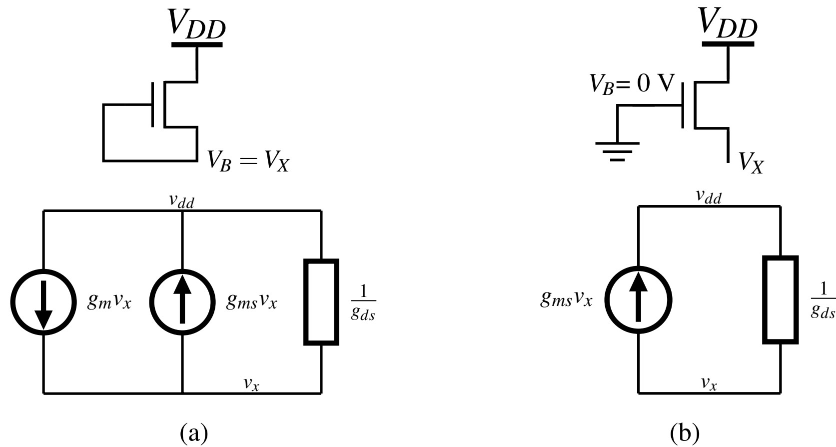


Figure 3.8: Implementations of I_{LOAD} using self-biased NMOS transistors. (a) gate-to-source load; (b) gate-to-ground load.

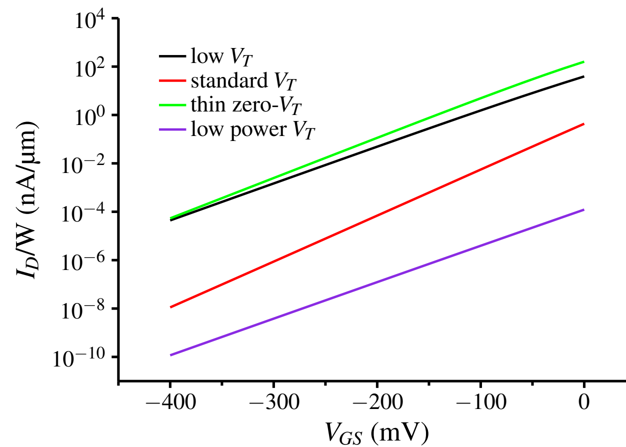


Figure 3.9: Current densities (I_D/W) for zero-V_T, low -V_T, standard-V_T and low power-V_T transistors. V_{DS} = 100 mV and W/L= 4 µm/1 µm for all transistors.

3.10 shows the simulated drain current for three different transistors (thin zero-V_T, thick zero-V_T and low-V_T). Among them the thin zero-V_T and thick zero-V_T present the highest and lowest current density, respectively.

I_{LOAD} will be designed using one of the previously mentioned transistors. Fig. 3.11 shows the I_{LOAD} implementation using one and two zero-V_T transistors.

Using the above equivalent circuit, v_x/v_{dd} is obtained for one and two zero-V_T transistors

$$\left(\frac{v_x}{v_{dd}}\right)_{\text{1-ZVT}} \approx \frac{g_{ds1}}{g_{ms1}}$$
$$\left(\frac{v_x}{v_{dd}}\right)_{\text{2-ZVT}} \approx \frac{g_{ds1}}{g_{ms1}} \cdot \frac{g_{ds2}}{g_{ms2}} \tag{3.28}$$

Through (3.28) it can be shown that by adding another transistor in series v_x/v_{dd} is reduced by a factor of g_{ms}/g_{ds}, consequently improving the overall PSR of the voltage reference. Fig. 3.12 presents v_x/v_{dd} as a function of V_{DS} for three different simulated transistors. Using just one transistor, we can obtain an attenuation of above -30 dB using

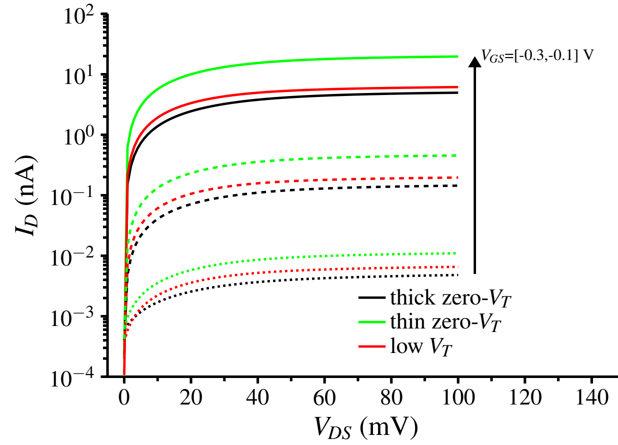


Figure 3.10: $I_D \times V_{DS}(V_B = 0\text{ V})$ characteristics of a thin zero-V_T, thick zero-V_T and low-V_T transistors. W/L= 4 μm/1 μm for all transistors.

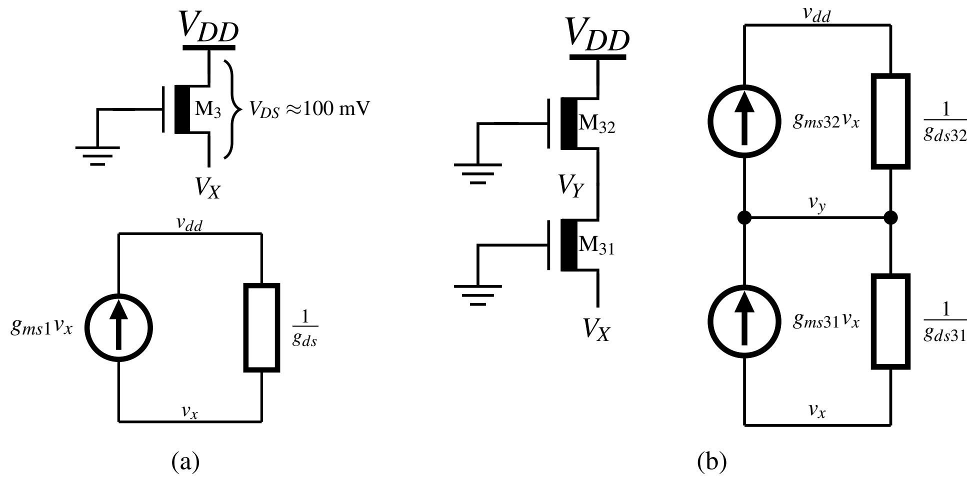


Figure 3.11: I_{LOAD} implementation with (a) One zero-V_T transistor; (b) Two zero-V_T transistors.

only 100 mV of V_{DS}. For the two transistor implementation the can go low as -60 dB, but at cost of 100 mV drop for the additional transistor.

3.3.4 Design of the SCM

The first step to design our voltage reference is to choose the transistors of the SCM. Since our goal is low power operation, we will choose from the process the two available transistors with high-V_T. The voltage reference is designed in a standard 130 nm CMOS process. Fig. 3.13 shows the normalized α_{VT} variation, where the low power V_T transistor presents the lowest variation of α_{V_T} which is desired, recalling that the second term of (3.24) should be minimized.

Fig. 3.14(a) shows the threshold voltage (V_T) variation against channel length (L) for different transistors ratios W/L, having L as the major contributor its variation. V_T is extracted through the g_m/I_D method proposed in SIEBEL; SCHNEIDER; GALUP-MONTORO (2012). Transistor M_1 is sized small (W/L between 1 to 2) to satisfy the first term of (3.24), $V_{T1} > V_{T2}$, while M_2 is sized taking in to consideration the following:

- $L_2 > L_1$, condition of the first term in (3.24).

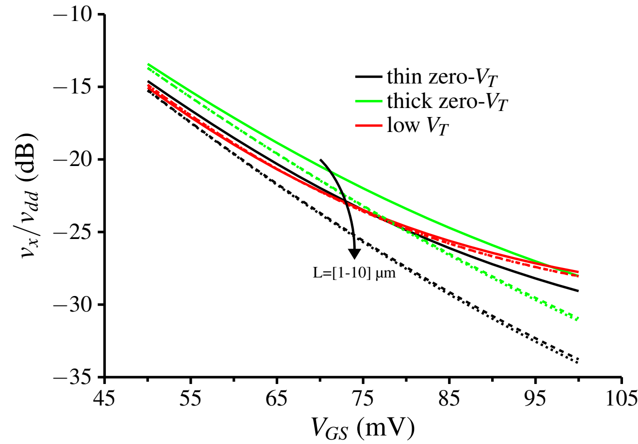


Figure 3.12: v_x/v_{dd} as function of V_{DS} for the simulated transistors. W = 4 µm for all transistors.

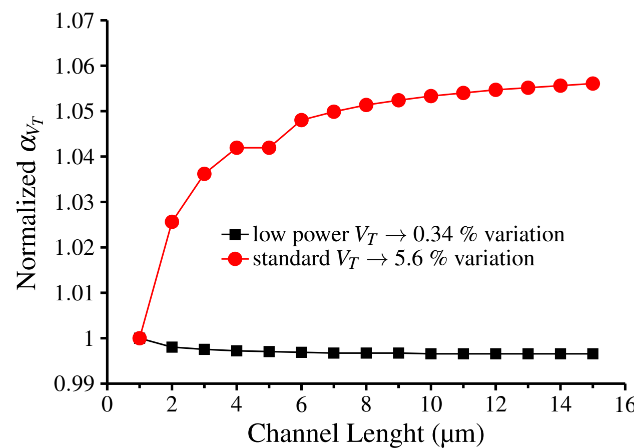


Figure 3.13: Variation of normalized α_{V_T} for different transistor channel length.

- To prevent charging damage in the polysilicon, the maximum thin oxide area for any single gate in the process is 230 µm^2.
- In order to guarantee an efficient layout area and compliant with $(W \times L)_2 \leq 230$ µm^2, a range of $[1-2]$ for $(W/L)_2$ and $L_2 = [10-15]$ µm is defined, as illustrated in Fig. 3.14(b).

From the previous considerations, the maximum value for V_{REF} is limited by the maximum area of M_2. As shown by Fig. 3.15(a), for a fixed size of M_1, the maximum value of the voltage reference is 70 mV.

Using the range defined for $(W/L)_2$ and L_2 as a starting point, the voltage references are designed to achieve the lowest possible temperature coefficient (TC) for the minimum V_X, as illustrated in Fig. 3.15(b). As previously stated, the area o M_2 is verified to satisfy the constraint of $(W \times L)_2 \leq 230$ µm^2.

The current reference (I_{LOAD}) for V_{REF} was designed with one and two series transistors for three different transistors (thin zero-V_T, thick zero-V_T and low-V_T). After several simulations, the thin zero-V_T transistor was chosen based on its capability to provide the lowest TC and PSR compared with the other transistors. Fig. 3.16 show the schematics for both implementations. Since for the conventional implementation I_{LOAD} is composed

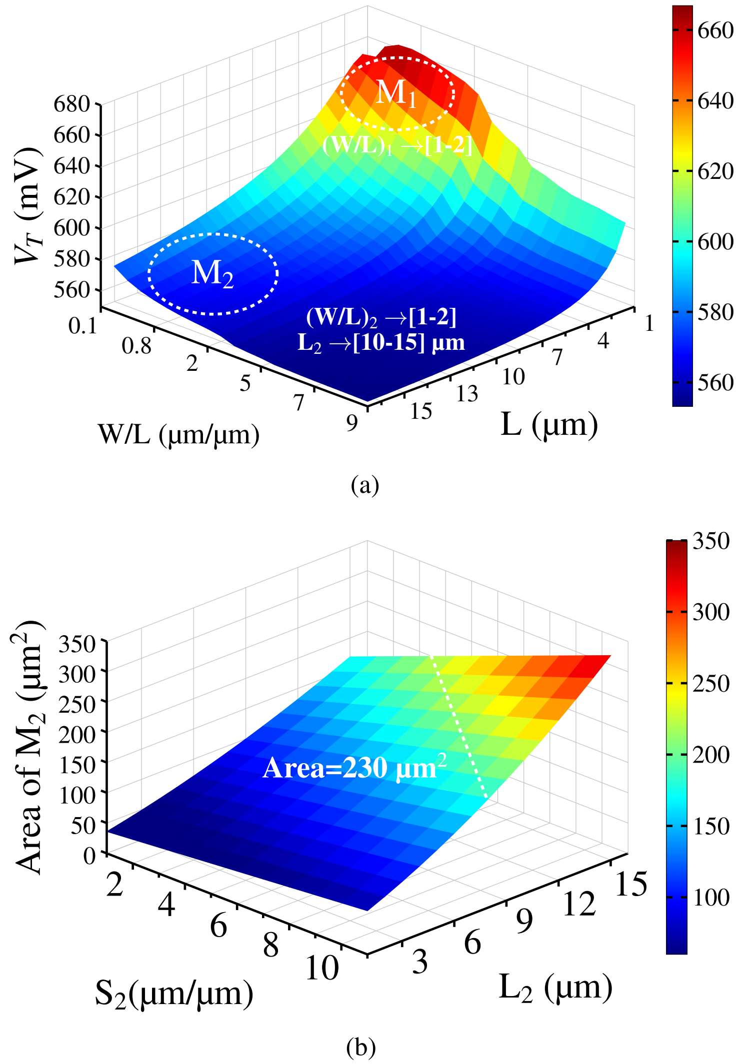


Figure 3.14: (a) V_T dependence with respect with W and L and (b) the maximum allowable area for a unit transistor M_2.

by only one zero-V_T transistor, the proposed circuit is called a 3-Transistor (3T) voltage reference. Table 3.2 shows the transistor sizing for the designed circuits. The ratio S_2/S_1 for optimal temperature compensation predicted by (3.23) is around 0.86, while the chosen after simulations is $S_2/S_1 = 0.826$. The proximity of the predicted and simulated values for temperature compensation validates the theoretical approach.

As stated before, in weak inversion the transistor is said to be saturated when $V_{DS} > 3 \sim 4\phi_t$. Thus, the minimum supply voltages for the conventional version will be given as $V_{DD\text{MIN}} = V_{DS3} + V_{DS2} + V_{\text{REF}}$, resulting in a minimum supply voltage of approximately 300 mV. For the PSR enhancement, the minimum supply voltage is increased in 100 mV to guarantee saturation for the additional series transistor in the I_{LOAD} implementation.

3.3.5 Sub-kT/q V_{REF}

The output voltage generation of the proposed 3T structure is mainly defined by the V_T difference of transistors that composed the SCM. And as previously presented, we can generate any value of voltage reference within the maximum V_T difference for a given technology. Thus allowing the generation of a voltage reference as low as the thermal

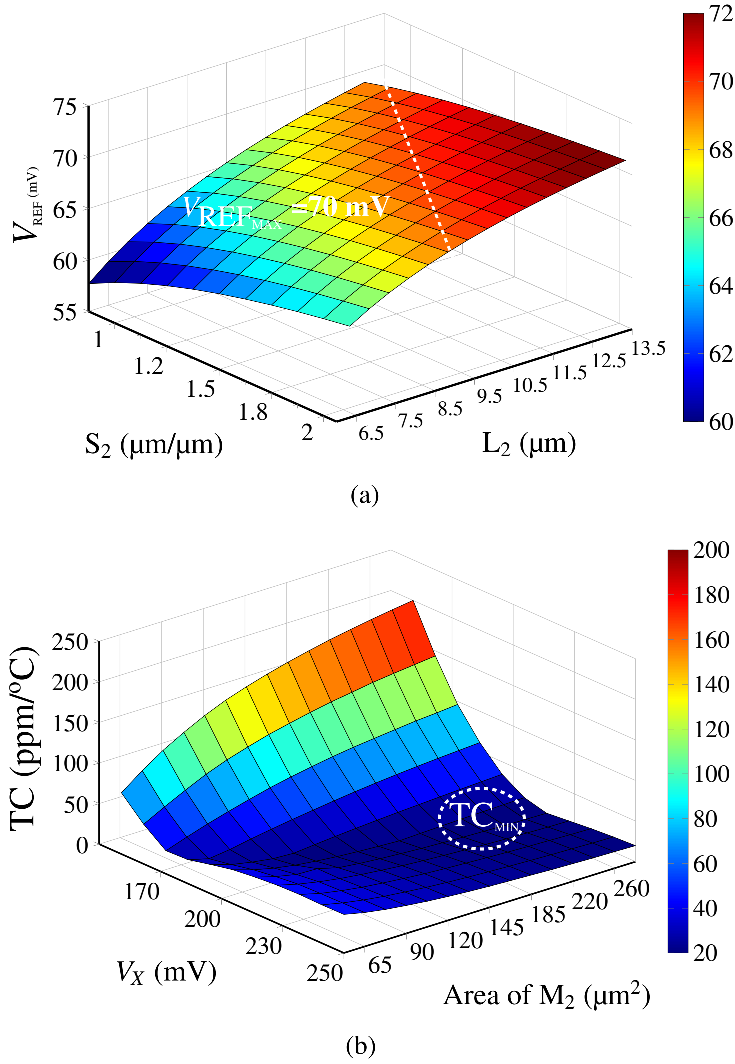


Figure 3.15: (a) V_{REF} as function of M_2 ratio (S_2) and channel length. $(\text{W/L})_1$ = 1 and n = 1.35 and (b) TC as function of V_x and M_2 area.

Table 3.2: Sizing for the conventional and PSR Enhancement versions.

(W/L)	IBM 130nm
M_1	$\frac{2\ \mu\text{m}}{1\ \mu\text{m}}$ (LP)
M_2	$\frac{19\ \mu\text{m}}{11.5\ \mu\text{m}}$ (LP)
$\text{M}_{3,31}-\text{M}_{32}$	$\left[\frac{3\ \mu\text{m}}{3.9\ \mu\text{m}} - 9\left(\frac{3\ \mu\text{m}}{3.9\ \mu\text{m}}\right)\right]$ (ZVT)

voltage, i. e., sub-kT/q. The generation of such value of voltage reference, with adequate temperature stability, can enable the development of area efficient resistor-based voltage-to-current converters, where the value of the resistor used can be reduced due to the very small voltage applied to it.

For the circuit analysis, consider the 3T circuit presented in Fig. 3.16(a). The situation where M_1 is considered to be in triode and M_2 is saturated stays the same as before. The only thing that needs to be addressed is that, for the case where V_{REF} is considered to be much less than $3 \sim 4\phi_t$, the $\ln(1+x) \rightarrow \ln(x)$ consideration done for the conventional

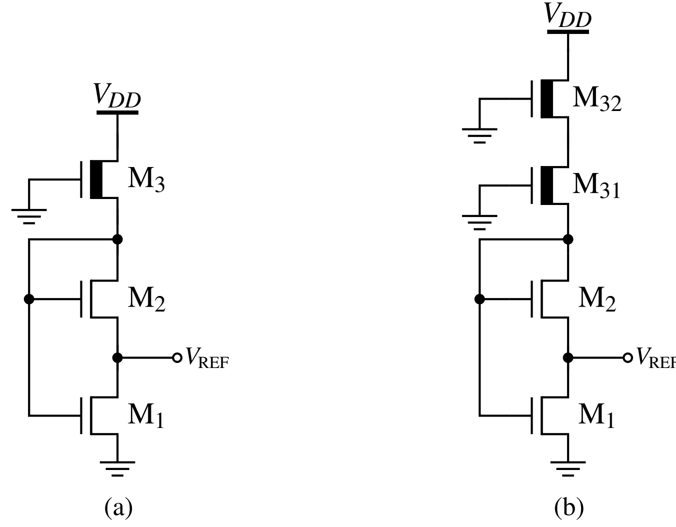


Figure 3.16: Schematics for the 3T voltage reference (a) Conventional and (b) PSR Enhancement versions

approach is no longer reliable since $x \gg 1$ is not satisfied. In this case, the generated voltage reference will be given by the expression (3.20).

The design methodology of the proposed 3T structure is based on obtaining the S_2/S_1 ratio for optimal temperature compensation. Through (3.20), it is possible to note that there is no explicit solution to obtain such ratio. Thus, rewriting it, we have

$$\ln\left(\exp\left(\frac{V_{\mathrm{REF}}}{\phi_t}\right)-1\right) = \ln\left(\frac{I_{S2}}{I_{S1}}\right) + \frac{V_{T1}-V_{T2}}{n\phi_t} \tag{3.29}$$

By making a linear approximation of the log function:

$$\ln\left(\exp\left(\frac{V_{\mathrm{REF}}}{\phi_t}\right)-1\right) \approx A + B\frac{V_{\mathrm{REF}}}{\phi_t} \tag{3.30}$$

where A and B are the fitting parameter which depends on the defined interval of V_{REF}. Since we want $V_{\mathrm{REF}} < \phi_t$, the chosen range for V_{REF} is from $\phi_t/2$ to ϕ_t. With these values the obtained fitting parameters are $A = -1.4$ and $B = 1.94$.

Replacing (3.30) in (3.29)

$$V_{\mathrm{REF}} = \frac{V_{T1}-V_{T2}}{nB} + \frac{\phi_t}{B}\ln\left(\frac{I_{S2}}{I_{S1}}\right) - \frac{A}{B}\phi_t \tag{3.31}$$

Including the temperature dependence of V_T through (3.9) in (3.31) and setting $\partial V_{\mathrm{REF}}/\partial T = 0$, the optimal value for the ratio S_2/S_1 can be obtained as

$$\left(\frac{S_2}{S_1}\right)_{\mathrm{OPT}} = \frac{I_{SQ1}}{I_{SQ2}}\exp\left[\frac{q}{k}\left(\frac{\alpha_{V_{T1}}-\alpha_{V_{T2}}}{n}\right)+A\right] \tag{3.32}$$

Through the optimal S_2/S_1 ratio, the sub-kT/q temperature compensated voltage reference can be expressed as

$$V_{\mathrm{REF}} = \frac{V_{T1}(T_0)-V_{T2}(T_0)}{nB} \tag{3.33}$$

Following the design methodology for the conventional approach, the value of V_{REF} is defined by the V_T difference between M_1 and M_2 where the upper bound is defined by V_{T1} while the lower bound of this difference is defined by V_{T2}. Meaning that any voltage reference value between the $\Delta V_{T_{\mathrm{MAX}}}$ can be obtained. Even though optimally temperature compensated, V_{REF} still presents a temperature variation of 150-200 µV due to the non-linear behavior of the compensated $\Delta\alpha_{V_T}$. This means that the same variation is expected for any voltage reference value. Therefore, one can conclude that as the generated voltage reference reduces its TC is degraded.

By following the same procedure as for the conventional approach, $S_1 = \frac{2\ \mu\mathrm{m}}{2\ \mu\mathrm{m}}$ defines the V_T upper bound. S_2 is sized considering the trade-off between TC and the output value for a fixed. The dependence of V_{REF} and TC with respect to S_2 for a fixed L_2= 15 µm, which defines the design space, is shown in Fig. 3.17. As it was done for the conventional approach, the usage of L_2 as long while L_1 is small implies in a wider voltage reference. Thus, in the case of the sub-kT/q V_{REF} the dependence of V_T with respect to the channel width will play the major role.

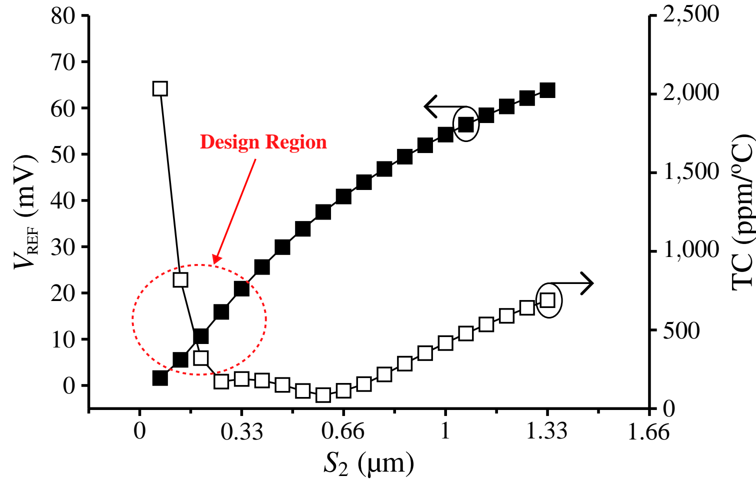


Figure 3.17: Design region for the Sub-kT/q voltage reference.

For this design, a voltage reference of less than 20 mV was set as the objective. Considering the TC and output voltage trade-off, from Fig. 3.17 we can achieve a 15.9 mV output voltage with a TC of 240 ppm/°C. The optimal temperature compensation ratio predicted by (3.32) was around 0.24, while the one obtained from simulation was 0.267.

As previously defined, the minimum supply voltage of the 3T structure is $V_{DD\mathrm{MIN}} = V_{DS3} + V_{DS2} + V_{\mathrm{REF}}$. This implies that for the sub-kT/q approach $V_{DD\mathrm{MIN}}$ equally reduces for a V_{REF} reduction with respect to the conventional approach, which would result in $V_{DD\mathrm{MIN}} \approx$220 mV. But if we consider that the PSR, and consequently LS, specifications that can be relaxed, the minimum supply voltage will be given just by the voltage drop across the SCM. Therefore, $V_{DD\mathrm{MIN}} = V_{DS2} + V_{\mathrm{REF}} \approx$120 mV. At $V_{DD\mathrm{MIN}}$ M_3 will be in deep triode which will reduce the power consumption substantially.

3.3.6 Bulk-Driven High-Order Compensation of V_{REF}

In temperature sensors, the main sources of temperature errors raise from temperature instability of the reference circuits. The previous versions of the 3T voltage reference present TCs that are greater than 30 ppm/°C. This means that these versions may not

be suitable for precision temperature sensor applications. For this reason, a bulk-driven high-orde temperature compensation scheme based on the 3T structure is proposed.

The schematics of the proposed high-order 3T voltage reference is shown in Fig. 3.18. The three transistors that compose the circuit are operating in weak inversion. Transistors M_1 and M_2 are triple-well devices (isolated bulk) and compose the SCM, and M_3 is a zero-V_T transistor which serves as current source biasing the SCM with its leakage current. High-order temperature compensation is achieved by feeding back V_X and V_{REF} voltages through the bulk terminals of M_1 and M_2.

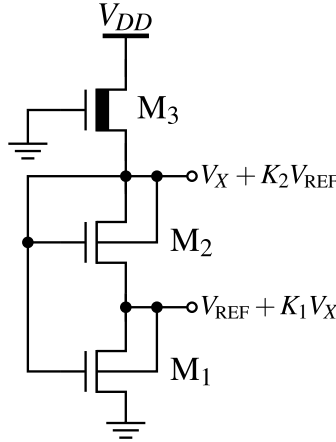


Figure 3.18: Schematic of the proposed high-order compensation scheme.

3.3.6.1 High-Order Compensation

Considering that all transistors in Fig. 3.18 operate in weak inversion ($i_f \ll 1$), are saturated ($i_r = 0$) and $V_{DS} \geq 3 \sim 4\phi_t$, their drain currents are given by

$$I_{D1} = 2eI_{S1} \exp\left(\frac{V_X - V_{T1} + V_{REF}(n_1 - 1)}{n_1\phi_t}\right) \tag{3.34}$$

$$I_{D2} = 2eI_{S2} \exp\left(\frac{n_2 V_X - V_{T2} - n_2 V_{REF}}{n_2\phi_t}\right) \tag{3.35}$$

$$I_{D3} = 2eI_{S3} \exp\left(\frac{-n_3 V_X - V_{T3}}{n_3\phi_t}\right) \tag{3.36}$$

V_{REF} is mainly defined by transistors M_1 and M_2. Since $I_{D1} = I_{D2}$ and $n_1 \approx n_2 \approx n$, V_{REF} is given by

$$V_{REF} = \frac{V_{T1} - V_{T2}}{2n - 1} + \left(\frac{n - 1}{2n - 1}\right) V_X + \frac{n}{2n - 1}\phi_t \ln\left(\frac{I_{S2}}{I_{S1}}\right) \tag{3.37}$$

Transistors M_1 and M_3 form the equivalent of a 2-Transistor voltage reference (SEOK et al., 2012), which means that the voltage V_X will be given by their gate-to-source voltage difference. Through $I_{D1} = I_{D3}$:

$$V_X = \frac{n_3 V_{T1} - n_1 V_{T3}}{n_1 n_3 + n_3} + \left(\frac{n_1 - 1}{n_1 + 1}\right) V_{REF} + \left(\frac{n_1}{n_1 + 1}\right) \phi_t \ln\left(\frac{I_{S3}}{I_{S1}}\right) \tag{3.38}$$

From (3.37) and (3.38) one can see that the high-order compensation is achieved by feeding back both V_{REF} and V_X through the bulk terminals of M_1 and M_2, making possible

to achieve high-order compensation to either V_{REF} or V_X voltages. Due their magnitude, one can conclude that V_X has more impact on V_{REF} than the opposite, i.e., $K_1 > K_2$ (Fig. 3.18). In the case of this work, the circuit is designed for the high-order compensation of V_{REF}, but the same can also be achieved for V_X.

By replacing (3.38) in (3.37), and defining $\beta = \frac{n(n+3)-2}{n+1}$, $\xi = \frac{n_3(n+1)}{n-1}$ and $\theta = \frac{n(n-1)}{n+1}$ the voltage reference is now given by

$$V_{\mathrm{REF}} = \frac{V_{T1} - V_{T2}}{\beta} + \frac{n_3 V_{T1} - n V_{T3}}{\beta\xi} + \phi_t \ln\left(\frac{I_{S2}^{\frac{n}{\beta}} I_{S3}^{\frac{\theta}{\beta}}}{I_{S1}^{\frac{n+\theta}{\beta}}}\right) \tag{3.39}$$

Thus, the proposed circuit provides at its output the weighted difference between the V_T of M_1 and M_2 transistors, as shown by the first term of (3.39). The second term of V_{REF} appears as the high-order compensation coming from V_X, where V_{REF} is compensated through the third term by adjusting S_1, S_2 and S_3 ratios. It is important to note that since in the model used the transistor terminals are referenced to the bulk, (3.39) includes the variation of V_T due to body-effect.

From expressions (3.9) and (3.39), and setting $\partial V_{\mathrm{REF}}/\partial T = 0$ the optimal ratio, still dependent on the subthreshold slope factor of the different type transistors, is given by

$$\left(\frac{S_2^{\frac{n}{\beta}}}{S_1^{\frac{n+\theta}{\beta}}}\right)_{\mathrm{OPT}} = \frac{I_{SQ1}^{\frac{n+\theta}{\beta}}}{I_{SQ2}^{\frac{n}{\beta}} I_{S3}^{\frac{\theta}{\beta}}} \exp\left[\frac{q}{k}\left(\frac{\alpha_{V_{T1}}(\xi + n_3) - \xi\alpha_{V_{T2}} - n\alpha_{V_{T3}}}{\beta\xi}\right)\right] \tag{3.40}$$

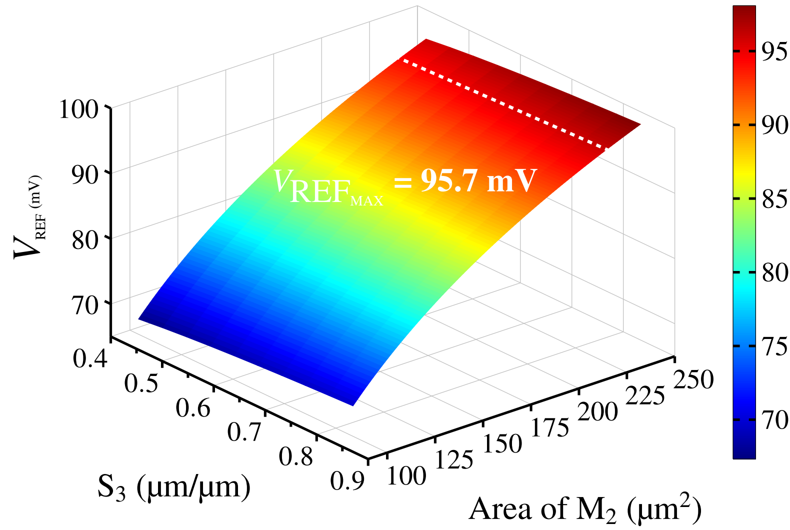
By satisfying (3.40), and neglecting α_{V_T} at room temperature, the high-order temperature-compensated voltage reference is expected to be equal to

$$V_{\mathrm{REF}} = \frac{V_{T1}(T_0) - V_{T2}(T_0)}{\beta} + \frac{n_3 V_{T1}(T_0) - n V_{T3}(T_0)}{\beta\xi} \tag{3.41}$$

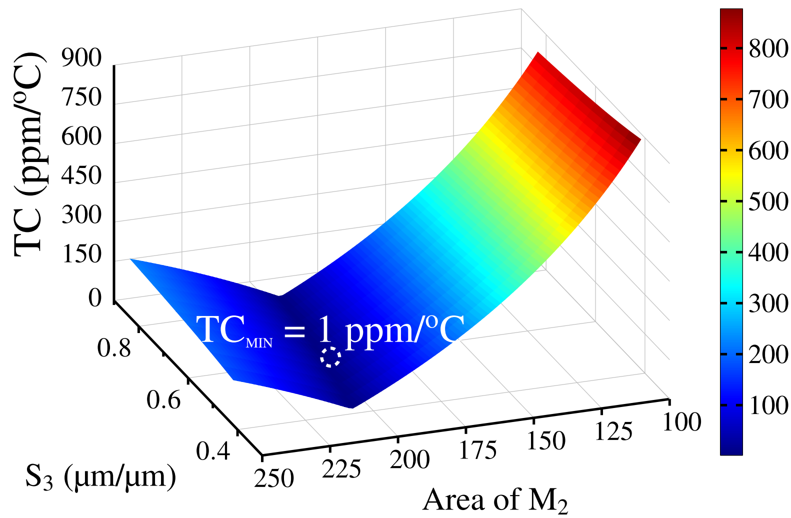
Reiterating, it is important to observe that for expressions (3.23), (3.32) and (3.40) if $\mu_1 \approx \mu_2 \approx \mu_3 \approx \mu$ is considered, the temperature dependent terms $\left(\mu\frac{\phi_t^2}{2}\right)$ of the specific currents (I_{SQ}) cancel each other. For this reason, the I_{SQ} is considered to be constant with temperature to provide an easy to extract quantity to size the transistors for optimal temperature compensation.

The maximum value of V_{REF} is limited by the maximum M_2 area as shown by Fig. 3.19(a), which results in a maximum voltage reference value of 95.7 mV. This value is used to defined the minimum supply voltage for proposed circuit. Since to guarantee saturation $V_{DS} \geq 4\phi_t$, $V_{DD_{\mathrm{MIN}}} = V_{DS3} + V_{DS2} + V_{\mathrm{REF}_{\mathrm{MAX}}}$, resulting in a minimum supply voltage of approximately 300 mV.

Through the range defined to S_2 and using L_2 as starting point, the circuit is designed to achieve the lowest TC as possible. For a fixed value of $(\mathrm{W/L})_1$=2μm/1 μm, the TC is dependent of both S_2 and S_3 ratios. From Fig. 3.14(a), V_T becomes almost independent of L for values greater than 10 μm, thus defining L_2 = 10 μm. Fig. 3.19(b) shows the TC dependence with respect to S_3 and M_2 area. In these conditions, S_2 has the major impact in the TC where the high-order compensation is achieved through the fine adjustment of S_3. As shown in Fig. 3.19(b), a minimum TC of 1 ppm/$^{\mathrm{o}}$C is achieved with S_2=2 and S_3=0.645. From (3.40) the optimal temperature compensation ratio was 0.95, while the simulated one was 0.93.



(a)



(b)

Figure 3.19: (a) V_T dependence with respect with W and L and (b) the maximum allowable area for a unit transistor M_2.

3.3.6.2 *Variability Attenuation*

From the previous considerations on the design of the SCM, one can conclude that M_1 is the major contributor to the mismatch variability of V_{REF} due its small W and L. With this in mind, the proposed bulk driven scheme also attenuates the variability caused by M_1 when compared to the conventional approach.

Suppose a positive (negative) ΔV_{T1} due to mismatch. This would also cause a positive (negative) variation of both V_{REF} and V_X voltages. But due to the magnitude and the definition of both voltages, the impact of a given ΔV_{T1} variation is much greater in V_{REF} than on V_X, i. e., $|\Delta V_{T1}| \rightarrow |\Delta V_{REF}| > |\Delta V_X|$. The dependence of V_T concerning the source-to-bulk voltage (V_{SB}) can be expressed as (SCHNEIDER; GALUP-MONTORO, 2010)

$$V_T = V_{T0} + (n-1)V_{SB} \tag{3.42}$$

where V_{T0} is the threshold voltage at zero V_{SB} voltage. This variation can also be seen

through Fig. 3.20.

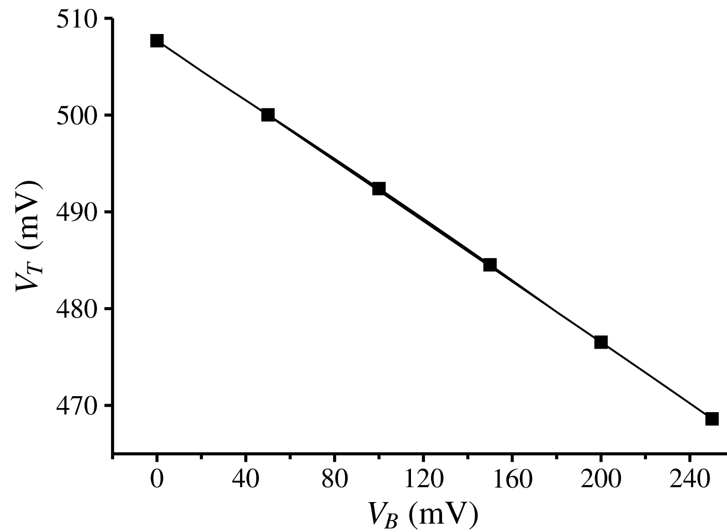


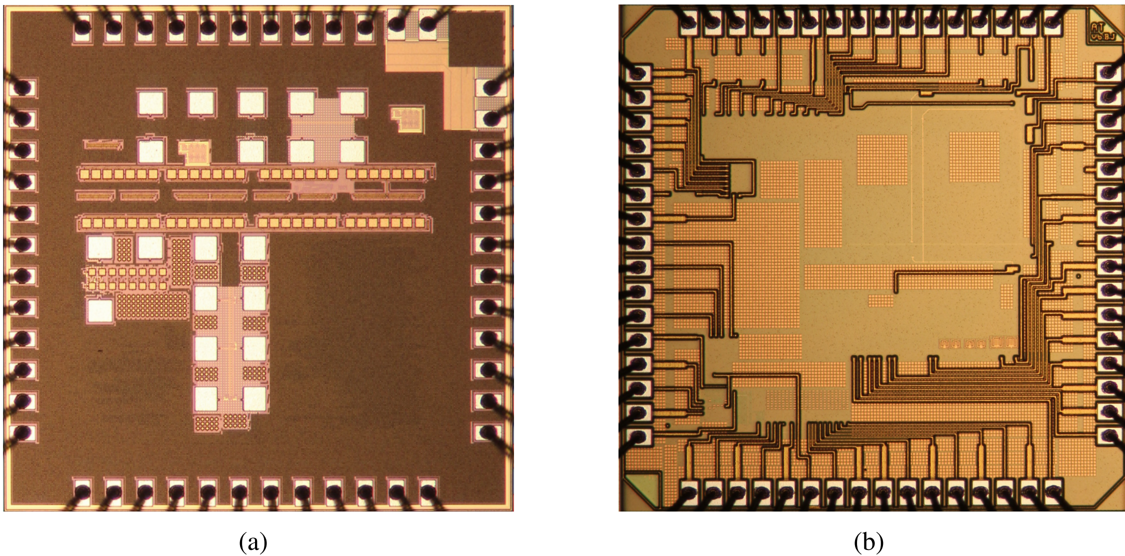
Figure 3.20: V_T dependence with respect to the bulk voltage (V_S = 0 V).

Thus, a positive (negative) ΔV_{T1} would cause a increase (decrease) on V_{SB2} voltage and consequently increasing (decreasing) V_{T2}. In summary, the proposed scheme attenuates the mismatch variability of V_{REF} by making V_{T2} slightly follow a V_{T1} variation. Therefore, reducing the variation spread of both V_{REF} and TC.

Since the proposed high-order scheme allows a V_{REF} about 30 mV larger than that provided by the conventional approach, the variability attenuation can also be interpreted as the increasing of the mean V_{REF} while using approximately the same S_1 and S_2 aspect ratios. Thus, maintaining the same mismatch spread.

4 SIMULATION AND MEASUREMENT RESULTS

This chapter presents the simulation and measurements results of the proposed pW voltage references. The self-biased voltage references were fabricated in 0.18-µm, while the 3T voltage references in 0.13-µm CMOS process. Figure 4.1 shows the photos of the fabricated chips.



(a) (b)

Figure 4.1: Photos of the (a) 0.18-µm and (b) 0.13-µm CMOS process prototypes.

4.1 Measurement Setup

The measurement results presented in this thesis were performed using a Keysight-4156 Semiconductor Parameter Analyzer for DC sweep and a Tenney Jr. thermal chamber for temperature control. The standard measurement setup can be seen in Fig. 4.2. The parameter analyzer is configured with a large integration time in order to get as many data as possible for each DC sweep. Triaxial and coaxial cables are used to connect the parameter analyzer to the test fixture, and coaxial cable from the fixture into the thermal chamber. A DC sweep from 0 - $V_{DD_{MAX}}$ were performed for each temperature point.

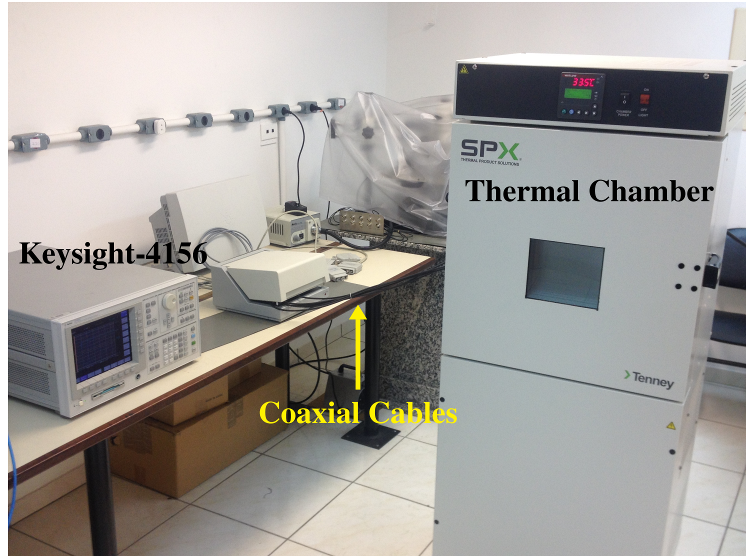


Figure 4.2: Standard measurement setup.

4.2 Self-Biased Voltage References

4.2.1 Simulation and Measurement Results

The proposed self-biased CMOS voltage references were fabricated in a standard 0.18-µm CMOS process. The chip photo and the layout of the proposed circuits are shown in Fig. 4.3. The total occupied areas are 0.0020 mm^2 and 0.0017 mm^2 for the SBSCM and SBNMOS, respectively. A total of 24 chips from the same batch were packaged in ceramic (SEBASTIANO et al., 2011) and measured.

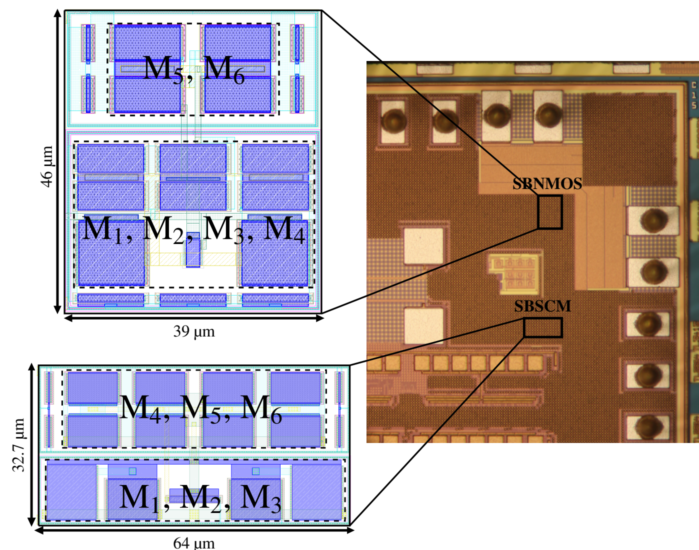
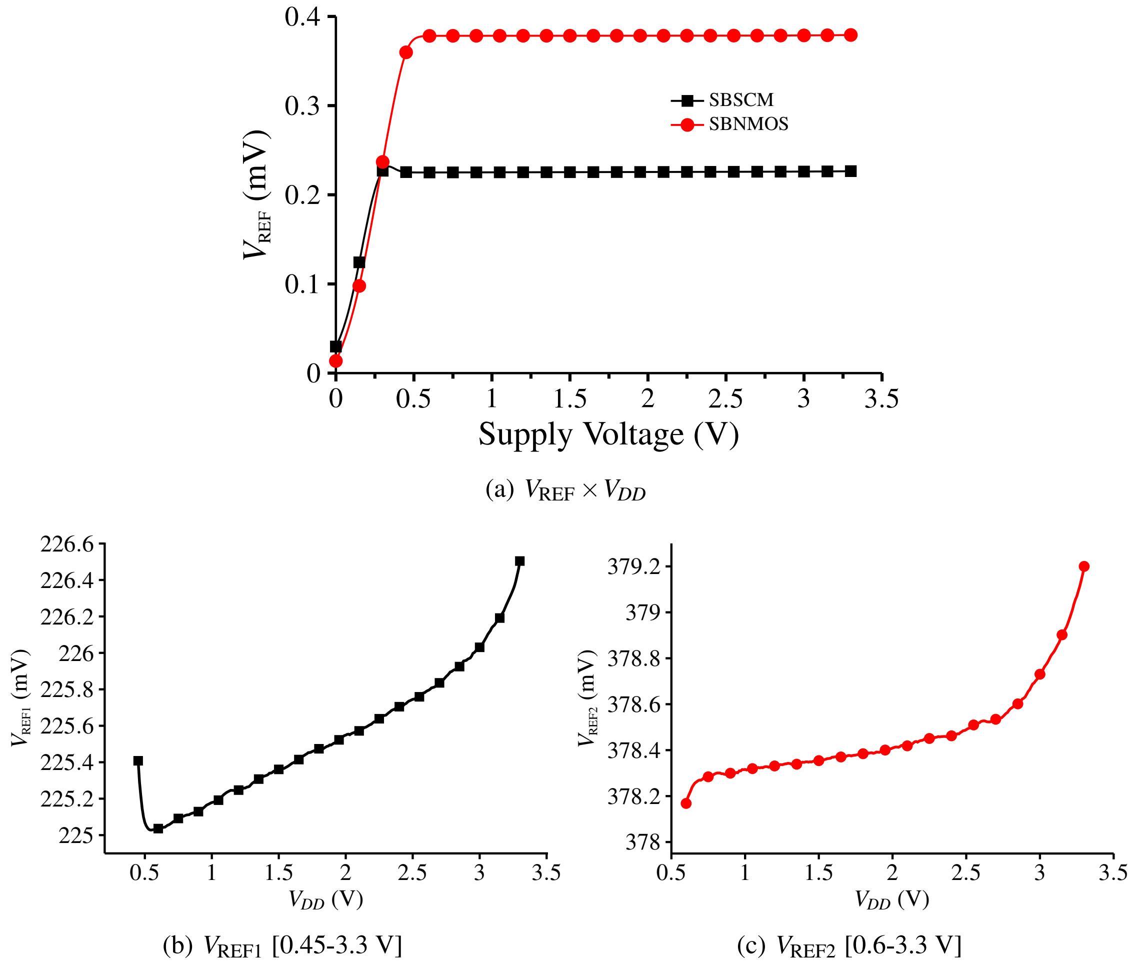


Figure 4.3: Chip photo of the proposed voltage references and their layouts.

Fig. 4.4(a) shows the measured results of the supply voltage dependence for average samples of both proposed circuits at 20 °C. As reported, the SBSCM starts to operate at 0.45 V supply, while the SBNMOS at 0.6 V supply. The average measured line sensitivity (LS) from V_{DDMIN} to 3.3 V was 0.15 %/V (SBSCM - Fig. 4.4(b)) and 0.11 %/V (SBNMOS - Fig. 4.4(c)).



(a) $V_{\text{REF}} \times V_{DD}$

(b) V_{REF1} [0.45-3.3 V]

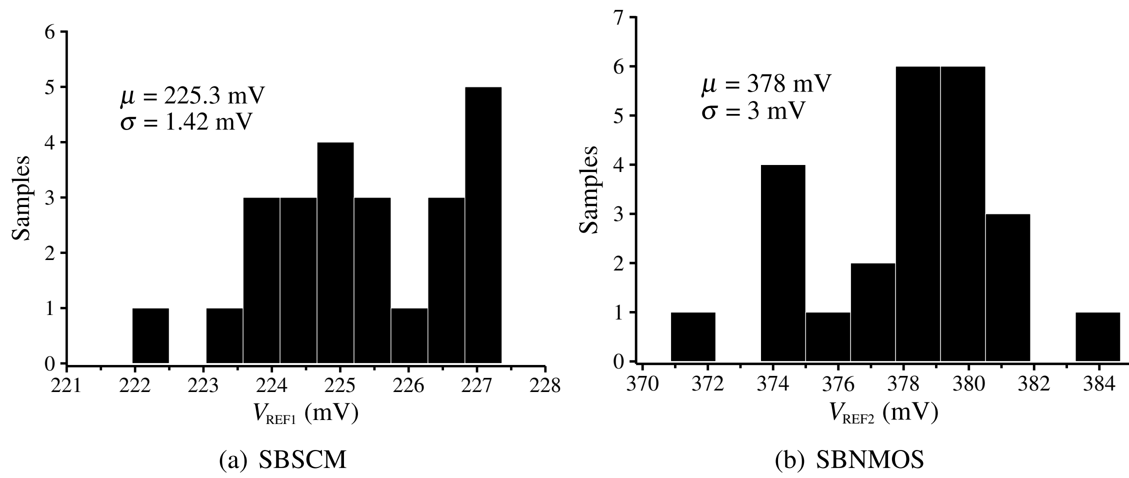
(c) V_{REF2} [0.6-3.3 V]

Figure 4.4: Measured supply voltage dependence of the proposed voltage references.

The spread of V_{REF} of the 24 measured samples of both circuits at 20 °C and minimum supply voltage are presented in Fig. 4.5. The V_{REF} mean reference voltages for the SBSCM and SBNMOS are 225.3 mV and 378 mV, respectively, and the V_{REF} variation coefficient (σ/μ - where σ and μ are the standard deviation and mean value) are 0.63 % and 0.8 %, respectively.

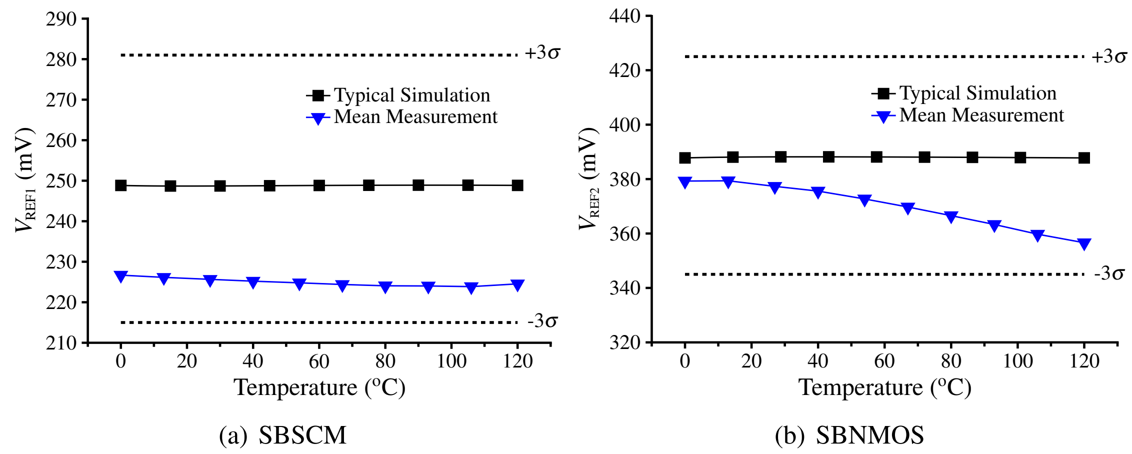
The simulated and measured temperature dependence from 0 °C to 120 °C for both circuits is shown in Fig. 4.6. The temperature coefficient (TC) is evaluated using the expression (1.1) previously defined. A TC between 68 ppm/°C and 150 ppm/°C, with a mean of 104 ppm/°C was measured from the 24 samples in the case of the SBSCM, as shown in Fig. 4.6(a), while for the SBNMOS the mean measured TC was 495 ppm/°C. The simulated worst case TCs at minimum supply voltage across all corners were 65 ppm/°C and 136 ppm/°C for the SBSCM and SBNMOS, respectively. The difference between the simulated and measured behaviors may be partially caused due to the inaccuracy of the BSIM3v3.2 for the temperature behavior in deep weak inversion (MAGNELLI et al., 2013).

Fig. 4.7 shows the measured temperature behavior of the power consumption for different values of V_{DD} for both circuits. Since they are biased with the subthreshold current, power increases exponentially with temperature. The SBSCM consumes typically 54.8 pW at 0.45 V and 27 °C and reaches a maximum of 8.6 nW at 3.3 V and 120 °C as shown in Fig. 4.7(a). The SBNMOS measured typical (0.6 V and 27 °C) and maximum (3.3



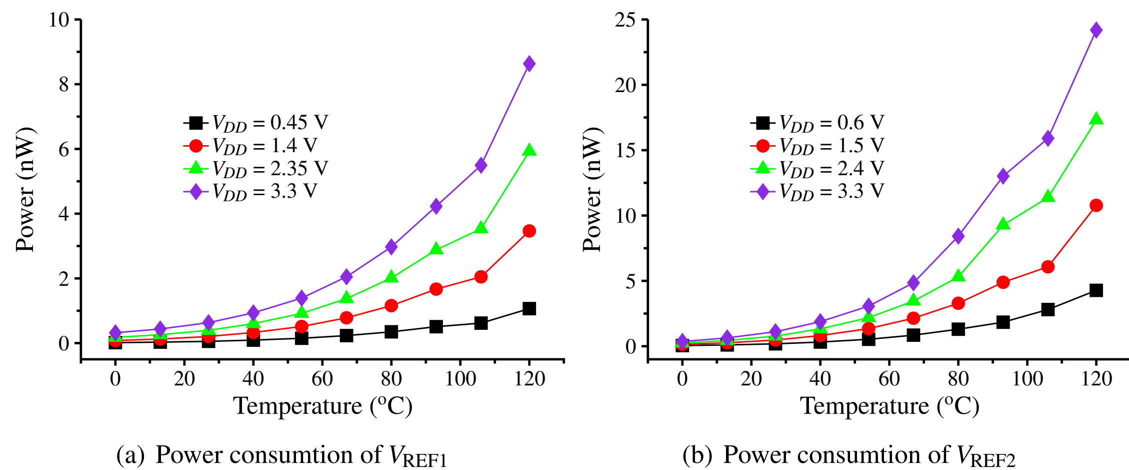
(a) SBSCM (b) SBNMOS

Figure 4.5: Distribution of V_{REF} @ 20 °C and V_{DDMIN}.



(a) SBSCM (b) SBNMOS

Figure 4.6: Measured temperature behavior for an average sample of the proposed voltage references.



(a) Power consumtion of V_{REF1} (b) Power consumtion of V_{REF2}

Figure 4.7: Measure temperature dependence of the power consumption for for different values of supply voltage for an average sample.

V and 120 °C) power consumption are 184 pW and 24.2 nW, respectively, as reported in Fig. 4.7(b). Simulated results of typical and maximum power consumption were 93 pW and 12.5 nW, respectively, for the SBSCM, while for the SBNMOS they were of 350 pW and 41.6 nW. Some discrepancy between measured and simulated power consumption is expected for both circuits. The SBSCM measured output voltage was around 25 mV less than that from simulation, which means that its current consumption was also reduced. The measured SBNMOS output voltage presented a CTAT behavior, indicating that the circuit is not biased with enough current to compensate the NMOS active load temperature dependence, thus reducing the power consumption.

Power Supply Rejection (PSR) was measured using a Keysight B2961A Low Noise Power Source and a Keysight MSO9104A scope. Fig. 4.8 presents the measured PSR for both circuits at minimum supply voltage and 100 Hz resulting -44 dB for the SBSCM and -47 dB for the SBNMOS. Worst case PSR from 10 Hz to 10 kHz are -44.5 dB (SBSCM) and -45 dB (SBNMOS). PSR measurements were done with a high input impedance buffer presenting a total input capacitance of about 4 pF.

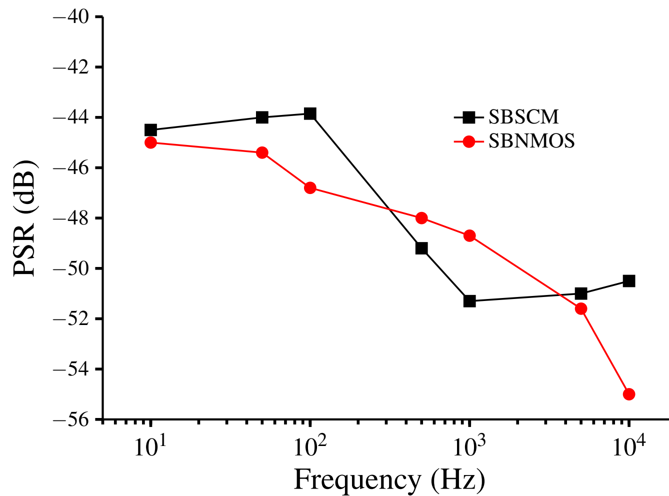


Figure 4.8: Measured PSR for both proposed circuits @ $V_{DD\text{MIN}}$.

4.2.2 Trimming Analysis

It is well known that sensitivity to process variations of circuits with transistors in subthreshold increases dramatically. Due to the exponential I-V characteristics of MOS transistor in weak inversion, any small variation in threshold voltage causes an exponential change in drain current. Voltage references operating at such region are usually hardly process dependent and present a large spread of both output reference voltage and its TC (MAGNELLI et al., 2011; OSAKI et al., 2013; SEOK et al., 2012). These variations can be compensated through trimming techniques. From expressions (3.8) and (3.13), process variations of the generated reference voltages can be compensated by either increasing or decreasing the current gains K_1 and K_2 through a digital control.

From the corner simulations presented in Fig. 4.10, the SBSCM and SBNMOS are expected to have a ΔV_{REF} at room temperature of approximately ±6% and ±8%, respectively. As presented in BRITO; BAMPI; KLIMACH (2007), the number of bits of the

trimming circuit is determined by the following expression

$$\text{BITS} \geq \frac{\ln\left(\frac{V_{FS}}{V_{LSB}} + 1\right)}{\ln(2)} \tag{4.1}$$

where V_{LSB} is the least significant bit voltage and V_{FS} is the full-scale voltage.

The trimming circuit must be designed to cover the entire output voltage variation range while a reasonable V_{LSB} must be chosen in order to reduce the spread of V_{REF}, compensating the output voltage for a target TC (SEOK et al., 2012). Therefore, the trimming circuit is designed to cover the maximum range at room temperature while having a small V_{LSB} for fine TC compensation. Thus, for SBSCM, by choosing $V_{FS} = 6\%V_{\text{REF1}}$ and $V_{LSB} = 0.25\%V_{\text{REF1}}$ leads to a 5-bit trimming circuit.

The SBNMOS can be adjusted by increasing or decreasing current gain K_1, which is equivalent to adding or sinking current at the reference voltage node. This can be achieved by using a current-trimming technique ZHU; HU; WANG (2016), where the trimming circuit can cover all the variation of the output voltage at room temperature. Defining $V_{FS} = 8\%V_{\text{REF2}}$ and using the same 5 bits as for the SBSCM, leads to $V_{LSB} = 0.3\%V_{\text{REF2}}$. The schematic of the 5-bit trimming circuit of the proposed voltage references is shown in Fig. 4.9.

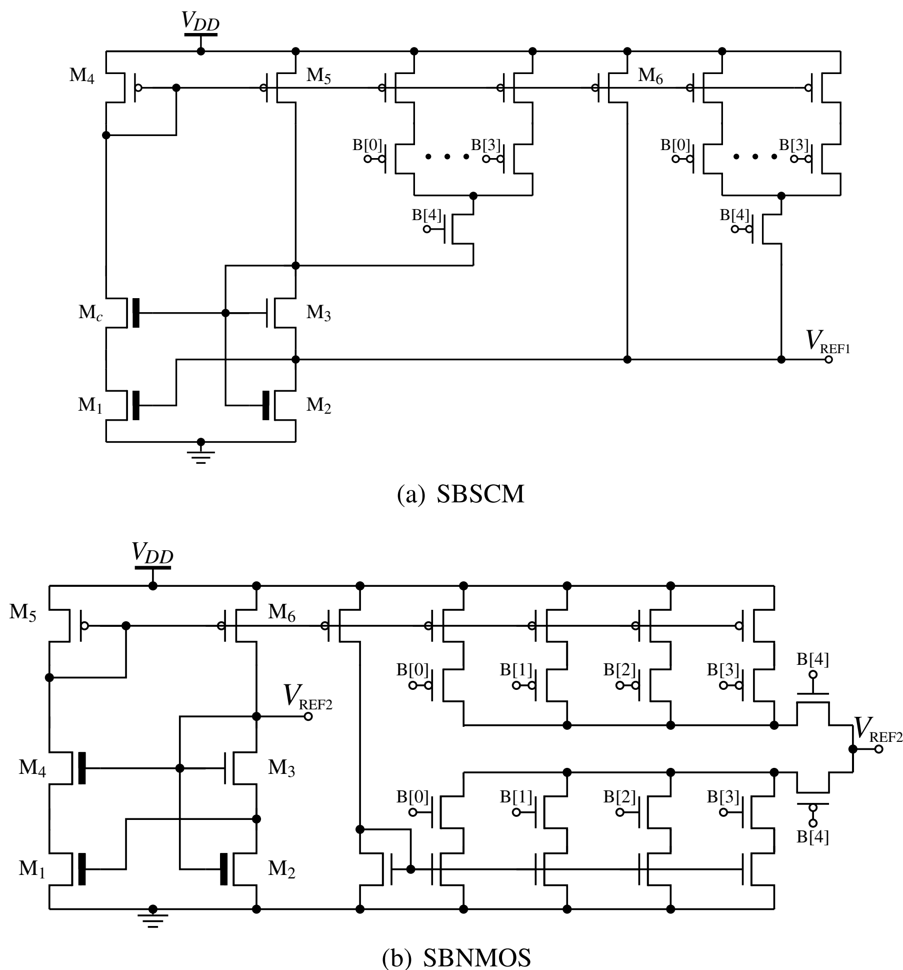
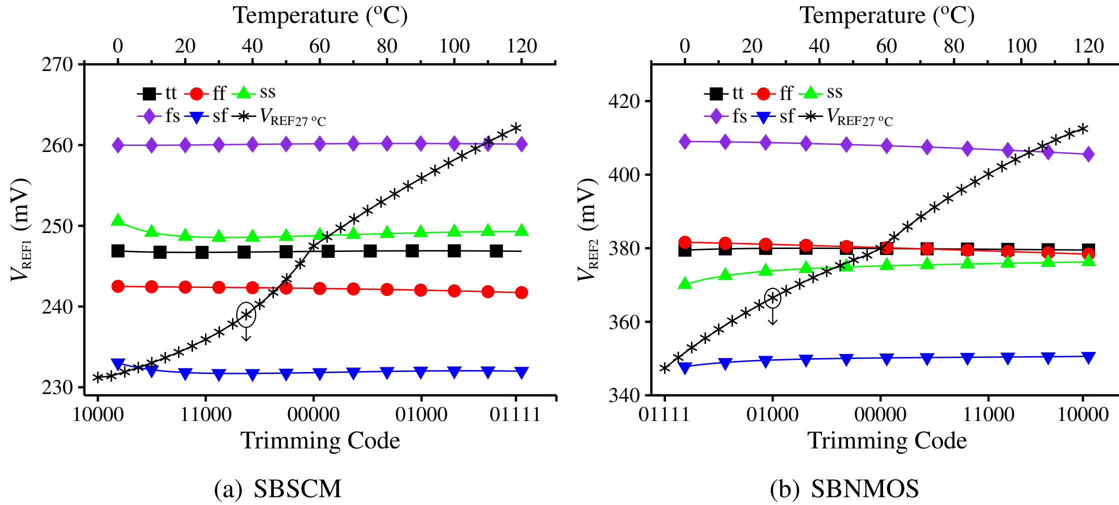


Figure 4.9: 5-bit trimming scheme for the proposed circuits.

The simulation of the trimming circuit, as well as the variation of the output voltage

with process corners, is shown in Fig. 4.10. For both circuits, the increase/decrease of the current gain is defined by the control bits B[4:0], where B[4] is a sign bit that determines the direction of the resulting trim to the output voltage, and B[3:0] are the binary codes proportionally controlling the current mirror gains (WANG et al., 2015). As it is clearly shown by Figures 4.10(a) and 4.10(b), the proposed trimming circuits can cover all process variations.



(a) SBSCM (b) SBNMOS

Figure 4.10: Simulated 5-bit trimming range for the proposed circuits.

Even though the trimming circuits were not fabricated due to silicon access restrictions, they can be emulated with the assitance of the measurement equipment, since each DC channel of the Keysight-4156 can perform a precision programmable current source at the same time it measures the node V_{REF}. This emulation can be made by increasing or decreasing the current at the voltage reference node through the following process: 1) By processing the measured data of a given sample through a mathematical software, an optimal temperature-compensated V_{REFOPT} is obtained; 2) Experimentally, at 27 °C a current (I_T) is sunk or applied to the reference node of the processed sample in order to achieve the same value as V_{REFOPT} in this temperature; 3) The generated currents of the proposed circuits increases exponentially with temperature, hence the applied/sunk I_T trimming current must follow this behavior. Using the obtained I_T from the previous step as starting point, the current that must be applied to the other temperature points is obtained by approximating it with a function that increases exponentially.

The CTAT behavior of the measured circuits indicates that there is not enough current to compensate their output voltages. Therefore, more current must be applied to them. As an example, Fig. 4.11 presents the measured current consumed by Sample 1 and the trimming current applied to it to emulate the trimming function, showing that the applied current follows the temperature behavior of the generated current.

The measured results after the trimming emulation, as explained before, for five random selected samples at minimum supply voltage are shown in Fig. 4.12. The measured TCs with trimming emulation for the 5 samples of the SBSCM were 34, 60.7, 75.4, 100 and 93 ppm/°C, while for the SBNMOS they were 13.2, 16, 7.25, 9 and 12.7 ppm/°C. The TCs for the SBNMOS were expected to be lower when comparing to those from the SBSCM since the latter circuit presented a more defined CTAT behavior. The TC and power consumption were 72.4 ppm/°C and 147 pW for the SBSCM, and 11.6 ppm/°C

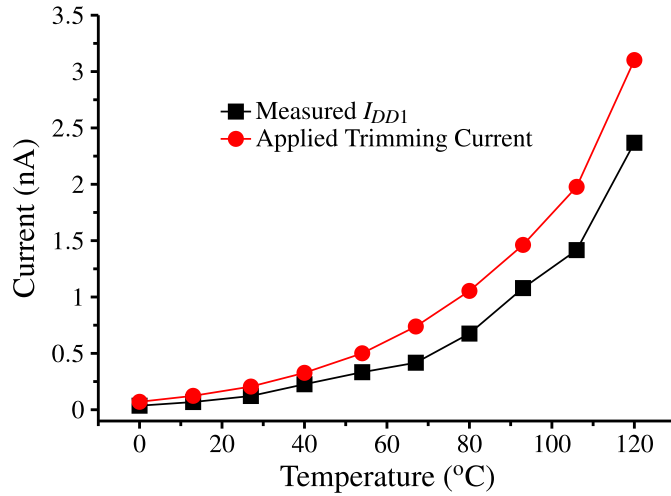


Figure 4.11: Current consumption and applied current to emulate the trimming function for Sample 1.

and 664 pW for the SBNMOS. Since the trimming circuits were not included in the fabricated references due to silicon access restrictions the presented emulation approach can help to validate the process compensation trimming scheme that was proposed.

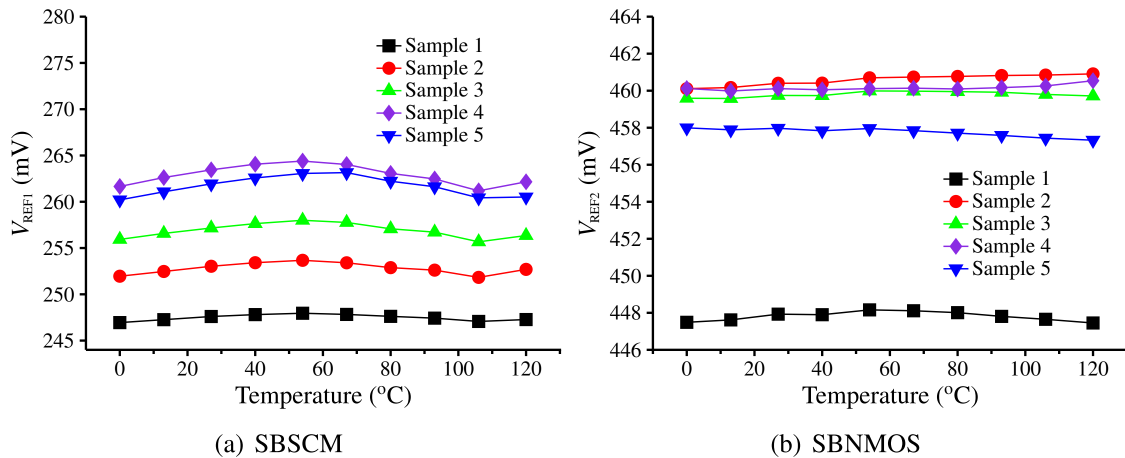


Figure 4.12: Measured temperature dependence of V_{REF} for five samples after trimming emulation.

4.3 3-Transistor Voltage References

For the 3T voltage reference 4 versions were designed and fabricated: using the conventional approach to achieve the lowest TC with the maximum temperature range (Conv.); a 0.4 V supply with PSR enhancement (PSR Enhanc.); a Sub-kT/q and a high-order (HO) compensated voltage reference. The following sections present the post-layout simulation results for each of these versions. Figure 4.13 shows the chip photo and the respective layout for each version of the 3T voltage reference.

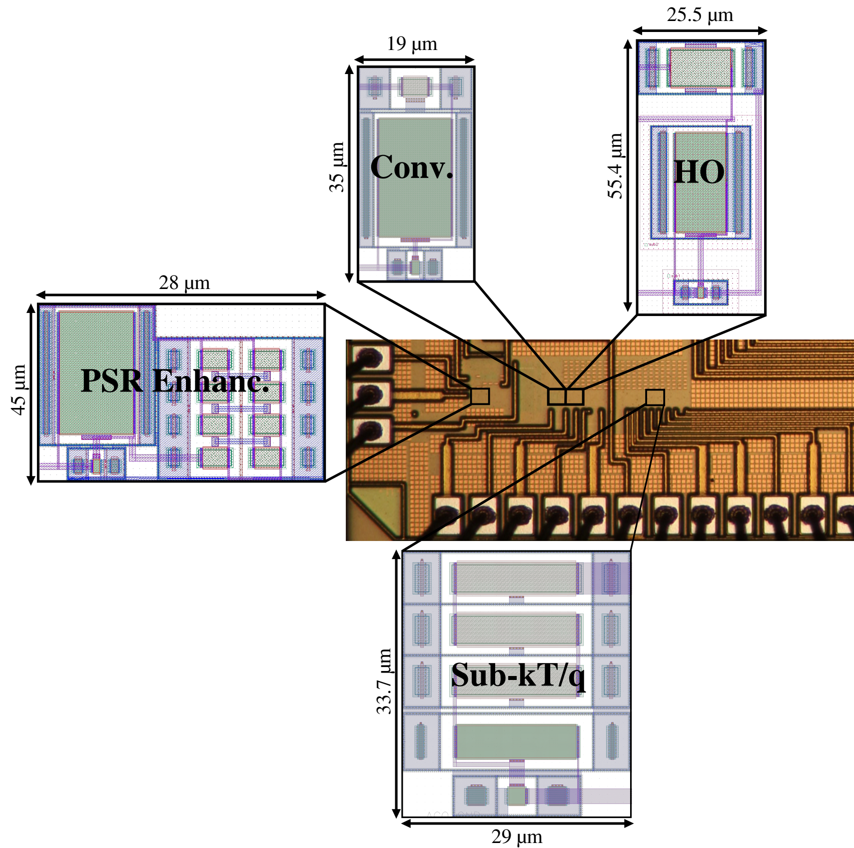


Figure 4.13: Chip photo of the proposed 3T voltage references and their layouts.

4.3.1 Post-Layout Simulation Results

The following subsections present the post-layout simulation results for the 4 versions described above. The proposed 3T voltage references were designed in a standard 0.13-µm CMOS process.

4.3.1.1 Conventional and PSR Enhancement

The following results are for post-layout simulation of a standard 0.13-µm. The layout of the Conv. (red) and PSR Enhanc. (blue) versions are shown in Fig. 4.13. The occupied area of these circuits are and 0.0006 and 0.0012 mm^2, respectively. The Conv. version is expected to start to operate at 0.3 V supply voltage, while the PSR Enhanc. is 0.4 V. The dependence of the voltage reference generated by these versions with respect to the supply voltage is shown in Fig. 4.14. The LS of the proposed circuits are 0.07 and 0.006 %/V for the 0.3-1.2 V (Conv.) and 0.4-1.2 V (PSR Enhanc.) supply voltage range. The PSR Enhanc. presented an LS reduction of more than 11 times when compared with the conventional approach. This was expected since this version was designed to provide a voltage reference more independent on supply voltage variations.

The sensitivity of the proposed versions with respect to temperature variations in the -25 ^{o}C to 125 ^{o}C temperature range can be evaluated through Fig. 4.15. The voltage reference at minimum supply voltage is around 62.3 mV for both versions. At the typical corner, the Conv. version presents a TC of 15 ppm/^{o}C at V_{DD}=0.3 V and reaches 24.6 ppm/^{o}C at V_{DD}=1.2 V. Under the same conditions the TC of PSR Enhanc. version is almost independent of V_{DD}, presenting a variation of 14.3 to 14.9 ppm/^{o}C from 0.4 to 1.2

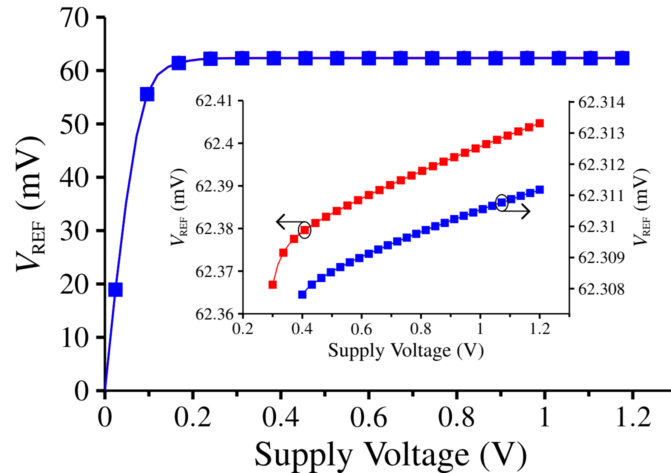


Figure 4.14: Line sensitivity of the Conv. (red) and PSR Enhanc. (blue) versions.

V supply voltage.

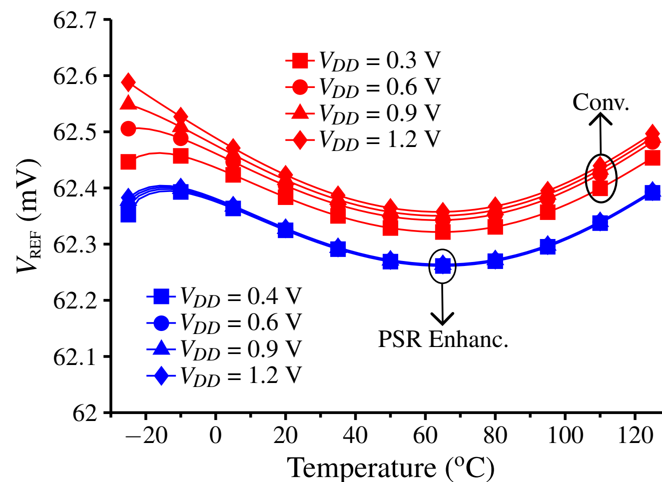


Figure 4.15: Voltage reference temperature dependence of the Conv. (red) and PSR Enhanc. (blue) versions.

The power consumption temperature dependence for different values of the supply voltage is shown in Fig. 4.16. At room temperature and minimum supply voltage the Conv. and PSR Enhanc. versions consume 21 pW and 28 pW, respectively, while they reach a maximum of 2.1 nW and 1.96 nW at 125 °C and 1.2 V supply voltage.

The PSR of both versions is presented in Fig. 4.17. The Conv. and PSR Enhanc. presented a PSR of -67.3 dB and -98 dB at the minimum supply voltage, 100 Hz and without any filtering capacitor, respectively. The results show that we can improve the PSR by -30 dB by adding another series transistor to compose I_{LOAD} and at the cost of 100 mV in the minimum supply voltage.

4.3.1.2 Sub-kT/q

Once again, the layout of the Sub-kT/q version is shown in Fig. 4.13, where it occupies a total silicon area of 0.0009 mm^2. As described in the design methodology section, this version was designed to provide an output voltage reference less than 20 mV. By doing so

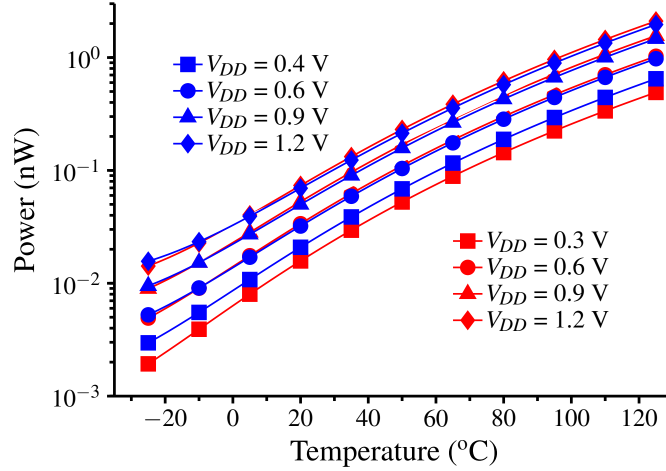


Figure 4.16: Power consumption temperature dependence of the Conv. (red) and PSR Enhanc. (blue) versions.

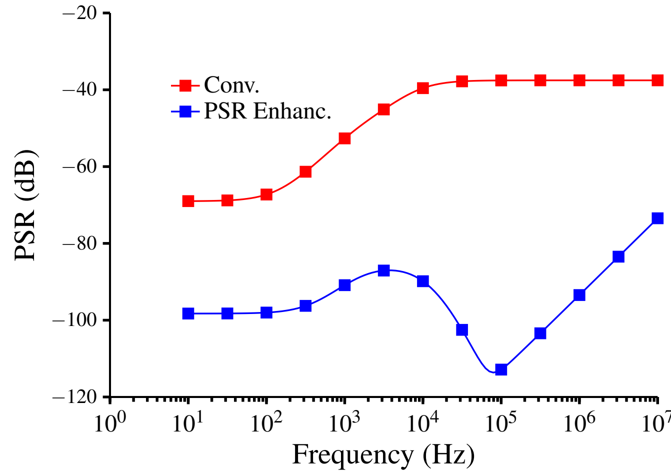


Figure 4.17: Power Supply Rejection of the Conv. (red) and PSR Enhanc. (blue) versions @ $V_{DD_{\mathrm{MIN}}}$.

and considering that M_3 will operate at deep triode, thus significantly reducing its power consumption at the minimum supply voltage. This version was designed to provide a 16 mV output voltage. Its sensitivity with respect to supply voltage variations is shown in Fig. 4.18. As can be seen, the circuit can be considered to operate at a minimum supply voltage of 120 mV while presenting a reasonable LS of 0.216 %/V.

The generated voltage reference temperature dependence for different values of supply voltage is presented in Fig. 4.19. At typical corner, the circuit presents a TC of 754 ppm/°C at V_{DD} = 120 mV, while for $V_{DD} > 500$ mV the TC stays at 170 ppm/°C.

The proposed version consumes merely 430 fW at the minimum supply voltage and room temperature and reaches 535 pW at 1.2 V supply voltage and 125 °C, as shown in Fig. 4.20. The remarkably fentowatt power consumption is because at 120 mV supply voltage M_3 is in deep triode, thus reducing the power consumption.

As Fig. 4.21 shows, the PSR for the Sub-kT/q version is -120 dB at 100 Hz and V_{DD} = 1.2 V and stays less than -90 dB up to 10 MHz. For the minimum supply voltage, V_{DD} = 120 mV, the PSR increases to -38.4 dB. The deep triode operation of M_3 at such low supply voltage degrades de PSR because at 120 mV supply the V_{DD} variations are

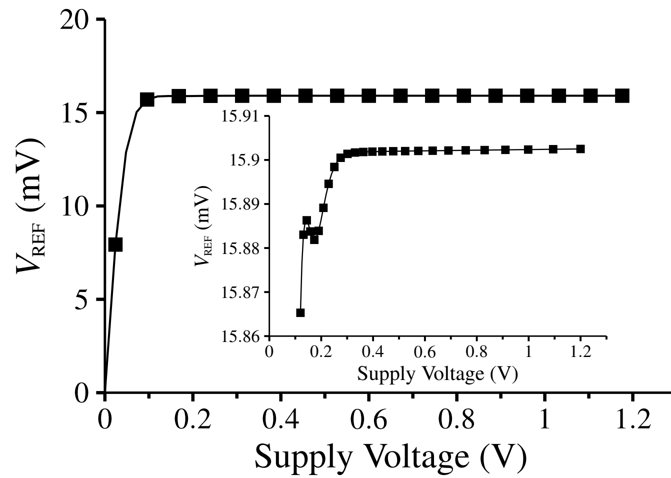


Figure 4.18: Sensitivity to supply voltage variations of the Sub-kT/q version.

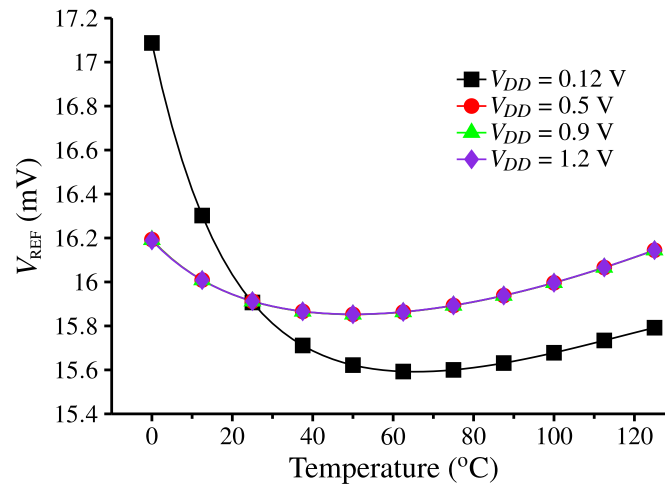


Figure 4.19: Temperature dependence of the Sub-kT/q version.

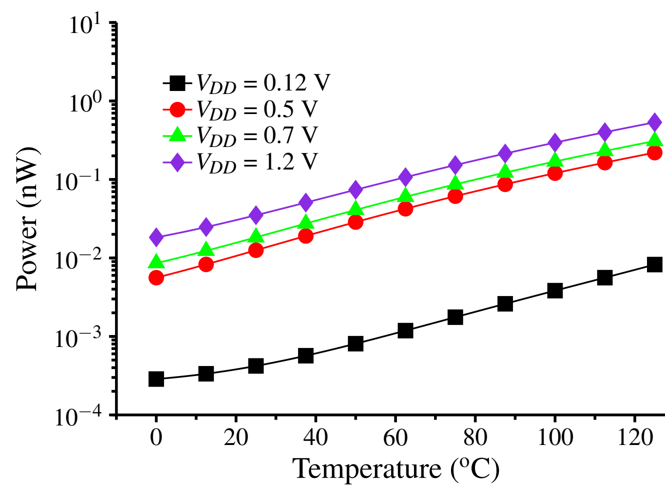


Figure 4.20: Power consumption temperature dependence of the Sub-kT/q version.

transferred directly to the gate of M_1 and M_2.

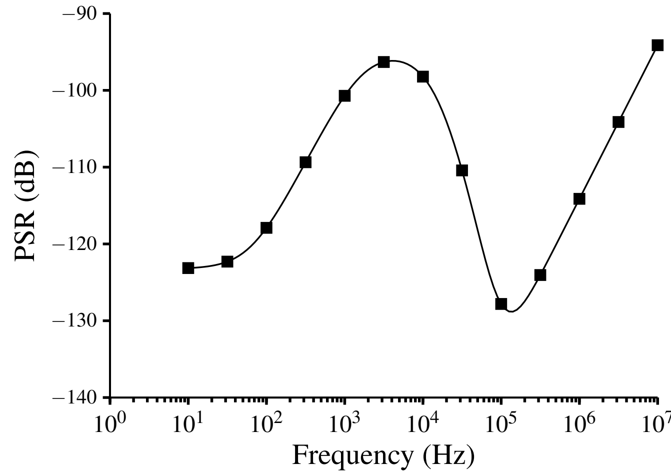
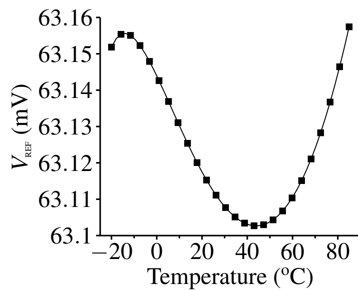
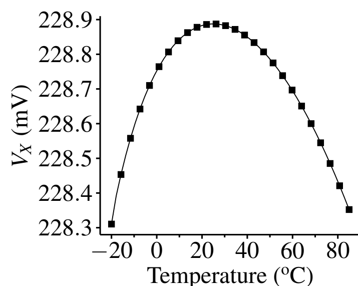


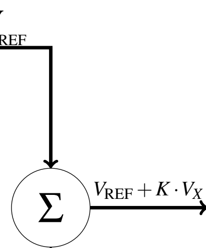
Figure 4.21: Power Supply Rejection of the Sub-kT/q version @ 1.2 V.

4.3.1.3 High-Order Curvature Compensated

Post-layout simulation results for the temperature behavior of high-order temperature-compensated V_{REF} is presented by Fig. 4.22, which shows V_{REF} and V_X voltages optimized for the -20 °C to 85 °C range, defined as the conventional approach (Conv.), and its sum, with $K < 1$, resulting in the high-order compensation. From typical simulations, the conventional circuit presented a TC of 8 ppm/°C while the proposed circuit achieves a minimum TC of 1 ppm/°C at 300 mV of supply voltage with an average value of 90.5 mV.







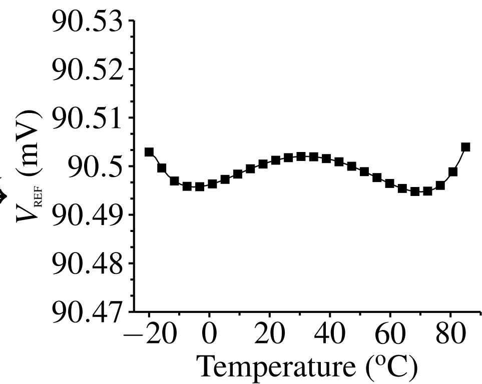
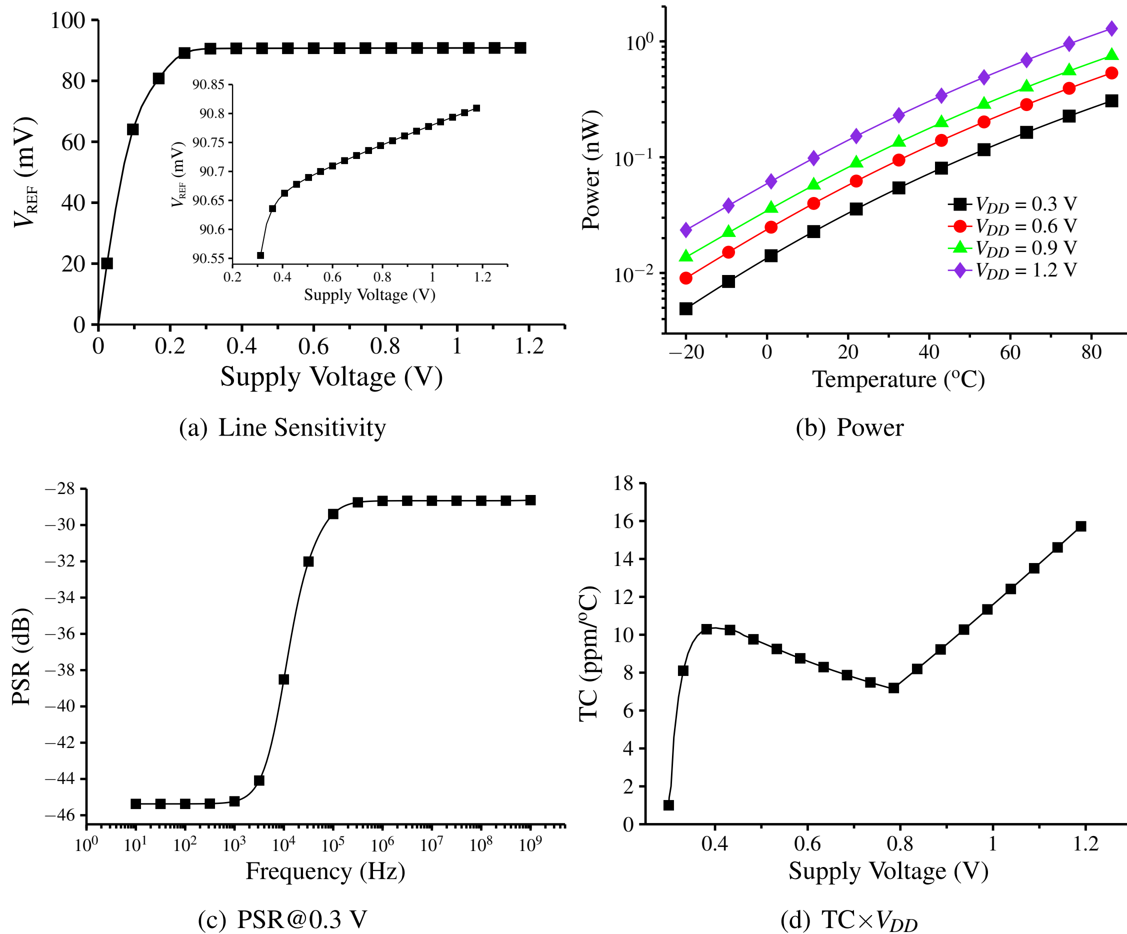


Figure 4.22: Temperature behavior of the proposed high-order voltage reference.

The LS obtained from 0.3 V to 1.2 V is 0.4 %/V as presented by Fig. 4.23(a). The circuit consumes 43.7 pW at 0.3 V supply and 27 °C, and reaches a maximum of 1.3 nW at 1.2 V and 85 °C, as shown by Fig. 4.23(b). At 0.3 V the circuit achieves a PSR of

-45.3 dB at 100 Hz and -28.6 dB for higher frequencies, as shown by Fig. 4.23(c). The dependence of TC with respect to V_{DD} is presented by Fig. 4.23(d), where it presents a minimum TC of 1 ppm/°C at 0.3 V and a maximum 16 ppm/°C at 1.2 V.



(a) Line Sensitivity

(b) Power

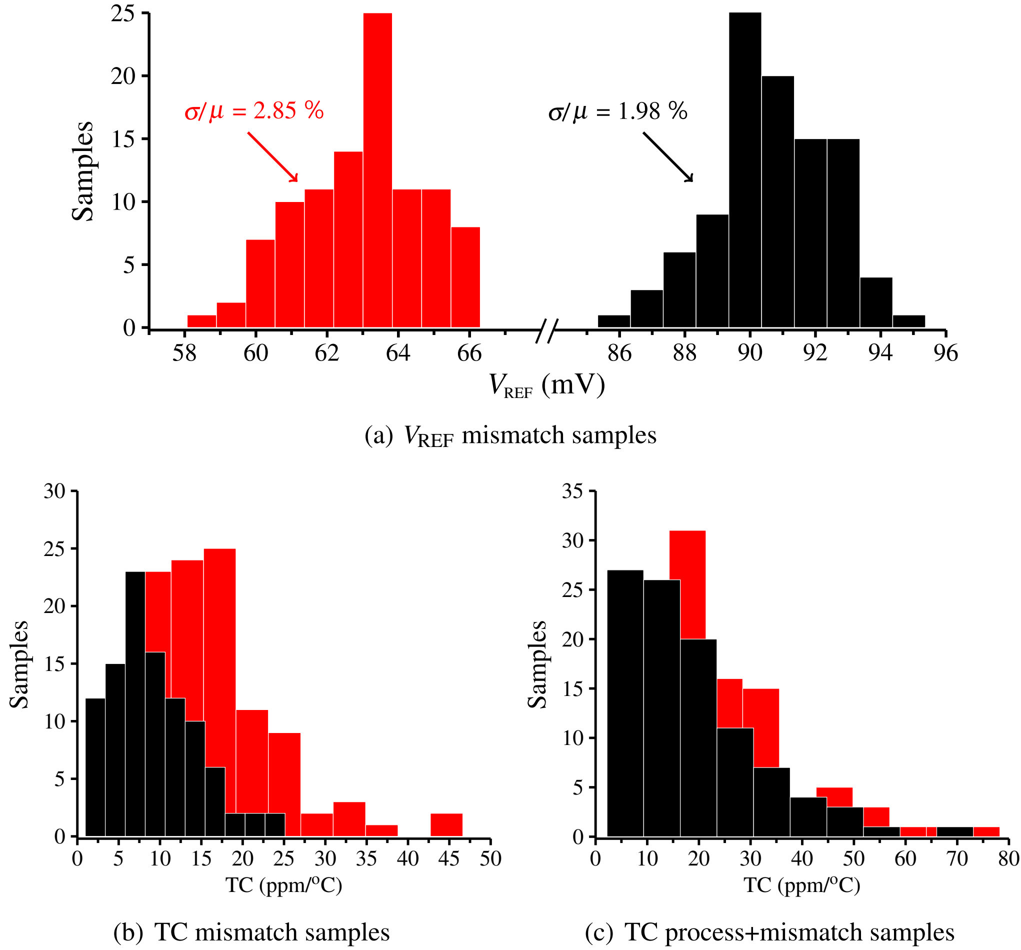
(c) PSR@0.3 V

(d) TC×V_{DD}

Figure 4.23: Post-layout performance for the 3T High-Order (HO) version.

The sensitivity to process and mismatch variability of the conventional and proposed circuits are presented in Fig. 4.24. The mismatch variability is presented by Fig. 4.24(a), where for the conventional implementation the circuit presents a $\sigma/\mu = 2.85$ % while the proposed circuit presented a σ/μ = 1.98 %. As the results show, the proposed scheme makes the spread of the voltage reference stay the same while its mean was increased, resulting in a 30% attenuation of the mismatch variability coefficient. This was achieved with approximately the same S_1 and S_2 ratios as for the conventional approach.

Considering mismatch variations, an average TC of 9.3 ppm/°C is achieved for the proposed circuit while the conventional reached a mean of 17 ppm/°C. When considering both process and mismatch variations, once again the proposed circuit presented a lower mean TC (18 ppm/°C) compared to the conventional approach (26 ppm/°C). In both cases, the spread of the TC in the proposed circuit was reduced. These results validate the proposed variability attenuation scheme.



(a) V_{REF} mismatch samples

(b) TC mismatch samples

(c) TC process+mismatch samples

Figure 4.24: Variability results for the conventional (red) and the proposed (black) 3-transistor voltage reference @ 0.3 V.

4.4 Comparison With Other Works

Table 4.1 and Fig. 4.25 summarize the performance of the proposed circuits in comparison with published low power CMOS voltage references.

4.4.1 Self-Biased Voltage References

When compared with the non-self-biased works (Non-SB), the SBSCM and SBNMOS circuits presented 47.5× and 7.75× of power and area improvement, respectively, while presenting the best FoM performance. As Fig. 4.25 explicitly shows besides presenting better FoM than Non-SB, the leakage based solutions have the smaller area and power consumption. The performance of the self-biased circuits concerning power, area, and FoM is among the best in literature. Although LEE; SYLVESTER; BLAAUW (2017) presents a higher FoM, when the 3T circuits are not considered, its minimum supply voltage is 1.4 V which is not suitable for low voltage applications. The SBSCM 0.45 V operation is in the range of ultra-low voltage applications.

4.4.2 3T Voltage References

The 3T voltage references presented a FoM more than a decade better than previous works. The Conv. version presents the smallest area and highest FoM among the

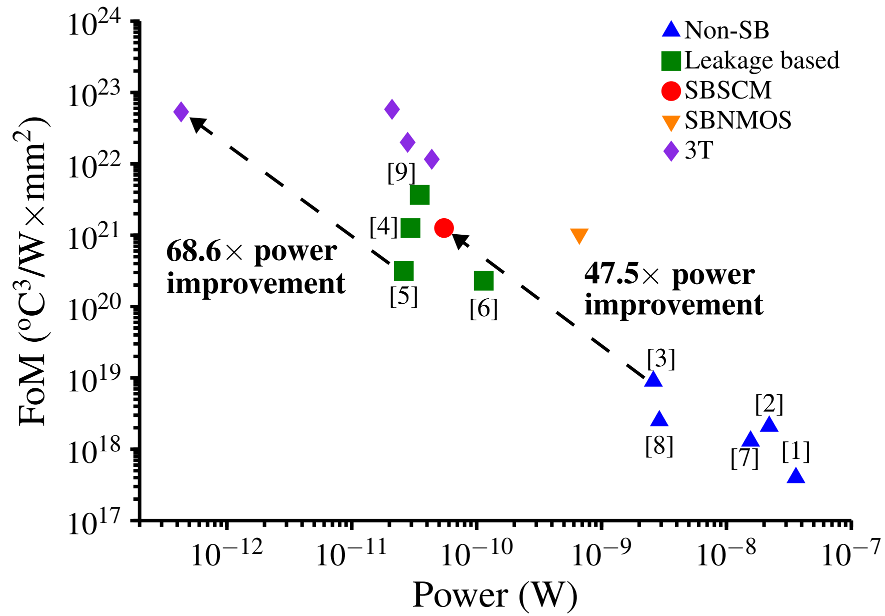
state-of-the-art. The Sub-kT/q version has the lowest minimum supply voltage and better performance, when compared with the only Sub-kT/q voltage reference presented in literature (ALBANO et al., 2015) while operating at sub-pW power consumption range. Compared with the lowest power consumption and the smallest area of the voltage references published so far, the proposed 3T voltage references presented 68.6× and 2× of power and area improvement, respectively.

Table 4.1: Performance Summary of the Proposed Circuits and Comparison With Other Works

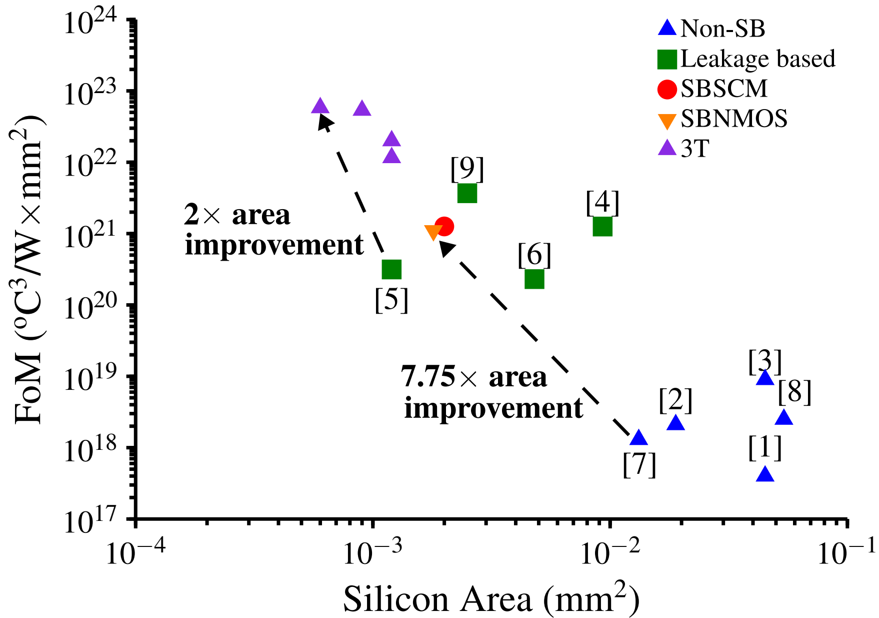
Specification	[1]	[2]	[3]	[4][a]	[5]	[6]	[7][a]	[8][a]	[9][a]
Technology (µm)	0.35	0.35	0.18	0.13	0.18	0.18	0.18	0.35	0.18
V_{DD} (V)	0.9-4	1.1-4	0.45-2	0.5-3	0.15-1.8	1.2-2.2	0.45-1.8	0.9-3	1.4-3.6
V_{REF} (mV)	670	96.6	263.5	176	17.69	986.2	118.41	713	1.25
Temp. Range (°C)	0-80	-20-80	0-120	-20-80	0-120	-40-85	-40-85	-20-80	0-100
TC (ppm/°C)	10	11.4	142	29	1462	124	59.4	26	31
LS (%/V)	0.27	0.09	0.44	0.036	2.03	0.38	0.033	0.3	0.31
PSR @ 100 Hz (dB)	-47	-60	-45	-51	-64	-42	-50.3	-	-41
Power (pW)	36,000	22,000	2,600	29.5	26.1	114	15,600	2,900	35
Area (mm^2)	0.045	0.0189	0.045	0.0093	0.0012	0.0048	0.0132	0.054	0.0025
FoM[b] (°C^3/W×mm^2)	0.0004	0.002	0.0007	1.25	0.315	0.23	0.0013	0.0025	3.7

Specification	**SB Voltage References[+]**				**3T Voltage References[*,×]**			
	SBSCM		**SBNMOS**		**Conv.**	**Sub-kT/q**	**PSR**	**HO**
Technology (µm)	**0.18**				**0.13**			
V_{DD} (V)	**0.45-3.3**		**0.6-3.3**		**0.3-1.2**	**0.12-1.2**	**0.4-1.2**	**0.3-1.2**
V_{REF} (mV)	**225.3**	**256.6[a]**	**378**	**457.1[a]**	**62.2**	**15.9**	**62.3**	**90.7**
Temp. Range (°C)	**0-120**				**-25-125**	**0-125**	**-25-125**	**-20-85**
TC (ppm/°C)	**104**	**72.4[a]**	**495**	**11.6[a]**	**30.7**	**240.4**	**33**	**18**
LS (%/V)	**0.15**		**0.11**		**0.07**	**0.216**	**0.006**	**0.4**
PSR @ 100 Hz (dB)	**-43.9**		**-46.8**		**-67.3**	**-38.4**	**-98**	**-45.3**
Power@27°C (pW)	**54.8**	**147[a]**	**184**	**664[a]**	**21**	**0.43**	**28**	**43.7**
Area (mm^2)	**0.002**		**0.0017**		**0.0006**	**0.0009**	**0.0012**	**0.0012**
FoM[b] (°C^3/W×mm^2)	**1.26**		**1.1**		**58.1**	**53.5**	**20.3**	**11.6**

[+]Measurement; [*]Simulation; [×]PC + MM (1000 runs); [a]After Trimming; [b]$\times 10^{21}$;
[1] VITA; IANNACCONE (2007); [2] YAN; LI; LIU (2009); [3] MAGNELLI et al. (2011);
[4] SEOK et al. (2012); [5] ALBANO et al. (2015); [6] DONG et al. (2016);
[7] ZHU; HU; WANG (2016); [8] LUONG et al. (2017); [9] LEE; SYLVESTER; BLAAUW (2017);



(a)



(b)

Figure 4.25: FoM related improvement regarding (a) power consumption and (b) occupied area.

5 CONCLUSION

In this thesis, we discussed the recent developments of ultra-low power voltage references operating at very-low supply voltages. Specifically, special attention was given for those operating at nanowatt/picowatt power consumption range. The main target of such circuits lies on the Internet of Things (IoT) scope, such as energy harvesting systems and energy-autonomous platforms. The power budget of these applications is extremely constrained, thus leading to the development of voltage references to attend this constraint.

The SCM structure is suitable for such applications since it can operate at very low current levels. It has been widely used to perform voltage or current generation functions. But prior works perform these functions separately, which leads to a higher power consumption. Therefore, we explore self-biasing within the voltage reference generation to further reduce the power consumption of SCM-based voltage references. Based on the SCM with different V_T transistors, two variants of the same structure were proposed: a self-biased self-cascode MOSFET (SBSCM) and a self-biased NMOS (SBNMOS) load. Both circuits are described in detail, and design considerations are discussed. To compensate for after fabrication process variations, trimming techniques for both circuits are presented. The proposed circuits were fabricated in a standard 0.18-μm CMOS process. Measurement results for 24 samples show that they can operate at 0.45-0.6 V minimum supply voltages, consuming merely 54.8 and 184 pW at room temperature. Without trimming, from 0 to 120 ^{o}C the circuits presented a temperature coefficient of 104 and 495 ppm/^{o}C, while after trimming this values were reduced to 72.4 and 11.6 ppm/^{o}C at the cost of increasing the power consumption. The variants of the proposed circuit achieve a line sensitivity of 0.11 and 0.15 %/V and a power supply rejection of -43.9 and -46.8 dB. Also, the occupied silicon of the proposed circuits are 0.002 and 0.0017 mm^2, respectively.

Distinct V_T devices have different fabrications processes. Consequently, their process sensitivity related to one another is large. Which also increases the sensitivity of the generated voltage/current references to process variations. To attenuate these variations, we explore the dependence of V_T with the transistor dimension (RSCE and NWE) to obtain distinct V_T while using devices of the same type. The proposed circuit is also based on the SCM, and it is biased with the leakage current of a zero-V_T for PSR improvement and ultra-low power consumption, leading to a 3T voltage reference. A detailed designed methodology is described. To show its versatility, five different versions of the proposed circuit were designed: a conventional, PSR enhancement, sub-kT/q, high-order compensation and with reduced power consumption. The 3T voltage references were fabricated in a standard 0.13-μm CMOS process. Post-layout simulation results show that the proposed circuit can operate 0.12 to 0.4 V minimum supply voltages with sub-pW/pW power consumption.

The measured (SBSCM and SBNMOS) and simulated (3T) performances were compared with the state-of-the-art. The comparison shows that the SB VRs presented a 47.5× and 7.75× power and area improvement, respectively, with the best FoM performance when compared to non-self-biasing solutions. Besides presenting the highest FoM, the 3T VRs versions also presented the lowest minimum supply voltage, silicon area, and power consumption when compared to all works used for comparison purposes. The given performances and ULV and ULP operation make the VRs circuits proposed in this thesis suitable for extreme power-constrained applications, such as battery voltage supervisors and ultra-low power temperature sensors for IoT applications.

5.1 Future Works

There are several issues and applications of the circuits proposed in this thesis to be addressed, such as the measurement of the 3T VRs and the application of theses circuits. During the MSc studies, several other circuits were developed and were left out of this thesis. Below, are listed the next steps of the research related to the proposed circuits:

1. Measurement of 3T voltage references fabricated in 0.13-µm;
2. Publication of the results of the proposed circuits;
3. Measurement of the current references published in ISCAS'2017;
4. Development of current references using the reverse short-channel and narrow-width effects;
5. Development of relaxation oscillators and temperature sensors based on the proposed structures.

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APPENDIX A LIST OF PUBLICATIONS

A Journal Papers

A1. OLIVEIRA, A. C., CORDOVA, D., KLIMACH, H. D. and BAMPI, S. *"Picowatt, 0.45-0.6 V Self-Biased Subthreshold CMOS Voltage Reference"*. Submitted to IEEE Transactions on Circuits and Systems-I: Regular Papers (**TCAS-I**). *Invited paper to the Special issue on LASCAS´17. Under Review.*

B Conference Papers

B1. OLIVEIRA, A. C., CORDOVA, D., KLIMACH, H. D. and BAMPI, S. *"An Ultra-Low Power High-Order Temperature-Compensated CMOS Voltage Reference"*. Proceedings of the 15th IEEE International New Circuits and Systems Conference (**NEWCAS'17**). Strasbourg, France. June 2017.

B2. CORDOVA, D., OLIVEIRA, A. C., TOLEDO, P., KLIMACH, H. D., BAMPI, S. and FABRIS, E. *'A Sub-1 V, Nanopower, ZTC Based Zero-*$\mathrm{V_T}$ *Temperature-Compensated Current Reference"*. Proceedings of the IEEE International Symposium on Circuits and Systems (**ISCAS'17**). Baltimore, United States. May 2017.

B3. OLIVEIRA, A. C., CORDOVA, D., KLIMACH, H. D. and BAMPI, S. *"A 0.45 V, 93 pW Temperature-Compensated CMOS Voltage Reference"*. Proceedings of the 8th IEEE Latin American Symposium on Circuits and Systems (**LASCAS'17**). Bariloche, Argentina. February 2017.

B4. CORDOVA, D., OLIVEIRA, A. C., TOLEDO, P., KLIMACH, H. D., BAMPI, S. and FABRIS, E. *"A 0.3 V, High-PSRR, Picowatt NMOS-Only Voltage Reference using zero-*V_T *Active Loads"*. Proceedings of the 29th Symposium on Integrated Circuits and Systems Design (**SBCCI'16**). Belo Horizonte, Brazil. September 2016. *3rd Place Best Paper Award*

B5. OLIVEIRA, A. C., CAICEDO, J. G., KLIMACH, H. D. and BAMPI, S. *"0.3 V Supply, 17 ppm/°C 3-Transistor Picowatt Voltage Reference"*. Proceedings of the 7th IEEE Latin American Symposium on Circuits and Systems (**LASCAS'16**). Florianopolis, Brazil. February 2016.