STUDY AND IMPLEMENTATION OF ROUTING PREDICTION ALGORITHMS FOR VLSI

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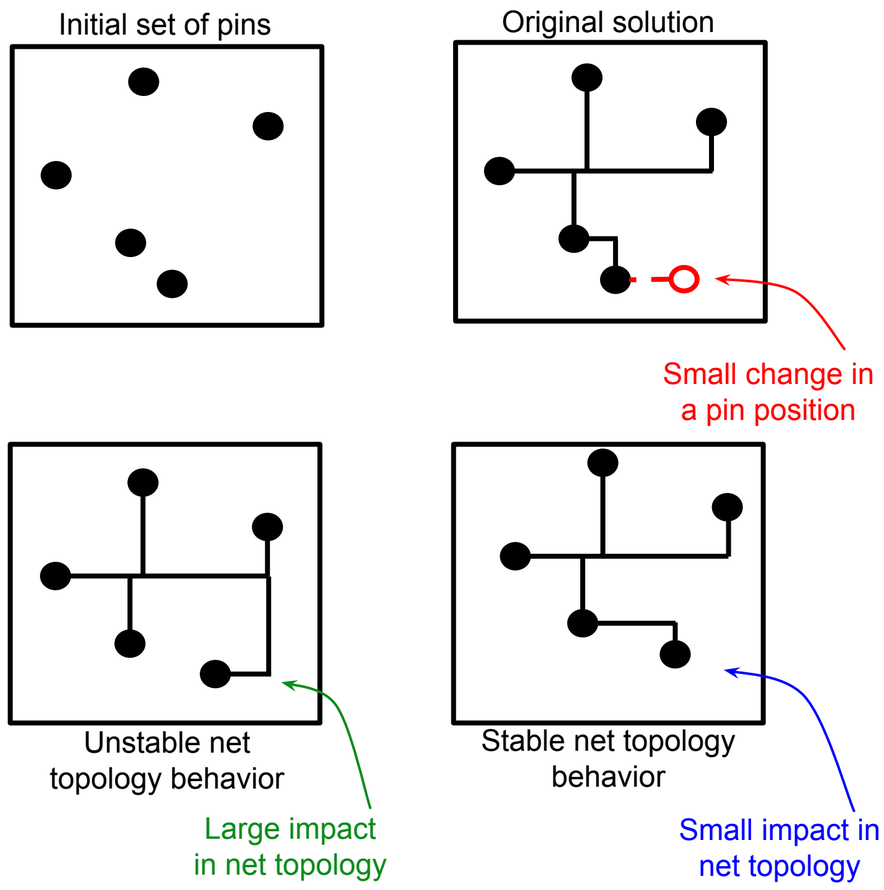
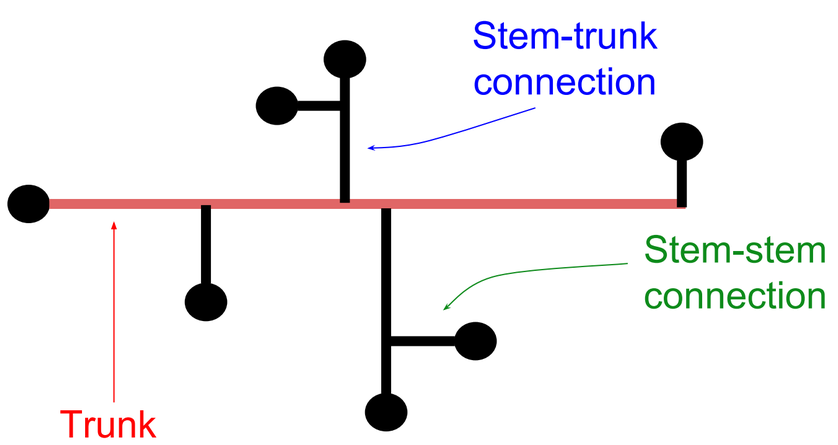
Motivation

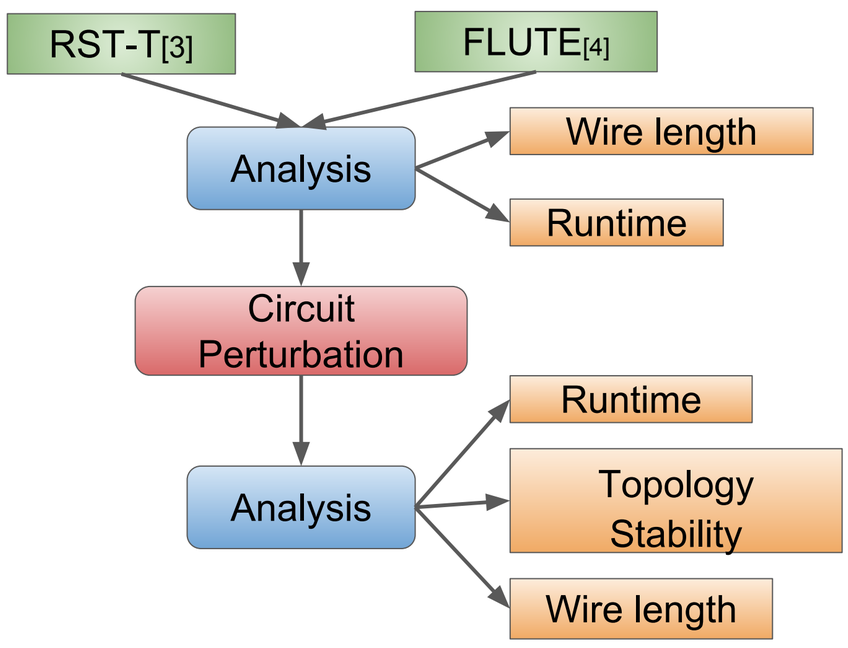


Refined Single Trunk Tree

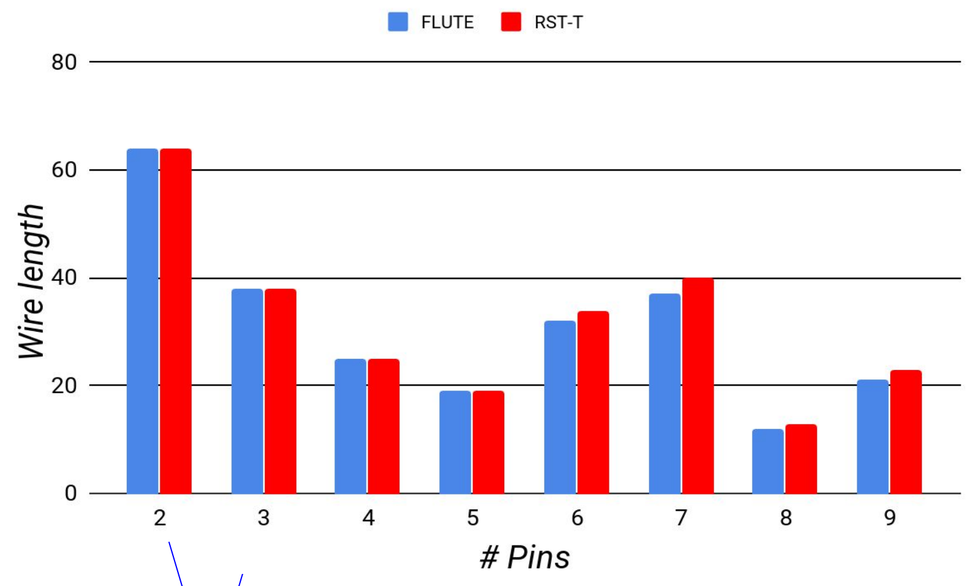


Methodology

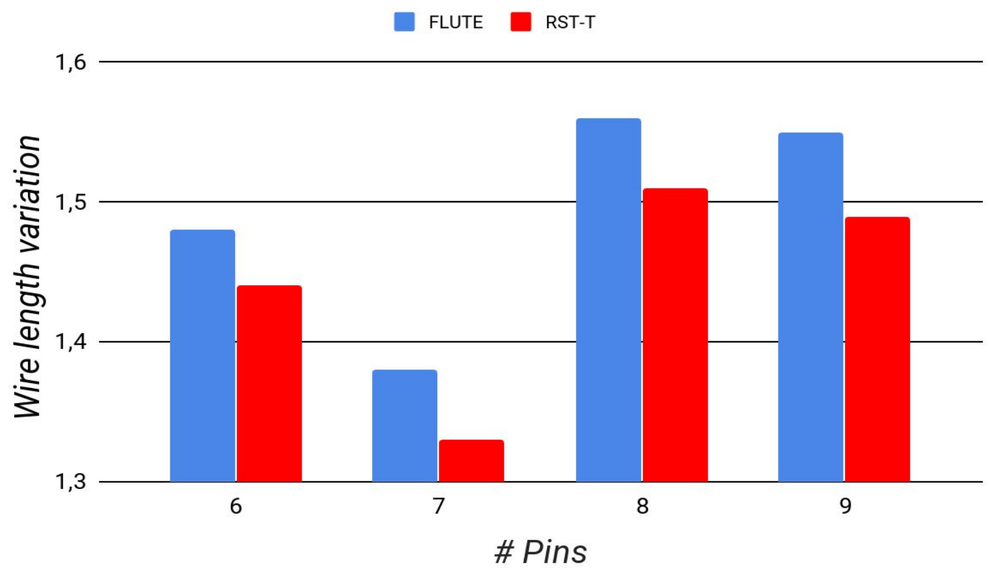
Benchmarks from IWLS 2005 [1]
Synthesized using Nangate 45nm Open Cell Library [2]



Results



> 80% of the nets



Conclusions

FLUTE

- Optimal wire length for nets up to 9 pins
- 0.05 seconds of runtime for the tested circuit

RST-T

- Optimal wire length for nets up to 5 pins
- 0.15 seconds of runtime for the tested circuit
- Wire length variation 6% less in comparison with FLUTE

Future Works: Build tree topology aiming to balance drive-sink delay and consider routability issues.

References

[1]IWLS 2005 Benchmarks, http://iwls.org/iwls2005/benchmarks.html
[2]NanGate, Inc. NanGate 45nm Open Cell Library, http://www.nangate.com/?pageid=2325.
[3]FLUTE: C. Chu and Y. C. Wong, “Flute: Fast lookup table based rectilinear steiner minimal tree algorithm for vlsi design,” IEEE TCAD, 2008.
[4]RST-T: H. Chen, C. Qiao, F. Zhou, and C.-K. Cheng, “Refined single trunk tree: A rectilinear steiner tree generator for interconnect prediction,” in Proceedings of the SLIP, 2002.