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**All-MOSFET M-2M Digital-to-Analog
Converter for Operation with Very Low
Supply Voltage**

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*"If I have seen farther than others,
it is because I stood on the shoulders of giants."*

— SIR ISAAC NEWTON

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ABSTRACT

Since the 80s, development of manufacturing processes in semiconductors industry have sought to reduce supply voltage. The main purpose is to reduce circuits power consumption. The starting point was the old 5 V standard, set by TTL logic in the 70s, until modern circuits that operate with supply voltages below 1 V. However, since the early 2000s, supply voltage is stabilized at this level due to technological limitations difficult to overcome. This challenge has been studied by research groups around the world and several strategies have been proposed to design analog and digital circuits operating with supply voltages far below than 1 V. In fact, these groups have focused their studies on circuits operating with supply voltages lower than 0.5 V, some of them around 200 mV or even less. Among various classes of circuits, digital to analog data converters (DACs) and analog to digital data converters (ADCs) are fundamental circuits for integration process between analog and digital processing modules, thus essential for the implementation of complex SoCs (System-on-a-Chip) nowadays. This thesis presents a performance study over the MOSFET configuration in a M–2M ladder network (similar to the R–2R ladder network that is built with resistors) used as a digital to analog converter, when sized to operate at very low supply voltages (200 mV or less). This study is based on a MOSFET model that is continuous from the condition of weak inversion (subthreshold) to strong inversion, and includes a mismatch model between MOSFETs also valid for any operating condition. Based on this study, a design methodology able to establish trade-offs between “supply voltage”, “effective resolution” and “silicon area” is developed. Electrical simulation results are presented and compared with the analytical results to support the methodology. The circuit has been sent to manufacturing and should start to be tested soon.

Keywords: CMOS analog design, digital to analog converter, low voltage design, mismatch.

Projeto de um Conversor D/A M-2M para operação em baixa tensão de alimentação.

RESUMO

Desde os anos 80 a evolução dos processos de fabricação de circuitos integrados MOS tem buscado a redução da tensão de alimentação, como forma de se reduzir o consumo de energia dos circuitos. Partiu-se dos antigos 5 V, padrão estabelecido pela lógica TTL nos anos 70, até os circuitos modernos que operam com alimentação pouco abaixo de 1 V. Entretanto, desde os primeiros anos da década de 2000, a tensão de alimentação está estabilizada neste patamar, devido a limitações tecnológicas que tem se mostrado difíceis de serem transpostas. Tal desafio tem sido estudado por grupos de pesquisa ao redor do mundo, e diversas estratégias tem sido propostas para se chegar a circuitos analógicos e digitais que operem sob tensão de alimentação bem inferior a 1 V. De fato estes grupos têm focado seus estudos em circuitos que operam com tensão de alimentação inferior a 0,5 V, alguns chegando à casa de 200 ou 100 mV, ou até menor. Dentre as diversas classes de circuitos, os conversores de dados dos tipos digital-analógico (DAC) e analógico-digital (ADC) são circuitos fundamentais ao processo de integração entre os módulos que processam sinais analogicamente e os que processam sinais digitalmente, sendo assim essenciais à implementação dos complexos SoCs (System-on-Chips) da atualidade. Este trabalho apresenta um estudo sobre o desempenho da configuração MOSFET em rede M-2M (similar à rede R-2R que emprega resistores), utilizada como circuito conversor digital-analógico, quando dimensionada para operar sob tensão de alimentação muito baixa, da ordem de 200 mV ou inferior. Tal estudo se baseia no emprego de um modelo para os MOSFETs que é contínuo desde a condição de inversão fraca (subthreshold) até a inversão forte, e inclui o uso de um modelo de descasamento entre MOSFETs que é válido para qualquer condição de operação. Com base neste estudo foi desenvolvida uma metodologia de projeto, capaz de estabelecer as relações de compromisso entre “tensão de alimentação”, “resolução efetiva” e “área ocupada em silício”, fundamentais para se atingir um circuito otimizado. Resultados de simulação elétrica são apresentados e confrontados com os resultados analíticos, visando a comprovação da metodologia. O circuito já foi enviado para fabricação, e deve começar a ser testado em breve.

Palavras-chave: projeto de circuito analógico, conversor D/A, projeto com baixa tensão, descasamento.

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LIST OF ABBREVIATIONS AND ACRONYMS

AC	Alternating Current
ADC	Analog-to-Digital Converter
CMOS	Complementary metal-oxide-semiconductor
CVS	Carrier Velocity Saturation
DAC	Digital-to-Analog Converter
dB	Decibel
DC	Direct Current
DNL	Differential Nonlinearity
DSP	Digital Signal Processing
ENOB	Effective Number of Bits
FDSM	Frequency-to-Digital $\Sigma\Delta$ Modulator
FoM	Figure of Merit
Hz	Hertz
IBM	International Business Machines Corporation
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral Nonlinearity
ITRS	International Technology Roadmap for Semiconductors
LSB	Least Significant Bit
LVT	Low V_T Transistor
MC	Monte Carlo
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor Field Effect Transistor
MSB	Most Significant Bit
NMOS	N-channel MOSFET
Op-Amp	Operational Amplifier
PDK	Process Design Kit

PMOS	P-channel MOSFET
RF	Radio Frequency
SAR	Successive Approximation Register
SVT	Standard V_T Transistor
UICM	Unified Current Control Model
VCO	Voltage-Controlled Oscillator
WCDMA	Wide-Band Code-Division Multiple Access
WLAN	Wireless Local Area Network
ZVT	Zero V_T Transistor

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1 INTRODUCTION

In this chapter will be presented the main subjects that were used as a motivation for this work, like supply voltage reduction on electronic circuits over the years and circuits operating with very low supply voltage. A brief review on the converters evolution over the years related to supply voltage is also performed. We then state the main objectives of this thesis and describe the work structure.

1.1 Power Supply Voltage Reduction in Electronic Circuits

Over the last decades we have observed a spectacular increase in integration density and computational complexity of digital integrated circuits. Advances in device manufacturing technology allow a steady reduction of the minimum feature size such as the minimum transistor channel length realizable on a chip. To illustrate this point we have Fig. 1.1, which presents the evolution of the (average) minimum device dimensions starting from the 60s and projecting into the 21st century.

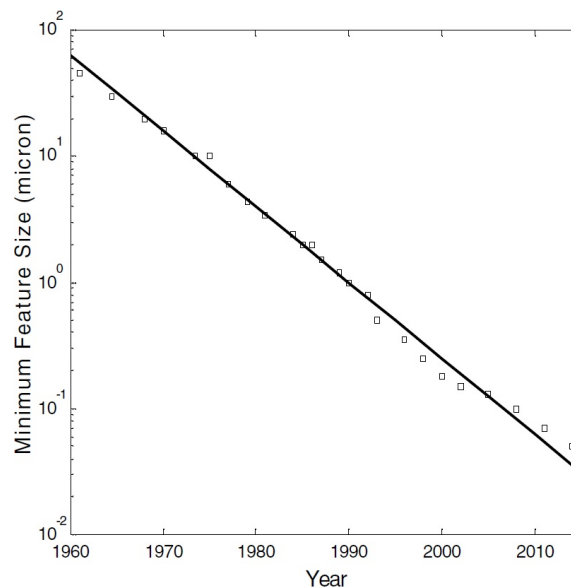


Figure 1.1: Evolution of (average) minimum channel length of MOS transistors over time. Picture taken from RABAEY (2002).

A scaling analysis performed by RABAEY (2002) showed how supply voltage is affected by the scaling process. Different scaling scenarios were presented for short channel devices, full scaling, general scaling and fixed-voltage scaling. In reality, full scaling is

not a feasible option. First of all, to keep new devices compatible with existing components, voltages cannot be scaled arbitrarily. Having to provide for multiple supply voltages adds considerably to the cost of a system. As a result, voltages have not been scaled down along with feature sizes, and designers adhere to well-defined standards for supply voltages and signal levels. As is illustrated in Fig. 1.2, 5 V was the *de facto* standard for all digital components up to the early 90s, and a fixed-voltage scaling model was followed.

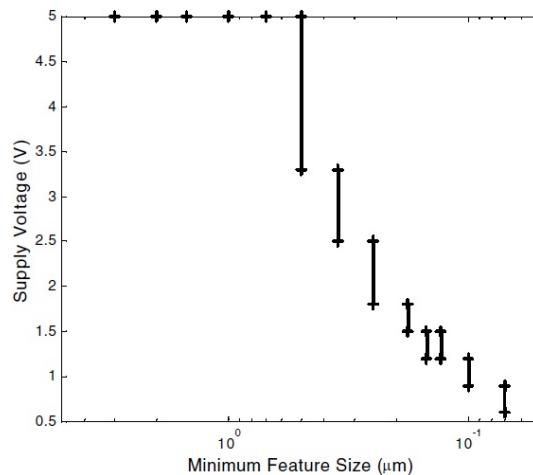


Figure 1.2: Evolution of minimum and maximum supply voltage in digital integrated circuits as a function of feature size. Picture taken from RABAHEY (2002).

With the introduction of the $0.5\mu\text{m}$ CMOS technology, new standards such as 3.3V and 2.5V make an inroad. Nowadays, a closer tracking between voltage and device dimension can be observed with the aid of the fixed-voltage scaling model. The International Technology Roadmap for Semiconductors ITRS (2013) build tables predicting some important features about semiconductor industry. In this case, we are interested in the supply voltage, so, using the fixed-voltage scaling model, the most recent compilation for technology nodes and supply voltages is presented on Tab. 1.1.

Table 1.1: ITRS Summary 2013

Year of Production	2013	2015	2017	2019	2021	2023
Logic Industry "Node Name" Label	"16/14"	"10"	"7"	"5"	"3.5"	"2.5"
V_{dd} (High Performance, high V_{dd} transistors)	0.86	0.83	0.80	0.77	0.74	0.71

The aforementioned analysis provides a wide view of the CMOS technology advancements, which lead us to the next section that presents some electronic circuits operating with very low supply voltage.

1.2 Electronic Circuits for Very Low Supply Voltage

The continuing scaling of CMOS technologies is the main driving factor behind low voltage operation, rapidly achieving sub-1 V supplies for process nodes below 130 nm. Current battery-operated systems require ultra-low current operation, that ranges from a few nanoamperes to a few microamperes, depending on the function being executed. Also future self-powered and self-sustaining electronic systems will require very low voltage operation, since the physical or chemical environmental strategies that can be used for energy harvesting generates from 10's to a few 100's of millivolts RABAHEY et al. (2007).

The energy available is very small, therefore ultra low power design for both computation and communication devices is required. We will now present some circuits and solutions for this topic. With the evolution of MEMS and semiconductor technologies, it is now possible to integrate complete sense, compute and communicate features into ever smaller size factors. This opens the door for ubiquitous deployment, often in hard to reach or unreachable areas. In such cases battery replacement is virtually impossible, and replenishment of the energy supply using harvesting is essential. In recent years, researchers have identified a wide range of harvesting opportunities, and efficient harvesting devices have been developed. Yet, the energy available is still quite small, so ultra low power design for both computation and communication devices is an absolute necessity.

Of course that some complicating issues have to be considered when it comes to the efficient delivery of energy to circuits. The efficiency of the harvester often depends upon operating conditions. For instance: light may not always be available; storage is required if the operational cycles of the harvester and the circuitry are out of phase; voltages and currents delivered by a harvester are often not compatible with the needs of the circuitry. To overcome this issues its common to use the architecture showed on Fig. 1.3.

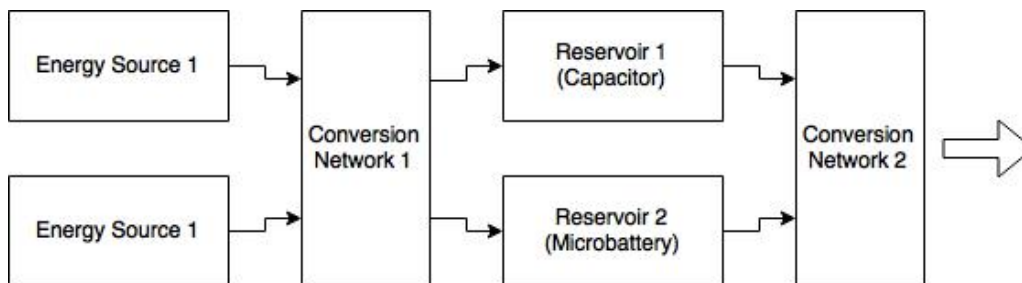


Figure 1.3: Energy Generation and conversion network.

From this diagram we can relate several applications in use nowadays. From motion, solar and thermal energy sources we can gather power through sensors, like showed on Fig. 1.4, and convert it to a temporary energy reservoir. This stored energy can be used to power several kinds of circuits.

We have to keep in mind that energy levels are quite low, so the circuits must have low power consumption. Just to make it clear, the Fig. 1.5 was taken from the Texas Instruments website and presents the estimated energy that can be harvested from different sources.

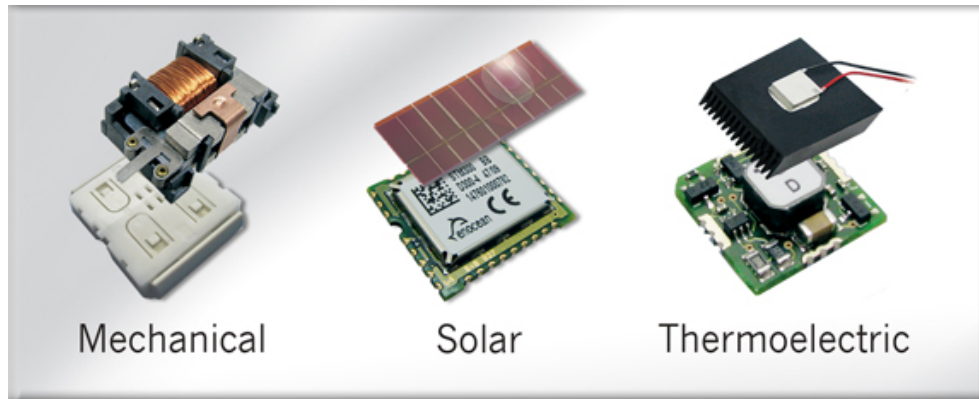


Figure 1.4: Different energy gathering devices.

Energy Source	Harvested Power
Vibration/Motion	
Human	4 $\mu\text{W}/\text{cm}^2$
Industry	100 $\mu\text{W}/\text{cm}^2$
Temperature Difference	
Human	25 $\mu\text{W}/\text{cm}^2$
Industry	1–10 mW/cm^2
Light	
Indoor	10 $\mu\text{W}/\text{cm}^2$
Outdoor	10 mW/cm^2
RF	
GSM	0.1 $\mu\text{W}/\text{cm}^2$
WiFi	0.001 $\mu\text{W}/\text{cm}^2$

Figure 1.5: Energy harvesting estimates, taken from Texas Instruments website TI (2010).

A circuit example that is very interesting is an Intra-Ocular Pressure Monitor (IOPM) device, showed in Fig. 1.6, that was implanted in the eye of a glaucoma patient. This device is presented by CHEN et al. (2011) and uses a custom 1 μAh thin-film Li battery. The lifetime is 28 days with no energy harvesting. To extend lifetime, the device harvests light energy entering the eye with an integrated 0.07mm^2 solar cell and recharges the battery. Given the ultra-small solar cell size, energy autonomy requires average power consumption of less than 10nW. The IOPM achieved a power consumption of 5.3nW and the solar cell supplies up to 80nW ($V_{\text{HARVEST}} = 500\text{mV}$) to the battery on a sunny day. Finally, the circuits requires 10 hours of indoor lighting or 1.5 hours of sunlight per day to achieve energy-autonomy.

All this talk is to reinforce the importance of this work. Low power circuits are undoubtedly one of the most important research areas nowadays.

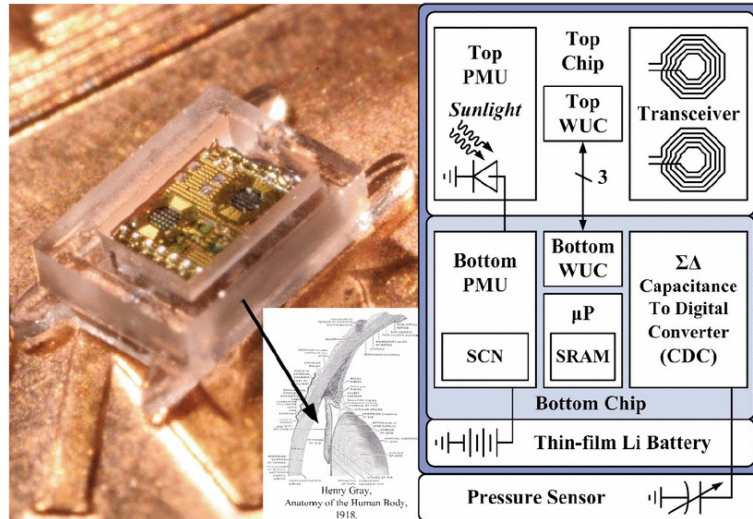


Figure 1.6: The IOPM contains a MEMS pressure sensor, integrated solar cell, and microbattery in a biocompatible enclosure. Its cubic-millimeter size enables implantation through a minimally invasive incision.

1.3 Analog and Digital Signal Converters

Of all circuits that can be study material for low voltage operation this thesis focus on Data Converters. This type of circuit appear on several different applications, like consumer electronics, communications, computing and control, instrumentation, etc.. Data converters emerged back in the 80s as a solution for signal processing. Digital Signal Processing (DSP) proved to be more efficient and replaces several application of analog circuits. The block diagram of Fig. 1.7 shows how to use Analog-to-Digital and Digital-to-Analog Converters.



Figure 1.7: Basic diagram for the use of converters.

Conversion involves quantization of the input, so it necessarily introduces a small amount of error. Instead of doing a single conversion, an ADC often performs the conversions (“samples” the input) periodically. The result is a sequence of digital values that have been converted from a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal. The inverse operation is performed by a digital-to-analog converter (DAC).

Converters performance can be evaluated in several ways. Resolution, supply voltage, sampling frequency, linearity, power consumption and area are usually the main concerns when designing a converter. There are also other concerns linked to the aforementioned, like process technology, that directly affect supply voltage and area, Integral and Differential Nonlinearities (INL and DNL), Effective Number of Bits (ENOB), Total Harmonic Distortion and others.

We will briefly explain the INL and DNL errors that are of vital importance on this

work. The integral nonlinearity error shown in Fig. 1.8 (sometimes seen as simply linearity error) is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a best straight line which is drawn so as to minimize these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. The second method is called end-point linearity and is the usual definition adopted since it can be verified more directly. For an ADC the deviations are measured at the transitions from one step to the next, and for the DAC they are measured at each step. The name integral nonlinearity derives from the fact that the summation of the differential nonlinearities from the bottom up to a particular step, determines the value of the integral nonlinearity at that step TI (1999).

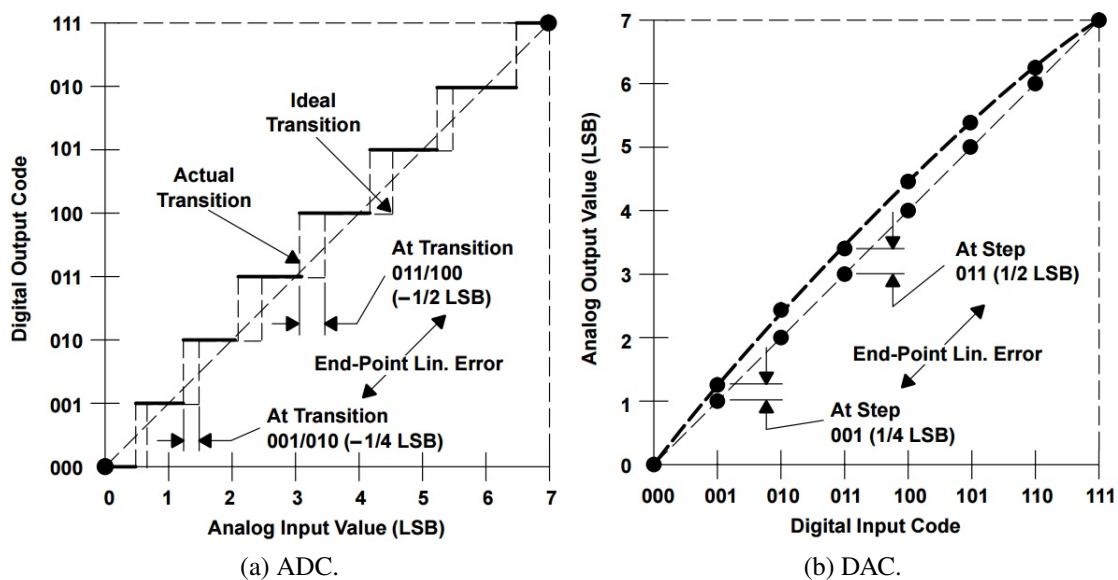
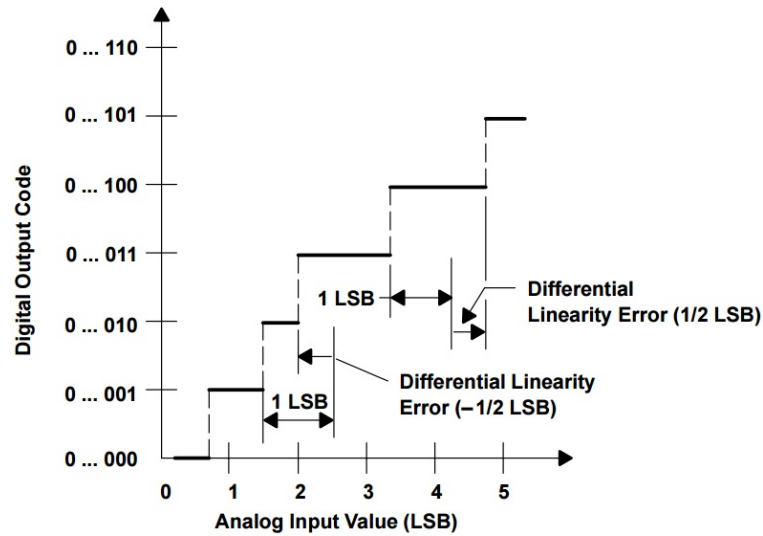
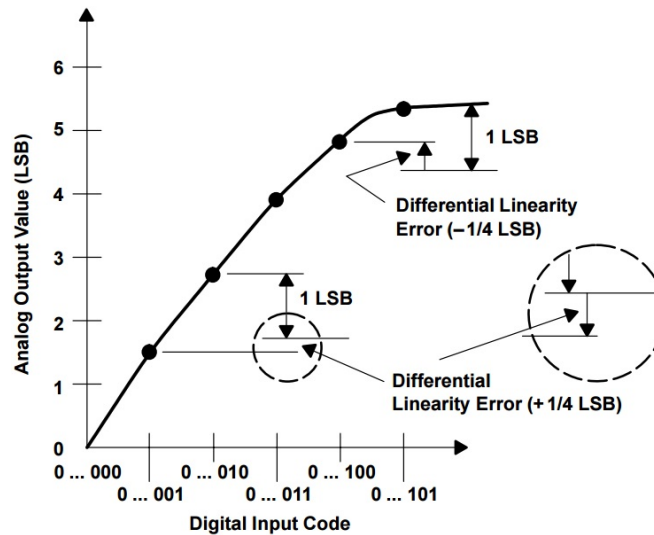


Figure 1.8: Integral Nonlinearity (INL) Error. End-point linearity error of a linear 3-Bit natural binary-coded ADC or DAC. Offset error and gain error are adjusted to the value zero.

The differential nonlinearity (DNL) error shown in Fig. 1.9 (sometimes seen as simply differential linearity) is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB. Therefore if the step width or height is exactly 1 LSB, then the differential nonlinearity error is zero. If the DNL exceeds 1 LSB, there is a possibility that the converter can become non-monotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC there is also a possibility that there can be missing codes i.e., one or more of the possible 2^n binary codes are never output.



(a) ADC.



(b) DAC.

Figure 1.9: Differential Nonlinearity (DNL) Error. Differential linearity error of a linear ADC or DAC.

As pointed out by JONSSON (2010), the supply voltage can vary as much as one order of magnitude within the same node for scientific Analog to Digital converters (ADCs). Figure 1.10 is a scatter plot showing the highest supply voltage applied to each ADC, and the evolution of low-voltage state-of-the-art over time has been highlighted. Since DACs are mainly a vital part of ADCs we can apply the same rule to them.

Recent researches are focusing on low consumption converters for specific applications. The highly digital flash ADC designed by DALY; CHANDRAKASAN (2009) operates on the range of 0.2 V to 0.9 V with 6-bits of resolution. This converter intends to be energy efficient and have a figure of merit (FoM) of 125 fJ/conversion-step at a 0.4 V supply, where it achieves an ENOB of 5.05 at 400 kS/s. It is also important to say that this architecture uses a 5-bits capacitive feedback DAC in order to cancel comparator offsets.

Nowadays, power efficient circuits becomes more and more important. Sensing devices for detecting and monitoring biomedical signals are an example of this kind of circuits. The sensed signals are usually digitized by ADCs with moderate resolutions

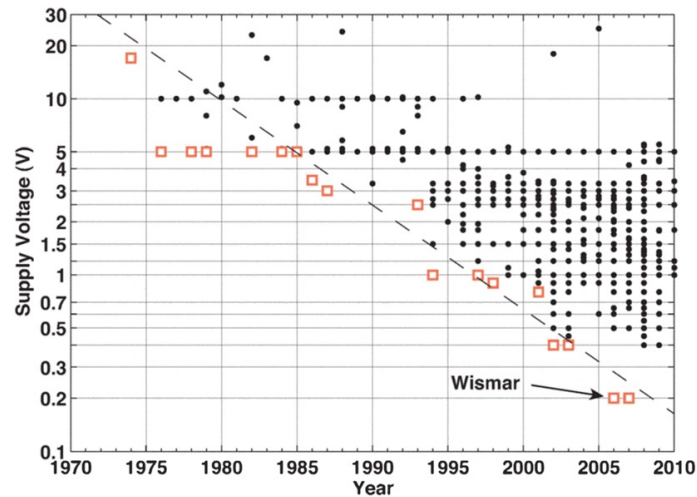


Figure 1.10: Supply voltage for scientific ADCs through the years.

(8 – 12 bits) and sampling rate (1 – 1000 kS/s). Among various ADC architectures the SAR ADC shows a better power efficiency, also benefits from technology downscaling because it mainly consists of digital circuits, which get faster in advanced technologies. LIN; HSIEH (2015) developed a SAR ADC with 0.3 V supply and 10 bits of resolution. They used a merge-and-split switching DAC without common-mode voltage shift in order to reduce the switching energy of the DAC network by 83%. The circuit diagram is presented on Fig. 1.11 and achieved a FoM of 1.78 fJ/conversion-step.

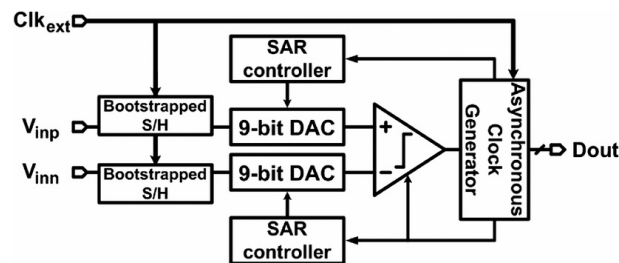


Figure 1.11: SAR ADC architecture. Picture taken from LIN; HSIEH (2015).

1.4 Motivation

We already pointed out the importance of data converters among electronic circuits and also highlighted a strong tendency on low voltage operation. Circuits working under these circumstances usually present new design challenges. This work is focused on Digital-to-Analog Converters, more specifically on the CMOS R–2R ladder that is just a resistor ladder with MOS transistors instead. This particular topology is suitable for low voltage operation because the transistor network current division, that is the base of the digital–to–analog conversion process, is performed with the MOSFETs in the linear region either in strong or in weak inversion (or subthreshold) condition. Throughout this work it is demonstrated a design methodology that establishes trade-offs between resolution, area, sampling speed and supply voltage.

1.5 Organization

This work is organized as follows: a review on the evolution of data converters will be presented on Chapter 2. The MOSFET model used for the circuit design and the all-MOSFET DAC for low voltage supply operation design is done in chapter 3. Post-layout simulation results are presented and discussed in Chapter 4. In Chapter 5 it is exposed the main conclusions and on the appendixes is presented some considerations about mismatch model, a Matlab routine used on the design methodology and the text in Portuguese.

2 DATA CONVERTERS EVOLUTION

There are several strategies for implementing converters using weighting elements that are related to certain electrical quantities such as voltage, current and charge. In Fig. 2.1 we can see four different basic conversion cells.

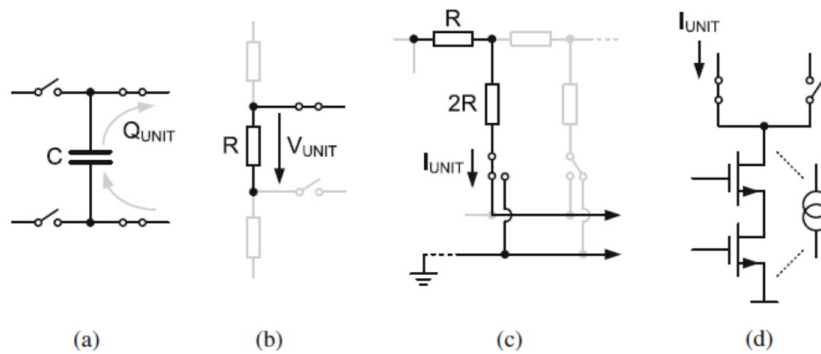


Figure 2.1: DAC unity cell types: (a) charge, (b) voltage, (c) current and (d) current.

Associating the unity cells it is possible to represent quantities in a unary or binary way. This work will focus only on binary weighted current DACs.

2.1 The R–2R binary current divider

Resistor ladder networks provide a simple, inexpensive way to perform digital to analog conversion (DAC). The most popular network is the R–2R ladder, mainly because of its inherent accuracy and ease of manufacture. Fig. 2.2 is a diagram of the basic R–2R ladder network with N bits. The "ladder" portrayal comes from the ladder-like topology of the network. Note that the network consists of only two resistor values, R and 2R (twice the value of R) no matter how many bits make up the ladder. Assume that a voltage-mode ladder connects the most significant bit (MSB) arm to V_{Ref} and all the others to ground. The circuit becomes a R–2R resistive divider of V_{Ref} leading to $V_{Out} = V_{Ref}/2$. If the next left switch is the only one connected to V_{Ref} , the voltage of the corresponding intermediate node results from a $2R - 6/5R$ division of V_{Ref} giving $V_{n-1} = 3V_{Ref}/8$ and $V_{Out} = V_{Ref}/4$. It can be also verified that connecting the next left switch to V_{Ref} leads to $V_{Out} = V_{Ref}/8$ and so forth.

The output of an R–2R ladder in the voltage mode is the superposition of terms that are the successive division of V_{Ref} by 2. For n -bit this gives

$$V_{Out} = \frac{V_{Ref}}{2}b_{n-1} + \frac{V_{Ref}}{4}b_{n-2} + \cdots + \frac{V_{Ref}}{2^{n-1}}b_1 + \frac{V_{Ref}}{2^n}b_0, \quad (2.1)$$

which is the DAC conversion of a digital input $b_{n-1}, b_{n-2}, \dots, b_1, b_0$.

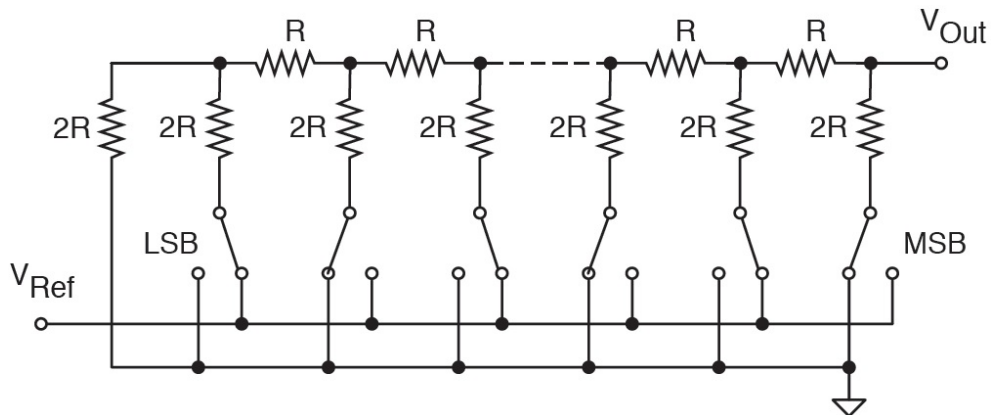


Figure 2.2: R–2R voltage mode ladder network. Picture taken from MALOBERTI (2007)

The resistor ladder is a subject matter since long time ago. One of the first works made with this topology was a 6-bit D/A converter proposed by DOOLEY (1971). In the early 80s, ERB; WIERZBA (1983) and BAPESWARA RAO; RAO (1985), presented methods for determining the resistance output of the ladder. Through the 90s other aspects of the ladder became objects of study, like a reduced physical model of the INL error performed by BONI et al. (1994) and investigations over the impact of different process resistors on the performance of the ladder WITTMANN et al. (1995). Some more complete studies started to appear after that, like in KENNEDY (2000) where he developed a model in terms of the effective resistances at the nodes of the ladder to perform appropriate trimming, design, and test strategies.

2.2 The Current Division Principle

BULT; GEELLEN (1992) noted that two series-connected MOS transistors, with same size and gate voltage (V_g), equally divide the current applied on their common terminal, regardless the voltage applied on other terminals (V_a and V_b) or the operation region. This principle is depicted on Fig. 2.3 where the current I_{in} goes through each transistor M_1 and M_2 with half of its value ($M_1 = M_2$).

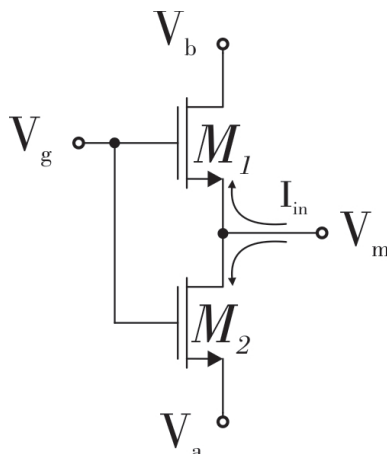


Figure 2.3: Current division principle.

For a better understanding, the similar circuit of Fig. 2.4 shows that a current I_{in} flowing into or out of the circuit will be divided into two parts, in which ΔI_1 flows into V_a and ΔI_2 flows to V_b . The ratio of the two currents is given by

$$\frac{\Delta I_1}{\Delta I_2} = -\frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} \quad (2.2)$$

where ΔI_1 represents the increase in the current that flows through M_1 and ΔI_2 the increase in the current that flows through M_2 , both resulting from the applied current I_{in} . It is also clear that $I_{in} = \Delta I_1 - \Delta I_2$. The two transistors can be viewed as a resistive current divider using nonlinear resistors. The accuracy of current division does not depend on the linearity of the two devices M_1 and M_2 , but only on the matching of their $V - I$ curves. We can use this concept in the resistor ladder network to design a MOS-only digital to analog converter.

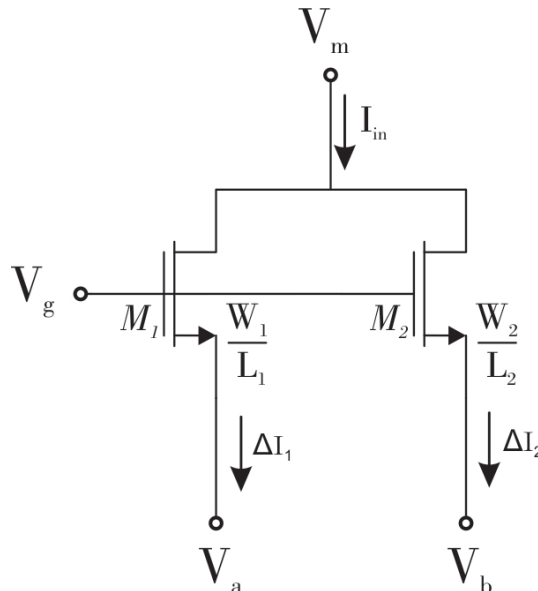


Figure 2.4: Similar circuit showing the current division principle related to the aspect ratios.

2.3 The M-2M Ladder DAC

Although the structure of an R-2R ladder consisting of MOS transistors (M-2M ladder) is similar to the classical resistor-based R-2R ladder, the transistors do not have to emulate identical resistor values. The MOSFET ladder is based on the linear current division principle (previously explained) and its topology is shown in Fig. 2.5.

The resistors in Fig. 2.2 are replaced by unit NMOS transistors operating in the linear region and four unit transistors form the unit cell for 1-bit conversion. Those unit transistors driven by the digital input S_i and \overline{S}_i operate also as switches. Since the division principle works on every operating region, with devices in triode second order effects are reduced and the current mismatch due to threshold voltage mismatch can be controlled by the effective gate-source voltage. Large gate overdrive is normally avoided to reduce the nonlinearity due to mobility degradation, but this is not necessary here since the current division is independent of mobility variations. This is an interesting feature especially for

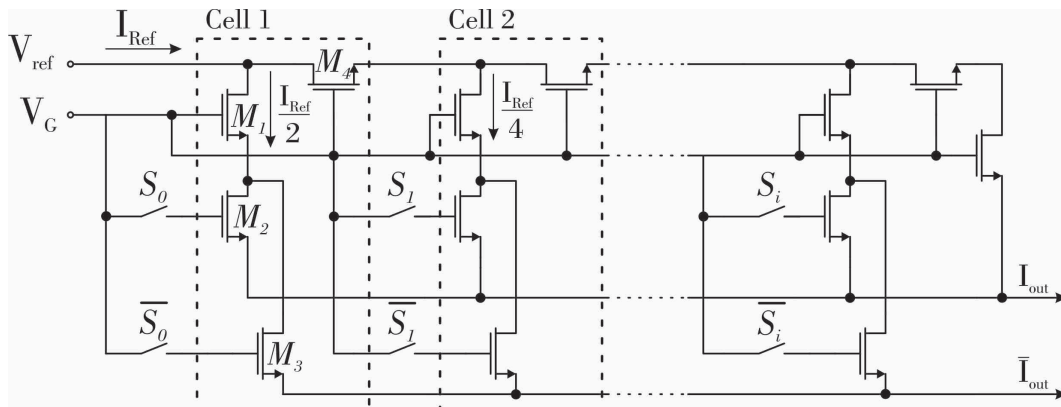


Figure 2.5: M-2M Ladder Network.

deep submicron processes, where the gate oxide becomes very thin and thus the transversal field increases and the surface scattering becomes worse.

2.4 Bibliographic Review

2.4.1 R-2R ladder Review

We already quoted some works about the resistor ladder but none of them says a thing about low voltage that is the main reason of this work. Then, MORTEZAPOUR; LEE (2000) explored the low voltage operation of the resistor ladder on his 1-V, 8-Bit Successive Approximation ADC. He designed the converter on a $1.2\mu\text{m}$ CMOS process, so 1 V of supply can be considered low voltage. The circuit achieved a sampling speed of 50kS/s and the entire ADC including all the digital circuits consumes less than 0.34 mW. The DAC topology that he used is shown in Fig. 2.6 and the strategy for low voltage operation is biasing the negative input terminals of the op-amps using two current sources (I_2) such that the op-amp input common-mode voltages can be set close to ground and the switches can have sufficient overdrive voltages.

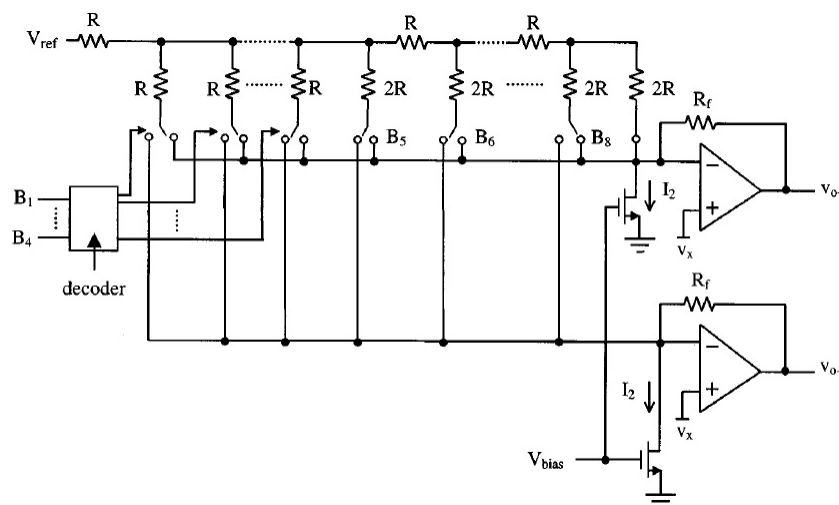


Figure 2.6: Low voltage DAC design. Picture taken from MORTEZAPOUR; LEE (2000).

GREENLEY et al. (2001) faced the downscaling problem designing a 1.8V, 10-bit DAC on a $0.18\mu\text{m}$ CMOS process by mixing segmented current sources with the R-2R

Further works, like WANG; FUKATSU; WATANABE (1998), characterized the current-mode M–2M ladder of the Fig. 2.9 showing that this topology is best suited for low-power operation. To validate their results a D/A converter with 8-bits of resolution was fabricated using a $0.6\mu\text{m}$ CMOS process.

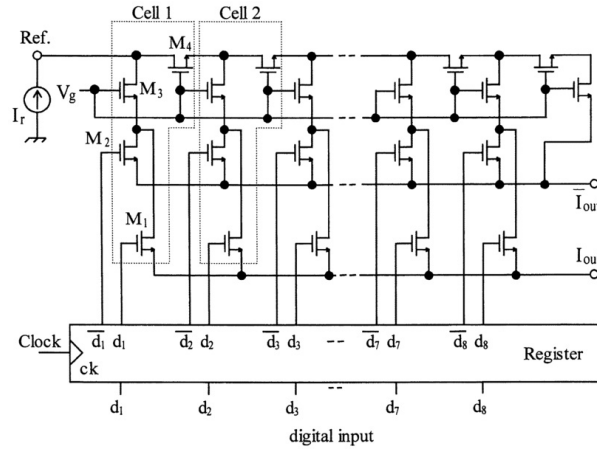


Figure 2.9: Circuit diagram of the 8-bit DAC. Picture taken from WANG; FUKATSU; WATANABE (1998)

In KLIMACH et al. (2008) the same converter was designed using a physical mismatch model on a $0.35\mu\text{m}$ CMOS technology. As can be seen in Fig. 2.10, the circuit is very similar to the one made by WANG; FUKATSU; WATANABE (1998) but the approach was different.

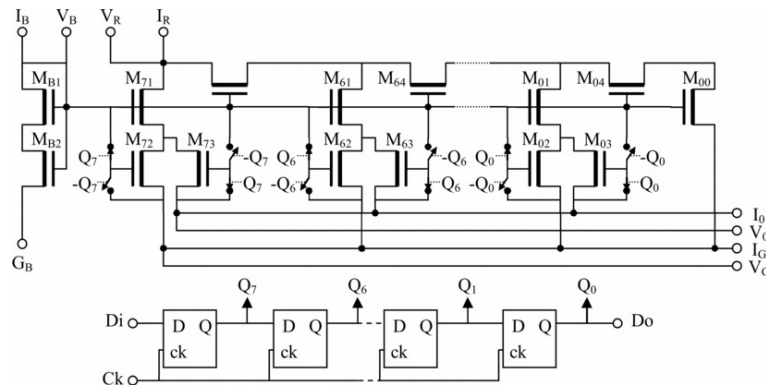


Figure 2.10: Simplified schematic of an 8-bit DAC. The shift register at the bottom is used for the series-to-parallel conversion of the input words. Picture taken from KLIMACH et al. (2008).

This two last circuits are the strong basis of this work, summed with the appropriate MOSFET model (UICM) it is possible to design a M–2M DAC using the mismatch approach. The ladder operates with transistors in triode condition and can also work in subthreshold, being a very promising topology for ULV operation. This possibility was already observed by KVITSCHAL et al. (2012) where they proposed a 6-bit DAC working with 0.1 V in 130 nm CMOS process.

Another very interesting application for the M-2M ladder was exposed by LEE; LIN (2010) exploring a nonlinear topology. They added transistors on the conventional M-2M ladder in order to obtain nonlinear characteristics of the output current. One of the applications of nonlinear DACs is for gamma correction in the driving systems of displays.

2.4.3 Very Low Voltage Converters Review

Until now we made an extensive review of the R-2R and M-2M ladders, but it is also interesting to review what happened to the converters when dealing with very low voltage supplies. From the Fig. 1.10 we can highlight the decrease of the supply voltage through the years showing that designers are always trying to achieve the lowest supply voltages on each technology node.

Lets first point out to the design made by MATSUYA; YAMADA (1994) where the main goal was to design a battery operated converter that has to work with low supply voltages. Until that time the lowest supply was 2.5 V (KUSUMOTO; MATSUZAWA; MURATA (1993)) which wasn't enough for battery operated circuits. To met the low voltage specification they implemented a 10-bits noise shaping ADC that works with 1 V of supply on a $0.5\mu\text{m}$ CMOS process. To accomplish this they used an RC integrator composed by an integrator, a quantizer and a feedback DAC, as shown on the block diagram of Fig. 2.11, in order to solve issues presented by switching capacitors working with low voltage supplies.

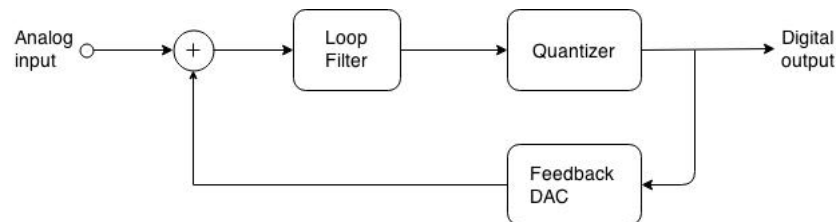


Figure 2.11: Block diagram of a basic noise-shaping A/D converter.

Following this line, PELUSO et al. (1998) reinforced the difficulties of using switching capacitors for low voltage operation and used a switched Op-Amp technique to design a 900mV Low Power $\Sigma-\Delta$ ADC with 10-bits of resolution on a $0.5\mu\text{m}$ CMOS process. They also chose this method to avoid the use of expensive multithreshold processes.

The downscaling of CMOS devices brings up new design possibilities, as well new difficulties. On a $0.13\mu\text{m}$ CMOS process, LIN; HAROUN (2002) designed a 0.8 V/22 MHz Flash ADC with 5-bits of resolution using a nonlinear double interpolation technique. At that time, high data rate converters became an interesting option by integrating a receive converter with digital baseband signal processing circuits (rather than an RF transceiver), as shown in Fig. 2.12. This architecture brings a design challenge because when converters are integrated on the digital baseband chip they need to be protected from the large digital noise.

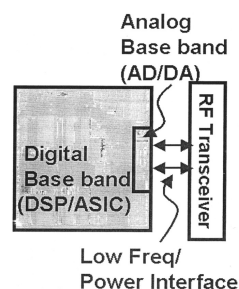


Figure 2.12: Typical baseband and RF transceiver configuration in wireless devices back in 2002, e.g., WCDMA, WLAN. Picture taken from LIN; HAROUN (2002).

SAUERBREY et al. (2003) designed a Successive Approximation (SAR) ADC with 0.5 V and 8-bits of resolution on a $0.18\mu\text{m}$ CMOS process. In this work they pointed out that switched opamp circuits, reset-opamp circuits and circuits using bootstrapping techniques are suited for low V_{DD} but presented another approach where only reference voltages are switched. The SAR architecture shown on Fig. 2.13 is opamp-free with a passive sample-and-hold (S & H) stage and a capacitor based DAC.

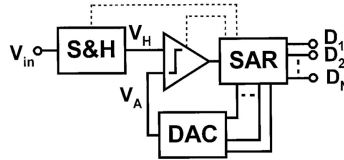


Figure 2.13: Successive approximation converter architecture. Picture taken from SAUERBREY et al. (2003).

The last state-of-art design that JONSSON (2010) mentioned was a Frequency-to-digital $\Sigma\Delta$ modulator (FDSM) made by WISMAR et al. (2006). They use an inverting voltage controlled oscillator (RVCO) as the integrator. The block diagram is shown in Fig. 2.14 and works with 0.2 V in a 90nm CMOS process.

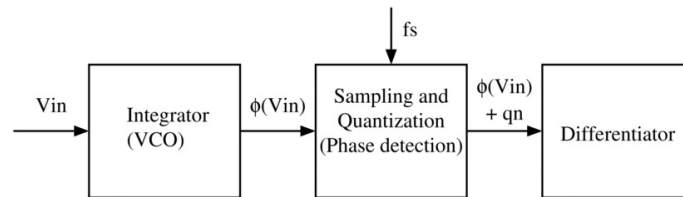


Figure 2.14: FDSM block diagram. Picture taken from WISMAR et al. (2006).

Two other works that fit in here were already quoted in section 1.3 (DALY; CHANDRAKASAN (2009) and LIN; HSIEH (2015)) to support the importance of ultra low voltage converters. To reinforce, we will quote now two recent works made by Chandrakasan and his colleagues that are state-of-art ADCs. In LEE; CHANDRAKASAN; LEE (2012), they developed a 12-bits 5 to 50 MS/s on the range of 0.5 to 1 V, voltage scalable zero-crossing based pipelined ADC. The circuit was manufactured on a 65 nm CMOS process and enables energy efficient operation. It uses switched-capacitor multiplying DACs (MDACs). The other work, YIP; CHANDRAKASAN (2013), is a resolution-reconfigurable, 5 to 10 bits, 0.4 V to 1 V, Power Scalable SAR ADC for sensor applications. This ADC features a reconfigurable 5 to 10 bits DAC whose power scales exponentially with resolution. The ADC operates up to 2 MS/s at 1 V and 5 kS/s at 0.4 V. Prototyped in a low power 65 nm CMOS process, the ADC in 10-bit mode achieves an INL and DNL of 0.57 LSB and 0.58 LSB respectively at 0.6 V, and the Nyquist SNDR and SFDR are 55 dB and 69 dB respectively at 0.55 V and 20 kS/s. From the two common DAC approaches, resistive DACs (RDACs) and capacitive DACs (CDACs), they chose the CDAC approach because it is more amenable to voltage scaling

3 LOW VOLTAGE ALL-MOSFET DAC

From the previous chapters we get the main ideas in order to design a Digital-to-Analog Converter that works with very low supply voltage. We want low voltage operation because it is ubiquitous among every circuits nowadays and the M–2M ladder topology proved to be suited for this specification. Through this chapter we perform a circuit description showing the schematic and explaining the operation regime. The design methodology based on the UICM Mismatch model and operation principles are shown in sequence. We also point out that some linearity issues, that might become a problem, are actually easy solvable problems.

3.1 The All-Regions UICM MOSFET Model and Mismatch Model

The Unified Current Control Model (UICM) SCHNEIDER; GALUP-MONTORO (2010), is a physics-based all-region MOSFET model that uses the “inversion level” concept, and it provides the modeling foundation for the analytical formulation used by KLIMACH et al. (2008). This model represents the drain current of a transistor as the difference between a forward (I_F) and a reverse (I_R) component

$$I_D = I_F - I_R = I_{SQ} \frac{W}{L} (i_f - i_r) \quad (3.1)$$

where $I_{SQ} = \frac{1}{2} \mu C'_{ox} n \phi_t^2$ is the sheet normalization current, (W/L) the aspect ratio, n is the slope factor, μ is the low field mobility, C'_{ox} the oxide capacitance per unit of area and ϕ_t is the thermal voltage. Parameters i_f and i_r are the normalized forward and reverse currents, or “inversion levels”, at source and drain, respectively.

The “ideal” slope factor (n) is equal to one. The bulk MOS transistor, however, is characterized by a slope factor a few percent to tens of percent higher than one. The deviation from ideal slope factor in bulk transistors happens because the change in gate voltage is not only accompanied by a change in the inversion charge but also by a change in the bulk charge SCHNEIDER; GALUP-MONTORO (2010).

The forward and reverse inversion levels are also related to the terminal voltages as follows

$$V_G - V_T - nV_{S(D)} = n\phi_t \left[\ln \left(\sqrt{1 + i_{f(r)}} - 1 \right) + \sqrt{1 + i_{f(r)}} - 2 \right] \quad (3.2)$$

where V_G , V_S and V_D are the gate, source and drain voltages referred to bulk, respectively, and V_T is the threshold voltage.

The MOSFET mismatch model based on the UICM model, used as basis of KLIMACH et al. (2008) work, was previously proposed by GALUP-MONTORO et al. (2005),

being more appropriate to the DAC variability analysis than the traditional Pelgrom's mismatch model, that does not consider the subthreshold nonlinear nature of MOSFETs in a proper way. In appendix B there's a comparison between the two models, explaining a little better their differences.

The following equation presents the dependency of current mismatch with transistor area, inversion levels and technology parameters

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{1}{WL} \left[\frac{N_{oi}}{N^{*2}} \frac{1}{i_f - i_r} \ln \left(\frac{1 + i_f}{1 + i_r} \right) + B_{I_{SQ}}^2 \right] \quad (3.3)$$

where $N^* = nC'_{ox}\phi_t/q$ is the carrier density at pinch-off condition, N_{oi} is the main mismatch model parameter, related to the number of impurity atoms inside the depletion volume under the channel area, and $B_{I_{SQ}}$ is a less significant model parameter that accounts for variations in the specific normalization current I_{SQ} .

3.2 The Binary Weighting Principle

For a long-channel MOSFET under any bias condition, the drain current is directly proportional to the channel width (W), and inversely proportional to its length (L). Based on this statement, one can show that any series-parallel association of identical transistors (Fig. 3.1) works similarly to one device with equivalent aspect ratio (W/L) KLIMACH et al. (2008). Assume $M = M_a = M_b = M_c = M_d$ in Fig. 3.1.

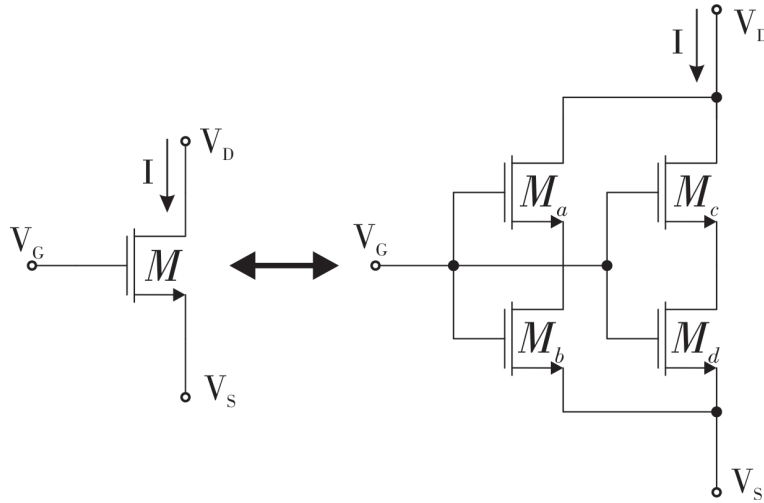


Figure 3.1: MOSFET association principle: one transistor can be substituted by a series-parallel association of identically designed transistors.

Using this association principle, transistor M_d in Fig. 3.1 can also be substituted by a series-parallel association of identical transistors, M_{da} , M_{db} , M_{dc} and M_{dd} , resulting the circuit in Fig. 3.2. Since the main branches in Fig. 3.2 are equivalent, the applied current I is equally divided between them. The same current division principle can be used in secondary branches. One can see that it is rather simple to establish a binary division of currents that flow through different branches of a series-parallel association of MOSFETs.

Transistor M_{dd} of 3.2 can also be substituted by another set of four transistors in series-parallel association, resulting in another binary division of the current. This procedure can be repeated successively, resulting in the network traditionally called the “M–2M ladder”.

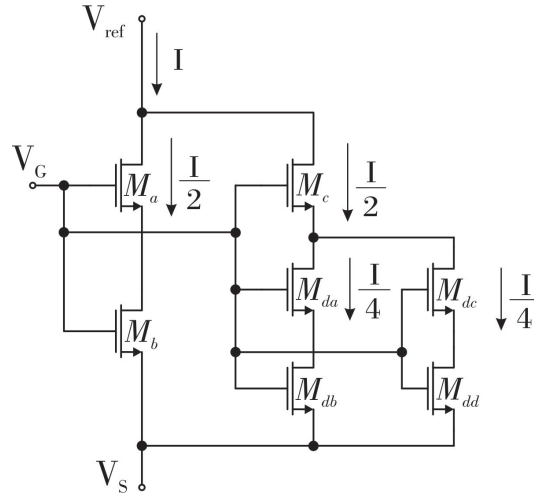


Figure 3.2: M_d in Fig. 3.1 can be substituted by a series-parallel equivalent association.

3.3 DAC Circuit Description

The ladder network shown in Fig. 3.3 is formed by a sequence of M–2M cells, one per bit, and finalized by a 2M termination. In general this ladder is formed by cells with transistors having the same geometry, simplifying the layout. Each cell divides its input current by half, performing the DAC weighting through successive binary divisions of the reference current I_{Ref} generated by V_{Ref} . The two drain connected transistors M_2 and M_3 deviates the binary fraction of the current to I_{out} or \bar{I}_{out} node, depending on the S_i switch state, since these nodes are tied to ground through a very low impedance connection, resulting for any binary combination that

$$I_{Ref} = I_{out} + \bar{I}_{out} \quad (3.4)$$

The switches are implemented with transmission gates driven by a digital register that stores the input binary data. At this work we do not explore the register design since our main focus is the ladder variability analysis, that's why the register operates at nominal supply (1.2V). Digital circuits like logical gates and registers operating with very low supply voltages have already been studied in recent works MELEK et al. (2014).

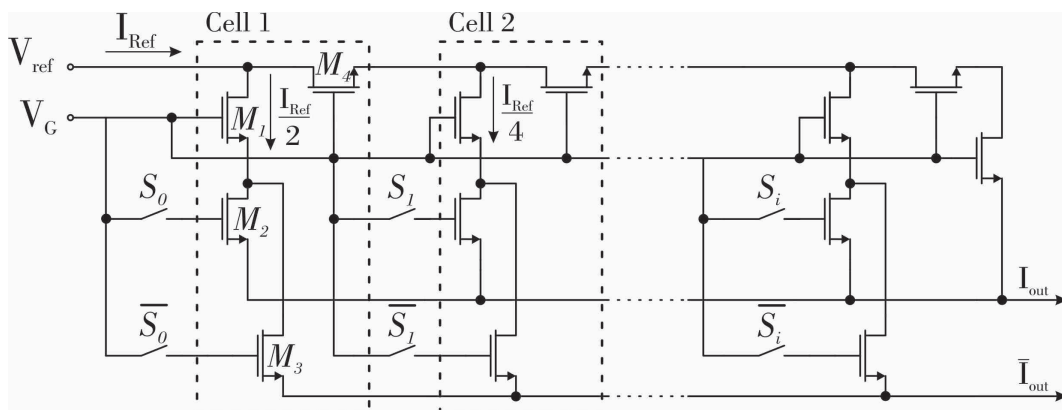


Figure 3.3: M–2M CMOS Ladder Network.

Finally, the current summing that results in I_{out} node represents a binary proportion of I_{Ref} , controlled by the input digital data. The four identical MOSFETs on each cell results a very regular and compact layout that improves matching.

3.3.1 Intrinsic Nonlinearity Considerations

The MOSFET DAC ladder topology can be symmetric or asymmetric, both exemplified in Fig. 3.4. Because the reduced number of transistors the asymmetric topology is most commonly used. However, this circuit presents an intrinsic nonlinearity that even not being the focus of this work it's important to make a few comments. As usual in the design of M-2M ladders, all transistors were designed with same size.

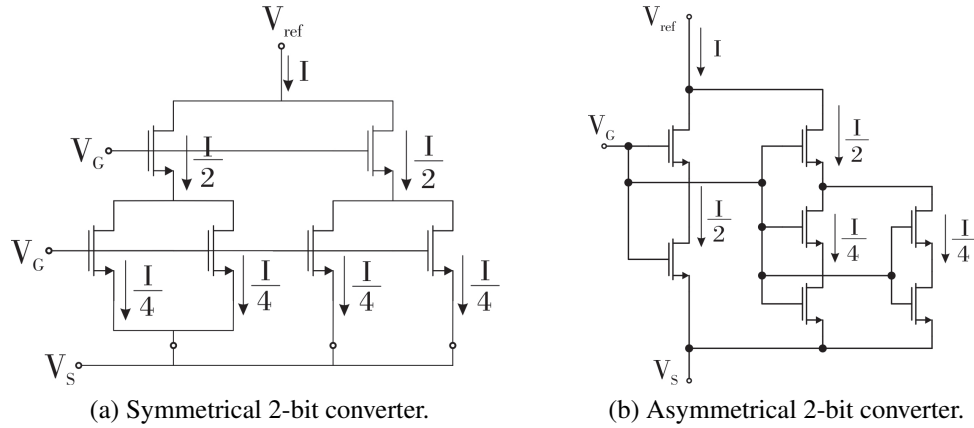


Figure 3.4: Different implementations of a M-2M ladder.

As a proof of concept we simulated on Cadence-Virtuoso tool the 4-bit asymmetric ladder showed in Fig. 3.5 with $V_G = V_{Ref} = 200mV$ and transistors size according to table 3.1. We kept the channel length equal for simplicity and since this is just a proof of concept we choose the sizes by trial and error. In this case we are not worried about the current magnitude, but we must assure that the current value on main branch (M_1 and M_2) is lower than on the other branches. This way the nonlinearity error, which is bigger on the main branch, will have less impact.

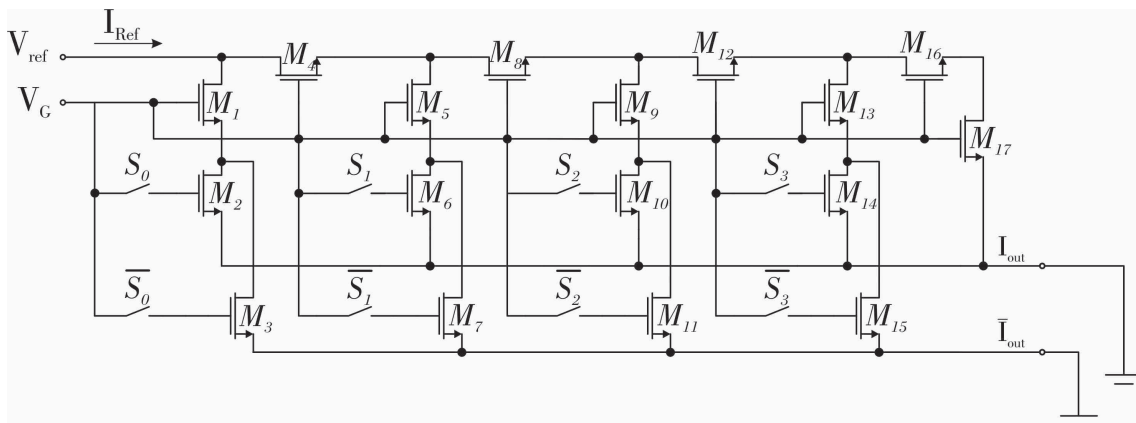


Figure 3.5: 4-bit M-2M ladder for nonlinearity analysis.

The Integral Nonlinearity (INL) was calculated in terms of the least significant bit (LSB). At first, all transistors have the same size and the INL appear by the name “Original INL” in Fig. 3.6, as can be seen, the higher nonlinearity appears at half scale. Then we applied one technique to reduce the nonlinearity by gradually decreasing the transistors size from the LSB to the most significant bit (MSB). The result is shown in the same

Table 3.1: Transistors width (W). The channel length is the same for all $L = 2\mu m$.

Transistors	Original Width	Reduced Width
M_1, M_2, M_3	$4\mu m$	$3.85\mu m$
M_4, M_5, M_6, M_7	$4\mu m$	$3.9\mu m$
M_8, M_9, M_{10}, M_{11}	$4\mu m$	$3.95\mu m$
$M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}$	$4\mu m$	$4\mu m$

figure by the name of “Reduced INL”. Another option to reduce the nonlinearity is using the symmetrical ladder topology, that is perfectly linear.

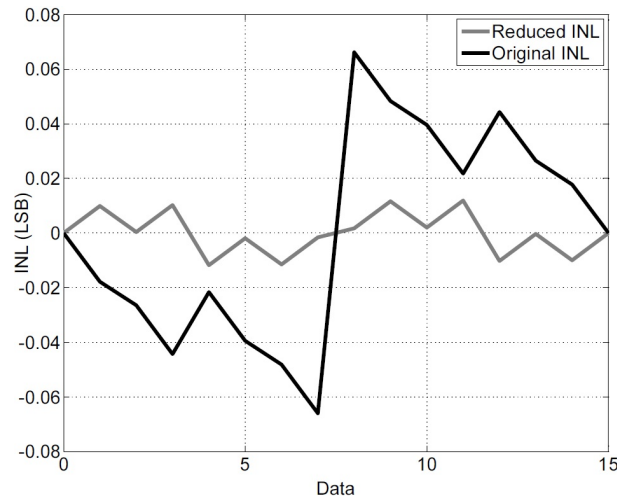


Figure 3.6: INL comparison between an asymmetric ladder with same sized transistors and with INL reduction technique.

The reader must note that this simulation was performed only with typical transistors and this error is not related to any variability issue, being it an intrinsic nonlinearity related to the asymmetrical MOSFET DAC topology. Also, a predistortion can be applied to the input data to correct this nonlinearity, since it is a predictive behavior. To summarize, there are options to mitigate the intrinsic nonlinear behavior of the asymmetric ladder used in this work. This issues will appear on development of this thesis and will be pointed out, but we want to make it clear that our focus is only the variability analysis caused by mismatch of MOSFETs.

3.4 Circuit Design Methodology

The analysis of the resulting inversion levels of transistor terminals that are connected to the ladder nodes can be done using a simplified version with only 2 bits of resolution, as shown in Fig. 3.7, where i_f and i_r are the inversion level of transistors source and drain terminals, respectively. Note that all transistors have same gate biasing, and since the lower transistors of the ladder have also same source biasing, they present same i_f level. Since the current in series transistors M_a and M_b is the same, having both same geometry, from eq. (3.1) one can state the following relationship for the intermediate inversion level i_1

$$i_1 = \frac{i_f + i_r}{2} \quad (3.5)$$

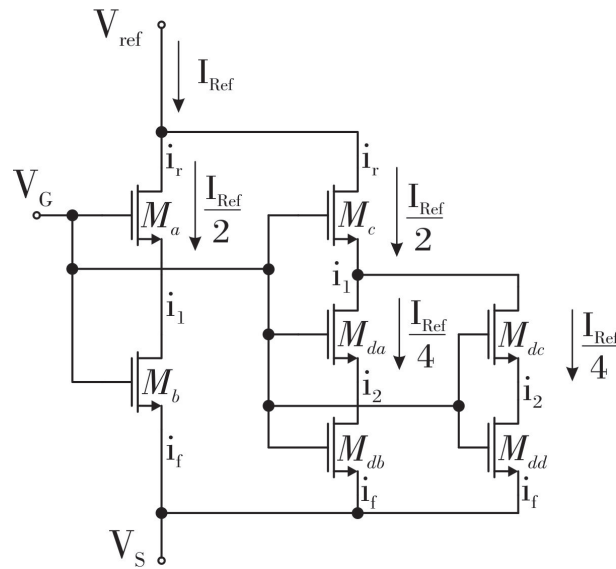


Figure 3.7: Simplified 2-bit DAC and current division process.

Also, since the input current I_{Ref} is divided in two equal portions by equally sized transistors (M_a and M_c), the inversion level on source terminal of these transistors must be the same (i_1). This analysis can be done in the next cell (formed by M_{da} , M_{db} , M_{dc} and M_{dd}), resulting that the inversion level of the intermediate node (i_2) is given by

$$i_2 = \frac{i_f + i_1}{2} \quad (3.6)$$

Expanding this analysis one can determine the intermediate inversion level (i_i) for any branch i of the ladder from i_f (determined by V_G) and i_r (determined by V_{Ref}) using the following expression

$$i_i = \frac{i_r + (2^i - 1)i_f}{2^i} \quad (3.7)$$

From this point a variability analysis can be performed over the ladder using a small-signal model, since the drain current mismatch in the branches can be considered small. Using eq. (3.3) and the forward and reverse inversion levels of the lower transistors of the ladder (M_2 , M_5 and M_8 in Fig. 3.8), one can estimate the mismatch statistical contribution of these transistors in the current flowing in each branch (in Fig. 3.8 the drain current mismatch contribution of M_5 is indicated as σ_{ID}).

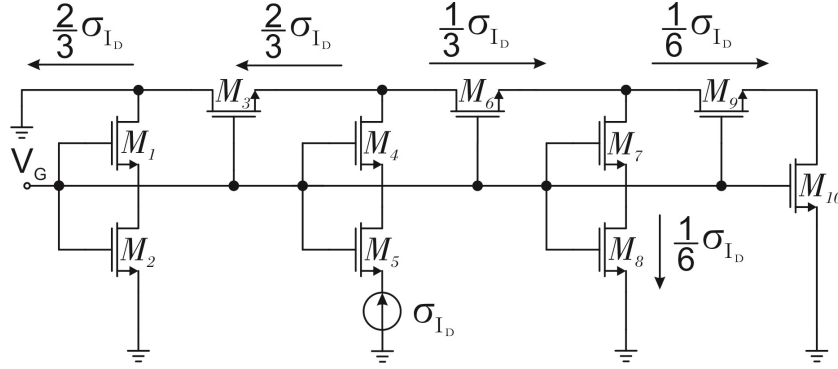


Figure 3.8: Small-signal model for mismatch analysis.

After that, the mismatch contribution of each branch can be propagated to the other branches following the relationship given by Eq. 2.2, using the small-signal approximation and considering the current division property of the MOS transistors BULT; GEELEN (1992). Finally, the contributions from the mismatch of all lower transistors can be combined in each branch to keep the total current equal to the reference current, resulting in an approximation of the drain current error, which can be used to estimate the DAC variability.

For example, in Fig. 3.8 the M_5 mismatch error σ_{I_D} propagates through M_3 and M_6 , according to the current division properties of both branches, the equivalent aspect ratio of transistors $M_6, M_7, M_8, M_9, M_{10}$ is $\frac{W}{2L}$ and M_1, M_2, M_3 is $\frac{W}{L}$. Again, from equation 2.2, the contribution that flows through M_6 is $\sigma_{I_D}/3$, through M_3 is $\frac{2}{3}\sigma_{I_D}$ and through M_8 is $\sigma_{I_D}/6$.

Now we will exemplify the design methodology considering a 130 nm standard process and applying it to a 3-bit DAC explaining in detail every step. We are using the IBM 130 nm process technology because its a very reliable process, also because we have access to it through the university. Another good reasons to use it is the variety of transistors and devices that can be found. From the circuit in Fig. 3.9, we assume $V_G = V_{ref} = 200mV$ and $\frac{W}{L} = \frac{25\mu m}{10\mu m}$. From Eq. 3.2, with $n = 1.35$ (that is a common value when using MOSFETs with less than 500mV of biasing SCHNEIDER; GALUPMONTORO (2010)), $\phi_t = 26mV$ and $V_T = 200mV$, we can calculate i_f of transistors M_2, M_5, M_8 and M_{10} , which value is 4.8. From the same equation, i_r of transistor M_1 is 0.002. Using Eq. 3.7 and the corresponding values of i_f and i_r it is possible to calculate the intermediate inversion levels i_1, i_2 and i_3 , which values are 2.4, 3.6 and 4.3 respectively.

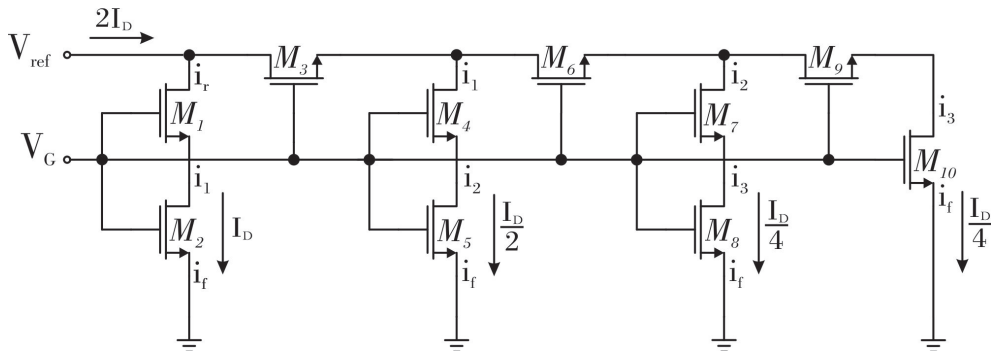


Figure 3.9: 3 bits DAC topology. This circuit

Now that we have all inversion levels, from Eq. 3.1, using $I_{SQ} = 243.7nA$, one can calculate the currents on each branch. The currents flowing through M_2 , M_5 , M_8 and M_{10} are $1.48\mu A$, $744nA$, $372nA$ and $372nA$ respectively.

The next step is to calculate the current mismatch on each transistor given by Eq. 3.3. Mismatch parameter $B_{I_{SQ}}$ has the same meaning of parameter K_β that can be obtained from the process PDK (3% - μm for the IBM 130 nm process). Since parameter N_{oi} is related to a new MOSFET mismatch model it is not usually estimated by foundries and should be measured from fabricated test mismatch structures as shown in KLIMACH; GALUP-MONTORO; ARNAUD (2005). An easier way to estimate N_{oi} is from the following approximate equation that establishes the relation between this parameter and the Pelgrom's mismatch A_{V_T} model parameter, that is related to the threshold voltage mismatch (KLIMACH (2008)), resulting $N_{oi} = 7 \cdot 10^{13} cm^{-2}$ for this process.

$$\sqrt{N_{oi}} = \frac{C'_{ox} A_{V_T}}{q} \quad (3.8)$$

Solving equation 3.3 for σ_{I_D} we find the standard deviation of current, given by mismatch, on each branch. The respective values are $16.9nA$, $7.9nA$, $3.8nA$ and $3.8nA$ and represents the average variations that can occur. The sensitivity of each branch follows the explanation given in Fig. 3.8. Like for instance, the increase of $7.9nA$ on branch $M_4 - M_5$ results on a decrease of $1.66nA$ on branch $M_7 - M_8$. The same happens with all variations following the relationship given by Eq. 2.2, and the effect of each one is added using the superposition theorem.

3.5 Design Space Exploration

We implemented in MatLab a tool that can estimate statistical error of an M–2M DAC, in terms of standard deviation of the output current (σ_{Err}), when related to the ideal linear behavior, showing this error already in LSB (related to the intended resolution). Details about the code can be found in appendix C. The estimated error is performed for a given bias (V_G and V_{Ref}), resolution (depth of the ladder), and transistors size (W and L).

The Matlab routine creates a sample space of choosable size with standard deviation σ_{I_D} and zero mean. This way we can evaluate the sensitivity of each branch, as explained in last section, and sums with the average current (I_D). Fig. 3.10 shows the average current for each data and its linearization in terms of minimum and maximum values. In this particular case we used $V_G = V_{Ref} = 200mV$, $\frac{W}{L} = \frac{25\mu m}{10\mu m}$ and 6-bits of resolution.

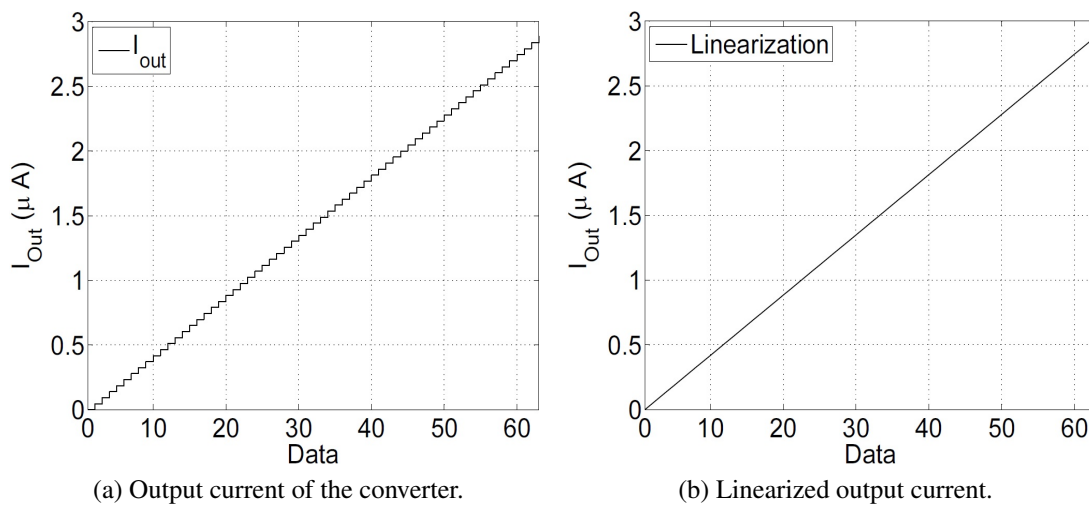


Figure 3.10: Analytical behavior using Matlab.

For each sample created and summed with average current we calculate the difference between each I_{out} and its linearization. As a result we have the Integral Nonlinearity (INL) shown in Fig. 3.11. The result is close to the one generated by Virtuoso Monte Carlo (MC) simulation.

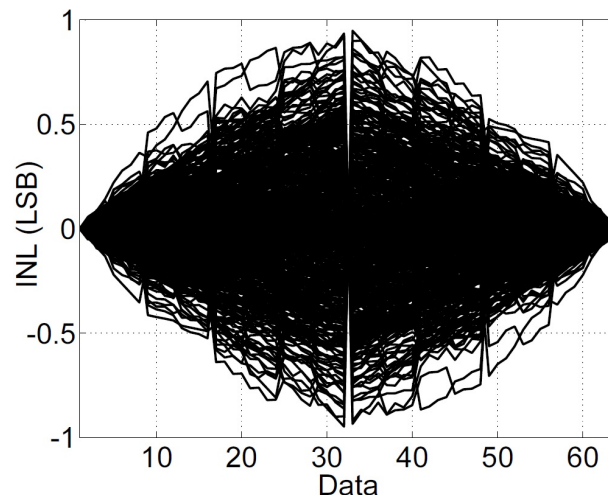


Figure 3.11: Integral Nonlinearity of 500 samples analytically performed in Matlab.

Now, if we calculate the standard deviation of INL we will have the parameter $\sigma_{Err}(LSB)$ showed in Fig. 3.12, that is widely used in this work.

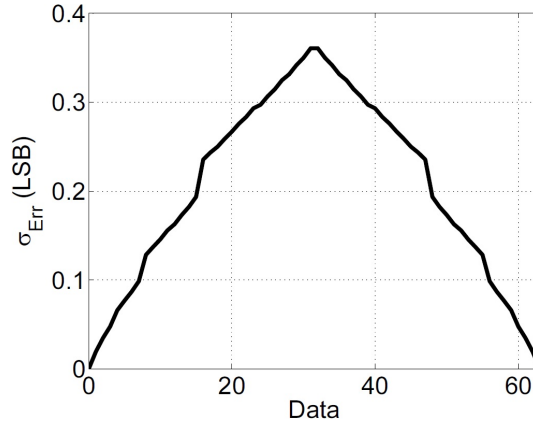


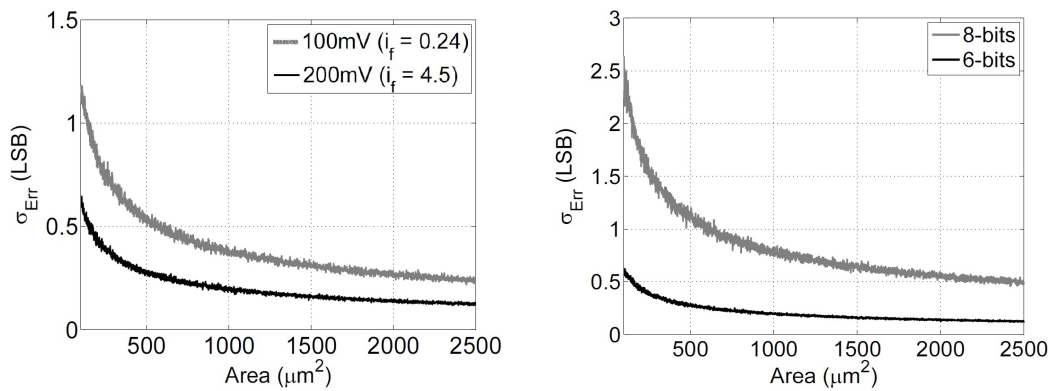
Figure 3.12: Statistical error in terms of the standard-deviation of the output current.

When considering a normal distribution sample, the reliability of the statistical parameters (mean and standard deviation) is related to the sample size (N) from the following approximate equation.

$$Reliability = \frac{1}{\sqrt{N}} \quad (3.9)$$

In the following simulations we are using $N = 500$ samples, resulting an approximate error of 4,4% in the statistical calculation.

To create an useful design space we developed another routine that plots the $\sigma_{Err}(LSB)$ as a function of the transistor area, the result is depicted on Fig. 3.13. We showed this result for two different biasing on Fig. 3.13a and for different resolutions on Fig. 3.13b. We are considering the active area of individual transistors on calculations. To estimate the total converter area we can just multiply the individual transistor area by the number of transistors. For example, a 6-bits converter have 4 transistors in each cell plus 2 in its termination. It is a good idea consider an increase of 10% in the total area for dummy structures, routing and auxiliary devices.



(a) Different biasing voltages for a converter with 6 bits of resolution.

(b) Different resolutions with 200 mV of biasing.

Figure 3.13: Standard deviation of the M–2M DAC error as a function of the transistor area.

3.6 Channel Length Determination

Another important point for this design is to choose a minimum channel length that mitigates the *carrier velocity saturation* (CVS) effect. This effect becomes significant when the channel length is reduced to such an extent that the carrier velocity is no longer proportional to the longitudinal electric field. To reduce the impact of this effect, we should either operate any transistor far from saturation or choose L large enough such that the CVS phenomenon is made insignificant, even when the transistors saturate. One can note that only the transistors connected to V_{Ref} are prone to operate in saturation, unfortunately, these are the transistors with higher impact on DAC accuracy, because they are related to the most significant bit (MSB). We intend to design the converter operating far from saturation but for the fabricated circuit its interesting to explore the circuit behavior with any supply. Here we use the following expression SODINI et al. (1984) for the CVS effect on mobility

$$\mu_{sat} = \frac{\mu_0}{\sqrt{1 + (E_x/E_C)^2}} \quad (3.10)$$

where μ_0 is the low field mobility ($440 \text{ cm}^2/Vs$, from the IBM 130 nm technology), E_C is the critical electric field, given by $E_C = \nu_{sat}/\mu_0$ and ν_{sat} is the carrier saturation velocity. E_x corresponds to the electric field value existing along the channel, approximated by $E_x = V_{DS}/L$, where V_{DS} is the drain-source voltage. Equation 3.11 is known to describe the dependence of mobility under high longitudinal electric fields with quite good accuracy. The magnitude of ν_{sat} is essentially independent of doping concentration and is of the order of 10^7 cm/s for both electrons and holes at room temperature.

From equation 3.11 we can estimate the minimum channel length that result in a maximum error ϵ for the CVS (μ_{sat}) by

$$L_{min} = \frac{V_{DS}}{E_C \sqrt{\frac{1}{(1-\epsilon)^2} - 1}} \quad (3.11)$$

Although the DAC was designed to operate with very low supply voltages, for the manufactured circuit to be characterized in a wide range of operating conditions, we considered the possibility of exciting the circuit between 100 mV and 600 mV. Considering a V_{DS} of 600 mV, that is high enough to saturate the transistor on the inversion levels used in this work, we have the minimum channel length according to table 3.2.

Table 3.2: Maximum channel length as a function of the maximum error.

Resolution	6 bit	8 bit
Error (ϵ)	1/64	1/256
$L_{min}(\mu m)$	15.8	29.8

The resulting length is equivalent to the length of the series association of M_1 and either M_2 or M_3 in Fig. 3.3. Thus, we have used $L = 10\mu m$ for all transistors.

3.7 Transistor Sizing

The Fig. 3.14 presents the estimated DAC error using the methodology described in the last section, for two biasing voltages and related to the individual transistor area.

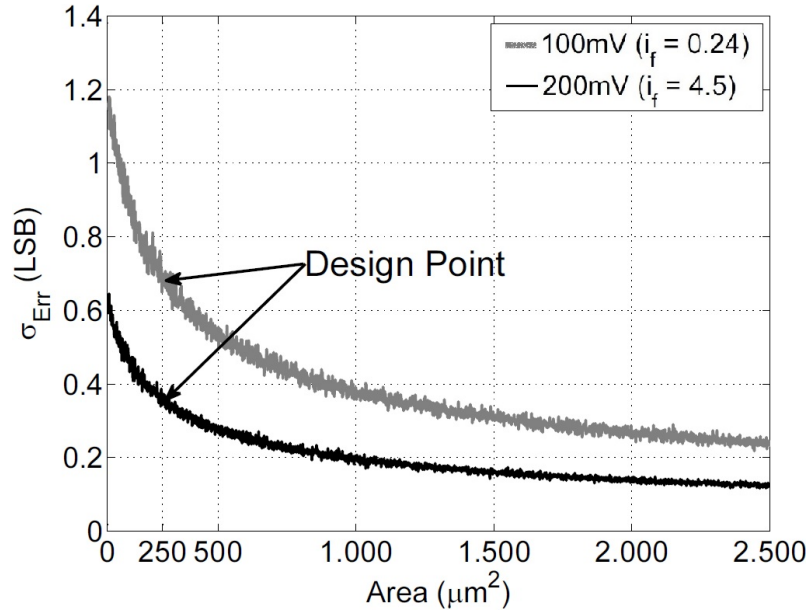


Figure 3.14: Standard deviation of the DAC error as a function of transistor area and biasing voltage. Considering the converter with 6 bits of resolution.

As a way to validate the presented linearity analysis methodology, the M–2M DAC was designed and simulated using Cadence-Virtuoso tool, which uses the BSIM4 and the Pelgrom’s mismatch model as basis. Monte Carlo (MC) simulation with 500 points was performed and the error standard deviation ($\sigma_{err}(LSB)$) was calculated and normalized to the nominal LSB.

Using Fig. 3.14 we choose the aspect ratio for the 6-bit converter equal to $\frac{W}{L} = \frac{25\mu\text{m}}{10\mu\text{m}}$ for each transistor. The final circuit layout is shown on Fig. 3.15 resulting a silicon area of 0.024mm^2 , including the digital part and dummy structures for matching improvement. The fabricated circuit is highlighted in Fig. 3.16, where the total chip area is $2.5\text{mm} \times 2.5\text{mm}$.

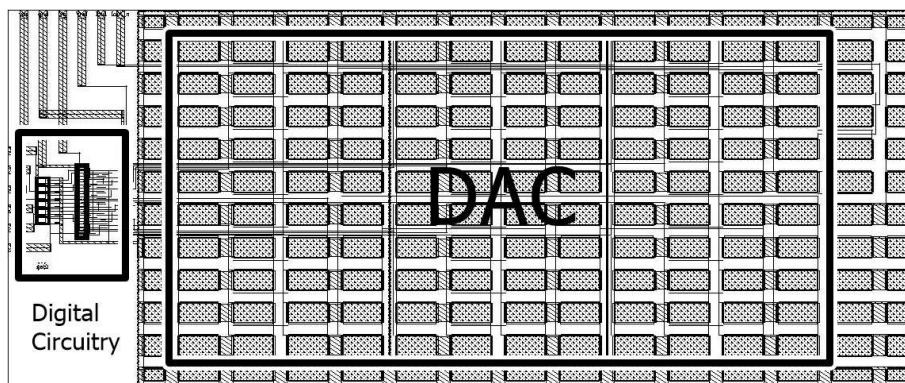


Figure 3.15: DAC layout.

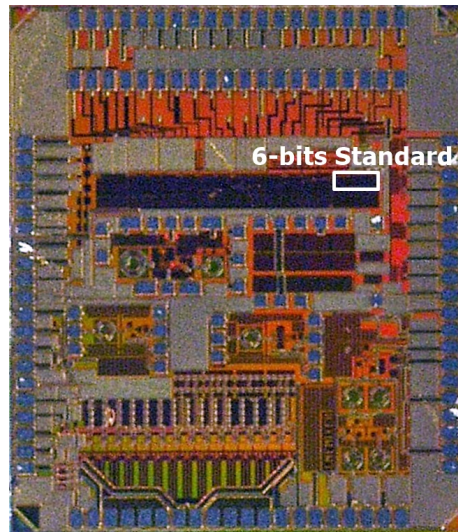


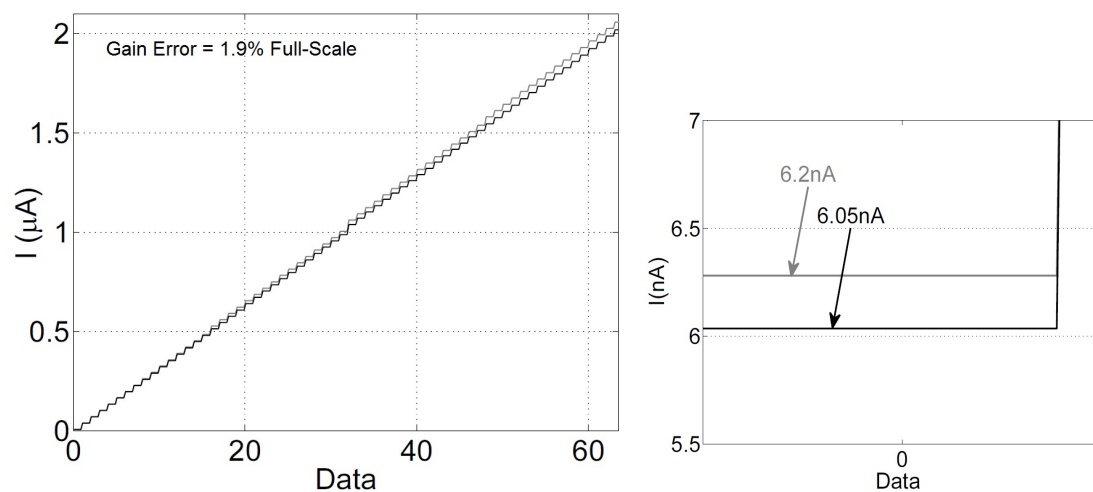
Figure 3.16: Chip micrograph highlighting the 6-bit converter.

3.8 Linearity Errors

Considering that the DAC works with extremely low gate voltages, the difference between the “on” and “off” states of the switching transistors (M_2 and M_3 of Fig. 3.3, for example) is small, but it does not cause significant linearity reduction, impacting only as offset and gain errors, that are linear limitations and can be easily calibrated.

Transistors M_2 and M_3

While performing the first Monte Carlo simulations on Virtuoso tool we noted these linear limitations. To illustrate this behavior we depicted the two worst cases, one is the gain error (Fig. 3.17a) and the other is a offset (“zero”) error (Fig. 3.17b), which is a zoomed part on the first data. As we can see, the deviation between the MC worst cases increases as the data increases showing that a gain variation occurs, which is an easy solvable problem. The same occurs with the offset error showed on Fig. 3.17b. This figure was obtained exciting the DAC digital input with a progressive binary code that changes from “0” to “63”.



(a) DAC output for the two Monte Carlo worst cases highlighting the gain error.

(b) DAC linear offset error.

Figure 3.17: DAC linear errors.

4 RESULTS

In this chapter we present simulation results performed over different converter resolutions with different transistors. The foregoing method was applied to M–2M DACs with 6 and 8 bits of resolution, implemented in the IBM 130 nm process using standard NMOS transistors ($V_T = 200mV$ for long channel FETs). This process was chosen due to availability on the educational program provided by MOSIS, this way we can fabricate our circuit and test it for more accurate results. To explore a wider design space we applied same method to devices with lower threshold voltages like Low- V_T transistors ($V_T = 100mV$) and Zero- V_T transistors ($V_T = -2mV$). Threshold parameters were extracted through $\frac{g_m}{I_D}$ curves. Equal values for V_G and V_{Ref} were chosen to simplify analysis ($200mV$ and $100mV$). The design uses $L=10\mu m$ as a way to avoid short-channel effects, as previously explained. This circuit went to fabrication and returned, but we didn't have enough time to test it.

4.1 DAC Simulation Test Benches

There are two test benches for this work designed on Virtuoso. The simplest, showed in Fig. 4.1, excites the DAC digital input simulating a progressive binary code that changes from zero to $2^N - 1$, being N the converter number of bits. The sources are connected to transmission gates that works as switches, directing the current to nodes I_{out} or \bar{I}_{out} .

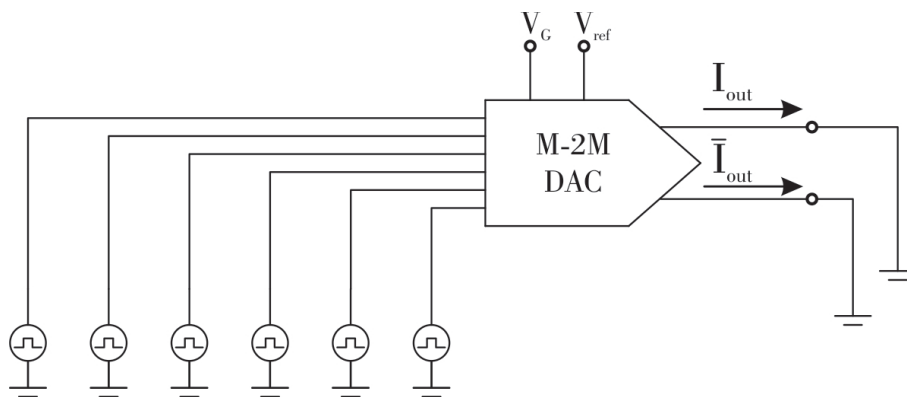


Figure 4.1: Testbench for error analysis of a 6-bit DAC.

In order to evaluate the converter sampling speed it is proposed a test bench (Fig. 4.2) that consists on a resolution configurable verilog ideal ADC with variable clock that converts a sinusoidal analog input signal to its digital counterpart, to be used as the DAC input.

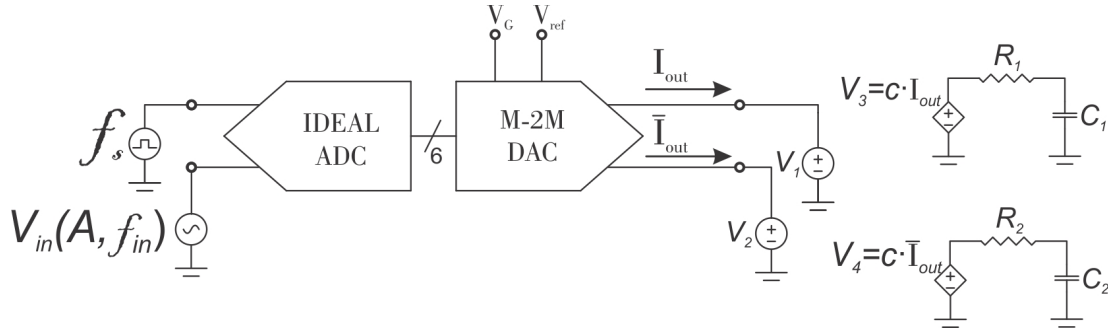


Figure 4.2: Testbench for speed analysis.

The current outputs are sensed by voltage sources V_1 and V_2 that controls the voltage sources V_3 and V_4 . The circuit only works if $V_1 = V_2$. The low pass filter formed by R_1 and C_1 was adjusted to remove glitches that appeared and will be shown later in this chapter, same for R_2 and C_2 . This test bench was used to evaluate the converter error and is fully analogical, which means that it does not require the mixed signal environment of Virtuoso tool, which implies in a simplified simulation.

From IEEE Std. 1241-2000 (2001), the signal frequency and ADC clock varies as follows

$$f_{in} = \frac{J}{M} f_s \quad (4.1)$$

being f_{in} the input frequency, f_s the sampling frequency (clock), J an integer, usually prime relative to M , ensuring that they don't have common factors. There are some important points to highlight here. M usually is a power of two and its value implies directly on simulation time, so after some tests it was decided to use the value 512 for M and 7 for J , making sure that the ADC works properly and not spend much time simulating.

4.2 DAC Simulation Results

This section presents simulation results of the converters designed in this work.

4.2.1 DAC Results: Standard MOSFETs

From the simplest test bench (Fig. 4.1) we performed a Monte Carlo simulation with 500 points on the 6-bit converter with standard transistors (SVT) and the output data was analyzed in Matlab for post-layout extraction. The INL that resulted from this simulation appears in Fig. 4.3 where we can see the sum of two effects, intrinsic nonlinearity and variability given by mismatch. All results are for biasing voltages of $V_G = V_{Ref}$ equal to $100mV$ (inversion level $i_f = 0.24$, corresponding to weak inversion) and $200mV$ (inversion level $i_f = 4.5$, corresponding to moderate inversion).

Separating the two effects, Fig. 4.4 shows just the intrinsic nonlinearity of the converter. Solve this issue is not our focus, but we already quoted some ideas on how to deal with it in session 3.3.1. Subtracting the intrinsic nonlinearity from Fig. 4.3 results in Fig. 4.5, that shows purely the variability error given by mismatch for two different supply voltages.

We can observe here that as far as we go in weak inversion the mismatch becomes the main source of error. Now, solving the standard deviation for each INL data we have the converter error variability presented on Fig. 4.6.

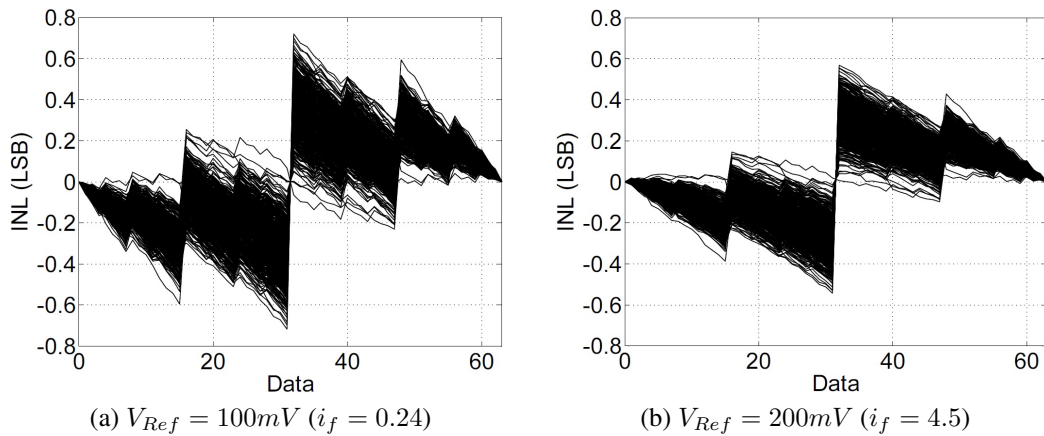


Figure 4.3: 6-bit SVT converter INL for post-layout simulated results.

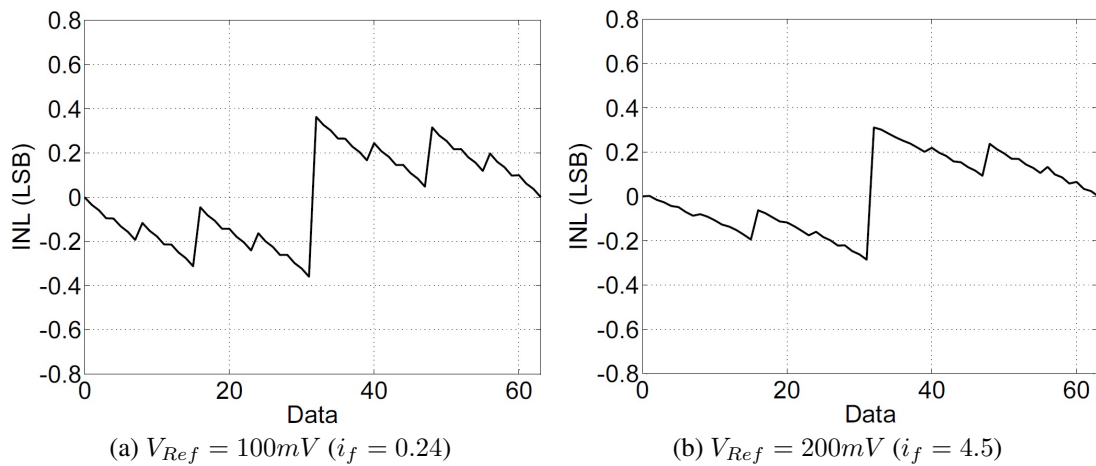


Figure 4.4: 6-bit SVT DAC Intrinsic nonlinearity.

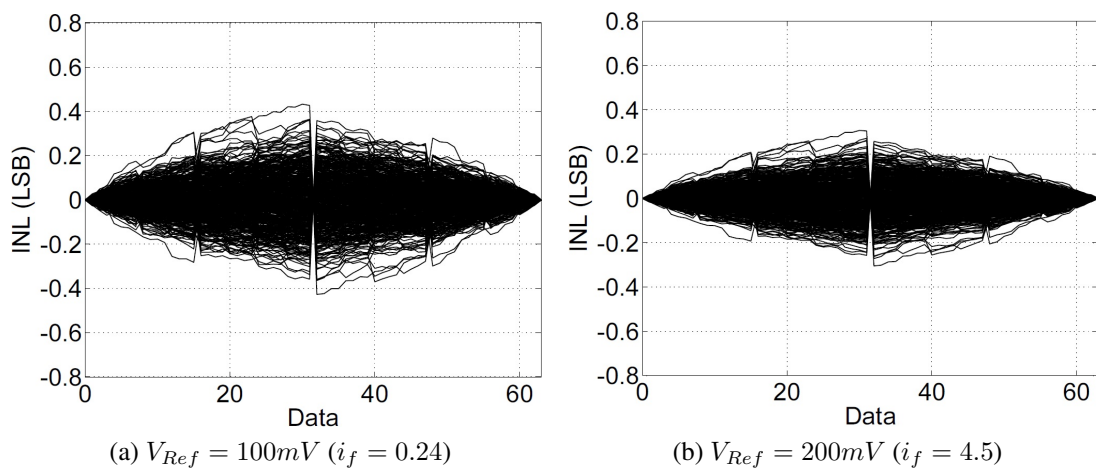


Figure 4.5: 6-bit SVT converter INL given by mismatch for post-layout simulated results.

If we compare MC simulated results with our analytical approach, previously demonstrated, it becomes clear that in weak inversion our model is more pessimistic. However, since our analytical analysis is based on a model valid in all operating regions it eval-

uates more accurately the converter behavior in weak inversion KLIMACH; GALUP-MONTORO; ARNAUD (2005).

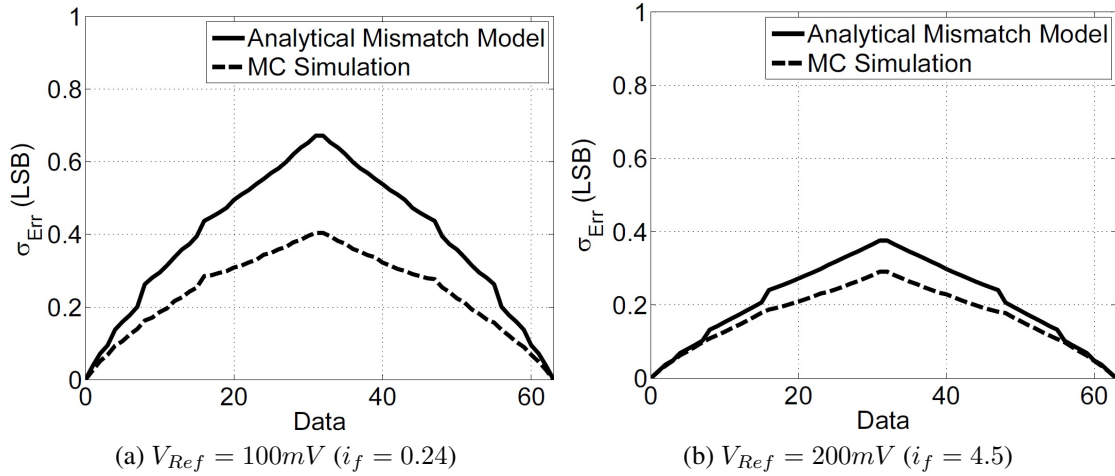


Figure 4.6: 6-bit SVT DAC comparison between analytical and post-layout simulated results.

Of course that measured results are needed to support this information but, since results are very similar we suppose that our methodology can be used for trade-off estimation and design-space exploration of M–2M DACs operating under very low supply voltage. Remembering that this circuit was already prototyped and is waiting to be measured.

4.2.2 DAC Results: Low- V_T MOSFETs

Until now we proved that a 6-bit M–2M DAC converter is feasible using standard NMOS transistors on the range of $200mV$ to $100mV$ of voltage supply. But can we go beyond this? To answer this question we designed an 8-bit converter with Low- V_T transistors (LVT) using the design space showed on Fig. 4.7. More resolution implies in higher transistor area to achieve same mismatch error, as previously observed in Fig. 3.13b. Theoretically, with transistors size of $\frac{W}{L} = \frac{300\mu m}{10\mu m}$, as shown in Fig. 4.7, this circuit will present an mismatch error below 0.5 LSB with $100mV$ of supply. The circuit layout is shown in Fig. 4.8 and was sent to fabrication. The total area occupied is $0.195mm^2$ and appears highlighted in the chip micrograph (Fig. 4.9).

Since we are using a different device, all process parameters must be re-extracted. The most important is N_{oi} , that is the main mismatch model parameter (Eq. 3.3), and its value is $6.5 \cdot 10^{13}cm^{-2}$. Also, $B_{I_{SQ}}$ parameter is equal to $6\% - \mu m$ for Low- V_T transistor.

Following the foregoing design methodology we ran a Monte Carlo simulation with 100 points (500 points takes too long for the 8 bits converter) on Virtuoso and depicted the INL in Fig. 4.10. What becomes very clear in this case is that the intrinsic nonlinearity inserts a huge amount of error. The INL of -12 LSB to $+25$ compromises 5 bits of resolution, so the ENOB in this case will be around 3 bits. This error wasn't predicted by our methodology but there are three possibilities to correct the intrinsic nonlinearity: designing the ladder in a symmetric way, unbalancing the branches (both explained in section 3.3.1) and software calibration, like for instance using a look-up table. Another thing we noticed is that this case was the only one where the intrinsic nonlinearity is higher with $200mV$ of supply than with $100mV$.

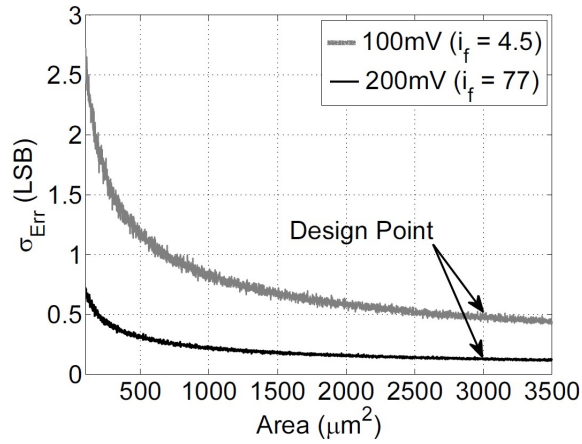


Figure 4.7: Standard deviation of DAC error as a function of Low- V_T transistor area. 8-bits converter. $V_G = V_{Ref} = 100mV$ ($i_f = 4.5$) and $V_G = V_{Ref} = 200mV$ ($i_f = 77$).

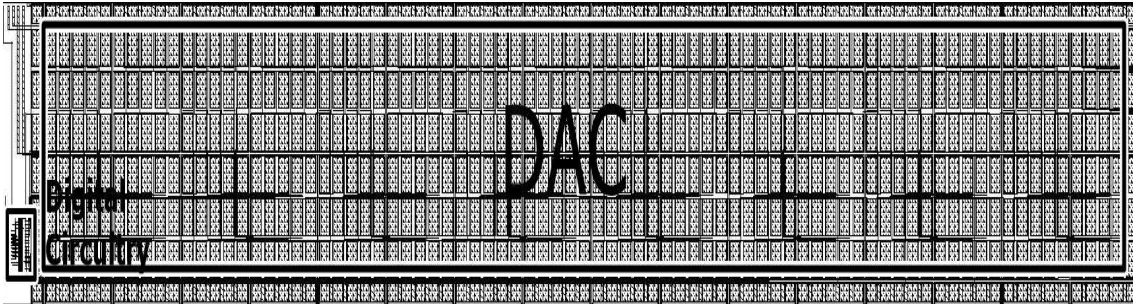


Figure 4.8: 8-bits LVT DAC layout.

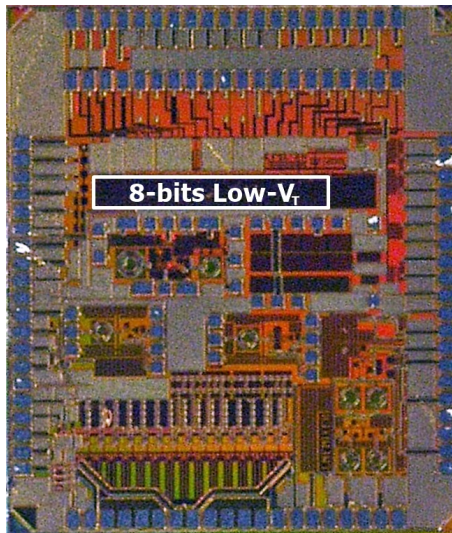


Figure 4.9: Chip micrograph highlighting the 8-bit Low- V_T converter.

Again, subtracting the intrinsic nonlinearity from Fig. 4.10 we have purely the mismatch variability presented in Fig. 4.12. Our methodology clearly predicts the mismatch variability by showing an error below ± 0.5 LSB. This is corroborated by results of Fig. 4.13.

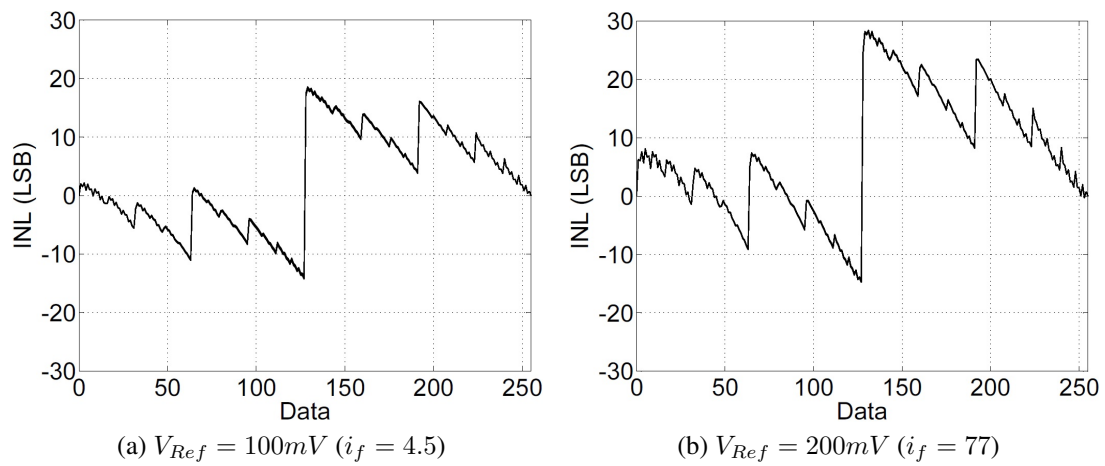


Figure 4.10: 8-bit LVT converter INL for post-layout simulated results.

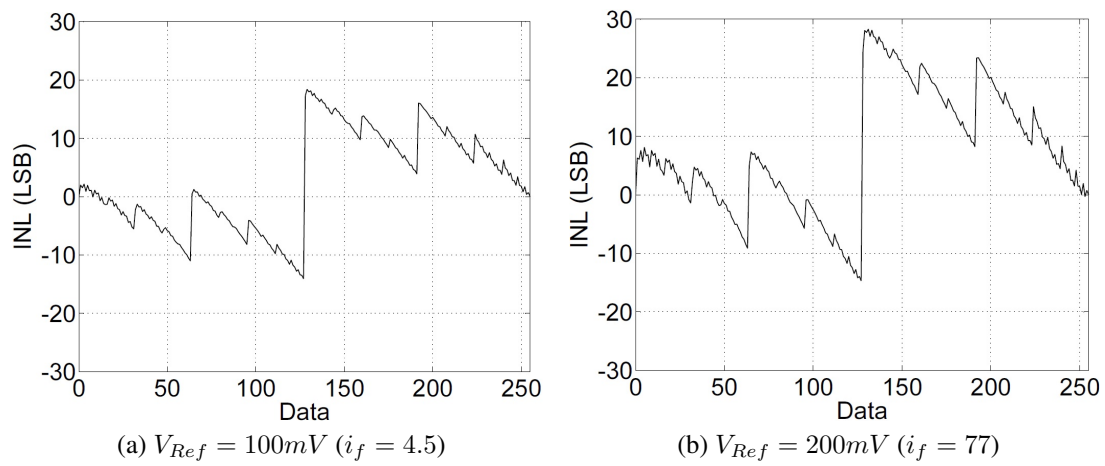


Figure 4.11: 8-bit LVT DAC Intrinsic nonlinearity.

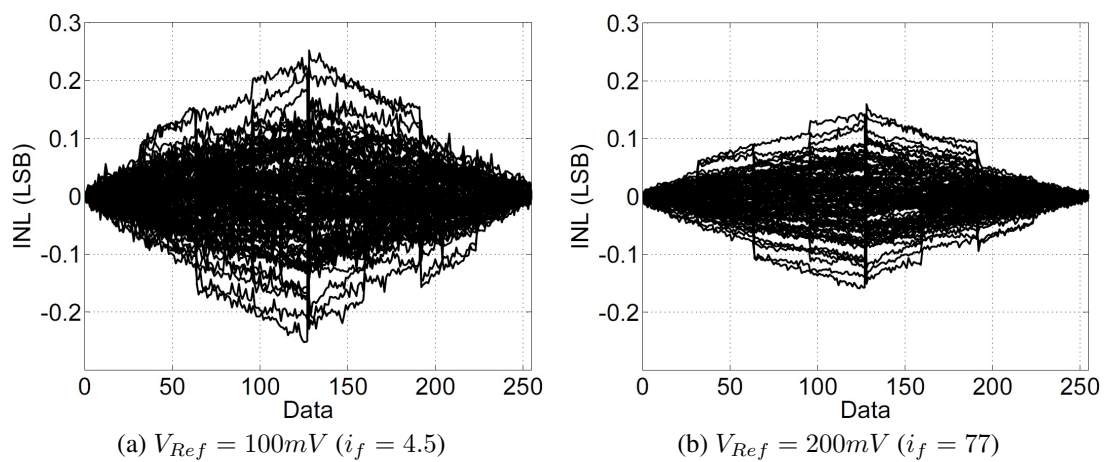


Figure 4.12: 8-bit LVT converter INL given by mismatch for post-layout simulated results.

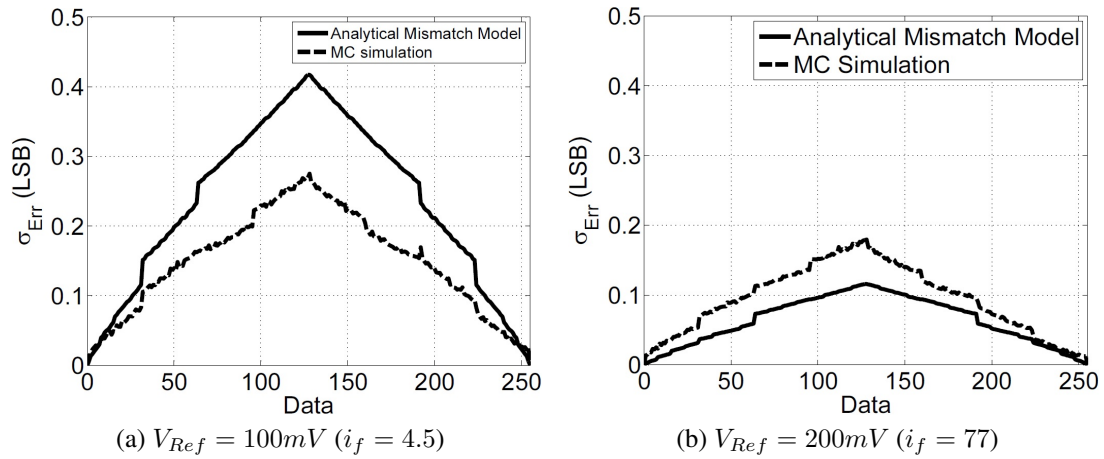


Figure 4.13: 8-bit LVT DAC comparison between analytical and post-layout simulated results.

This analysis with low threshold transistor raises a question: the intrinsic nonlinearity is the main problem because the higher resolution, higher transistor area or different device? To answer that we designed a 6-bit DAC with Low- V_T transistor (LVT). The aspect ratio of $\frac{W}{L} = \frac{25\mu m}{10\mu m}$ and supplies of $100mV$ ($i_f = 4.5$) and $200mV$ ($i_f = 77$) were used to compare with previously designed SVT DAC.

From the INL results showed in Fig. 4.14, that are the sum of intrinsic nonlinearity with variability, one can note that intrinsic nonlinearity inserts even more error when comparing with results in Fig. 4.3. Furthermore, since we are working on a higher inversion level, the mismatch is smaller, as proved by Fig. 4.16, as well its standard deviation presented in Fig. 4.17.

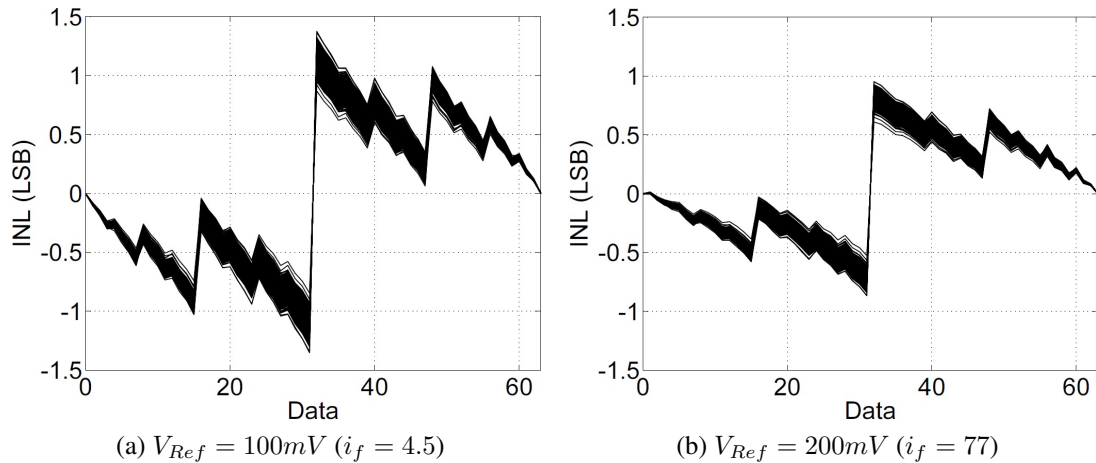


Figure 4.14: 6-bit LVT converter INL for post-layout simulated results.

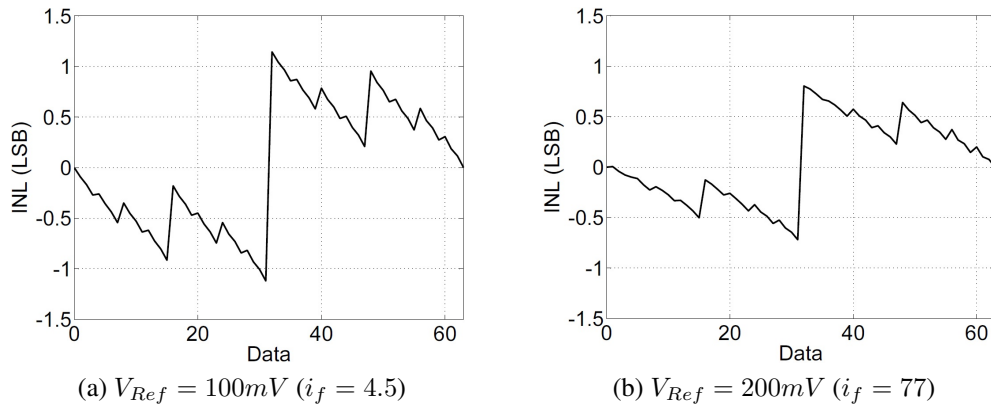


Figure 4.15: 6-bit LVT DAC Intrinsic nonlinearity.

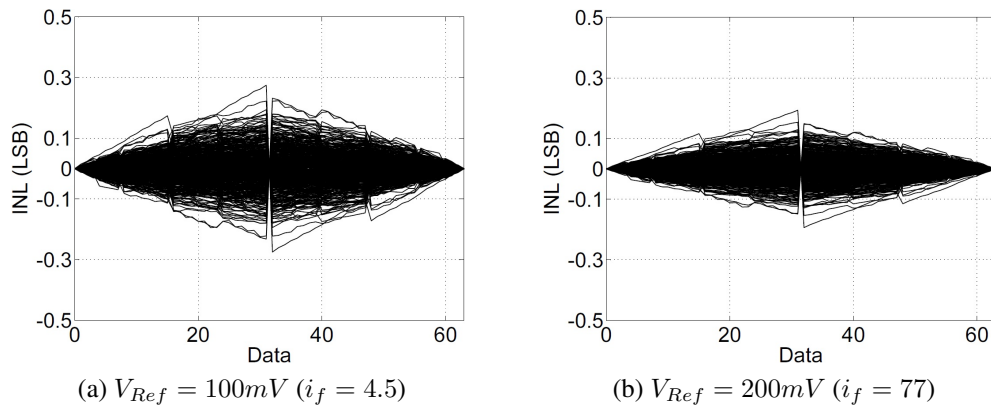


Figure 4.16: 6-bit LVT converter INL given by mismatch for post-layout simulated results.

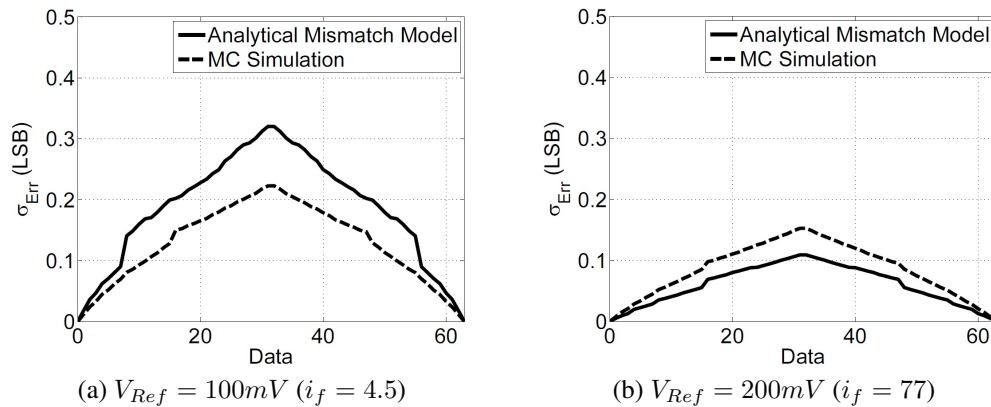


Figure 4.17: 6-bit LVT DAC comparison between analytical and post-layout simulated results.

What we take from this session is that Low- V_T transistors presents a higher intrinsic nonlinearity when comparing with standard transistors, even with same inversion level. To support this statement let's get as an example Fig. 4.14a, which has the same inversion level that 4.3b, but presents a higher INL. The high resolution converter presented even worse nonlinear behavior but still, the variability is well predicted.

4.2.3 DAC Results: Zero- V_T MOSFETs

Since we are evaluating the behavior of other devices it is a good idea to look at Zero- V_T transistors (ZVT), also called Native transistors. They are available for process of 180nm below, where there's no well implant to correct the threshold voltage on N-type transistors, which means that there are only N-type Zero- V_T transistors. They present a V_T around zero and for this reason work in moderate inversion when $V_G = 0V$, showing a similar behavior as depletion MOS devices.

It is expected that this converter presents a similar behavior that the LVT converter, which means less variability and higher intrinsic nonlinearity. To see if it's true we designed another 6-bit M-2M DAC, now using ZVT and compared with the others by maintaining the aspect ratio of $\frac{W}{L} = \frac{25\mu m}{10\mu m}$ and biasing with $V_{Ref} = 200mV$ ($i_f = 1800$) and $V_{Ref} = 100mV$ ($i_f = 104$). The layout with $246\mu m \times 100\mu m$ and chip micrograph are shown in Figures 4.18 and 4.19 respectively.

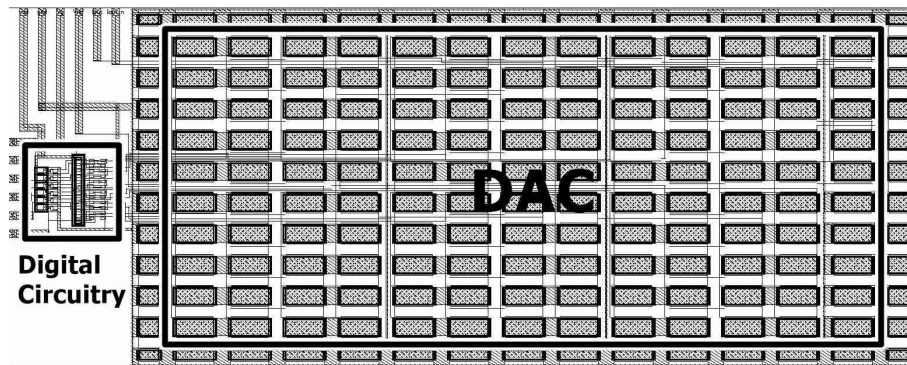


Figure 4.18: 6-bit ZVT DAC layout.

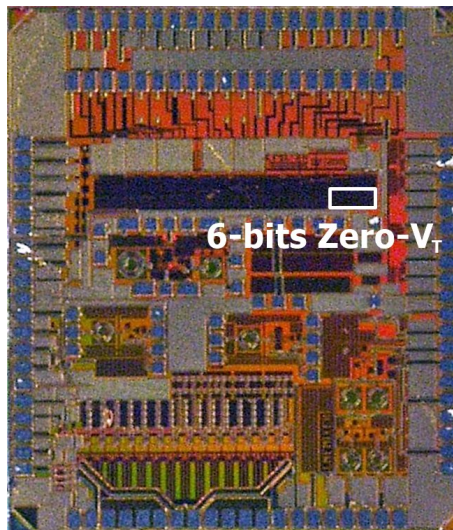


Figure 4.19: Chip micrograph highlighting the 6-bit ZVT DAC.

The INL results showed in Fig. 4.20 corroborate with our idea that this device present less variability and higher intrinsic nonlinearity. Because the intrinsic nonlinearity, showed in Fig. 4.21, this converter loose more than 1-bit ($INL = \pm 2$ LSB) of effectiveness and the variability is even lower than with Low- V_T transistors, which is justified by the higher inversion level.

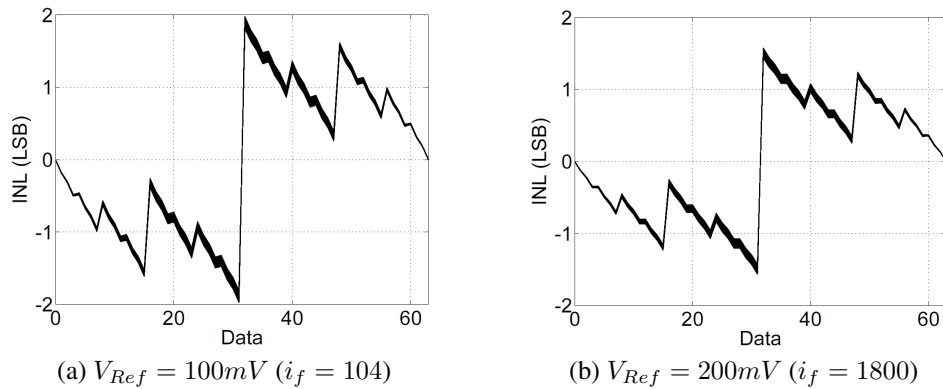


Figure 4.20: 6-bit ZVT converter INL for post-layout simulated results.

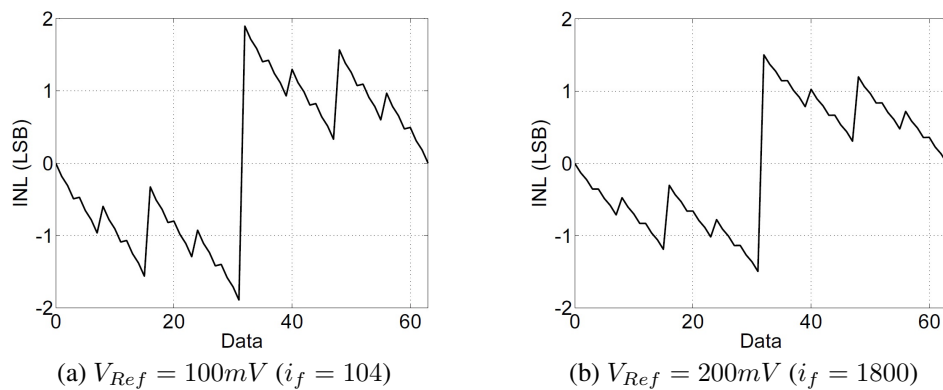


Figure 4.21: 6-bit ZVT DAC Intrinsic nonlinearity.

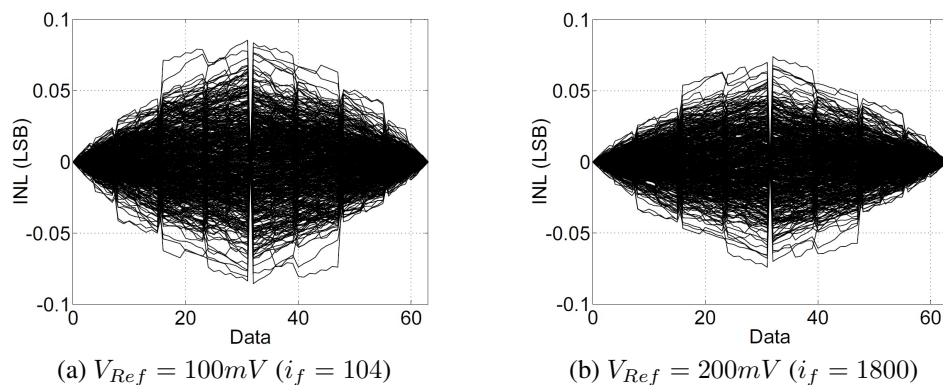


Figure 4.22: 6-bit ZVT converter INL given by mismatch for post-layout simulated results.

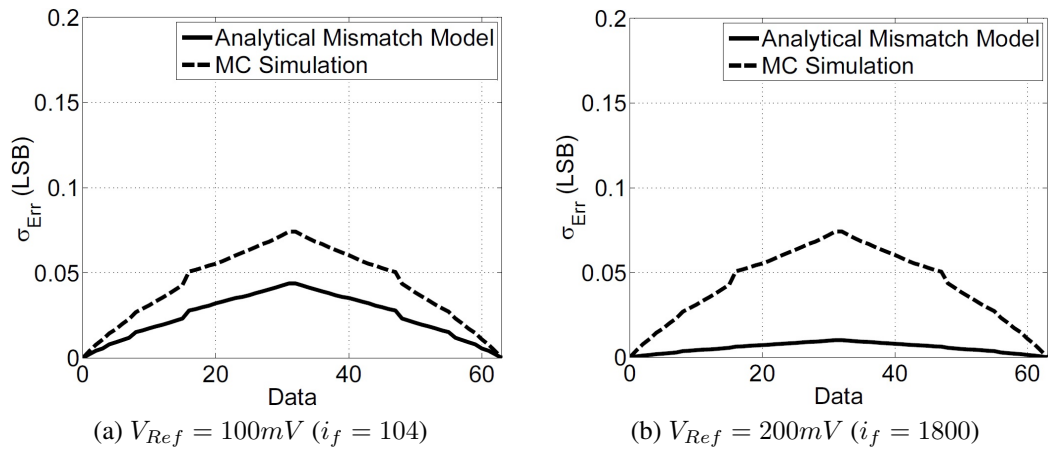


Figure 4.23: 6-bit ZVT DAC comparison between analytical and post-layout simulated results.

To conclude, our analytical model well predicts the circuit variability proving that a converter with 6-bits of resolution and less than 200mV of supply is feasible. We also noted room for improvement when using lower threshold devices but new techniques must be added in order to reduce the intrinsic nonlinearity, of course this is a scope for future works.

4.3 DAC Performance in Time Domain

Using the second test bench (Fig. 4.2) and simulating only the typical result it is possible to observe the converter behavior over time. Fig. 4.24 shows the verilog ADC input and the 6-bit SVT DAC outputs before and after filtering. The frequency wave is 136.7 Hz and is sampled with a frequency of 10 kHz. We can see that the converter clearly reconstructs the input signal, after that, some switching glitches are removed with the low pass filter formed by R_1 and C_1 (figures 4.1 and 4.2). The 6-bit SVT DAC presented a same AC and DC power consumption of $400nW$ with $V_{Ref} = 200mV$ and $13.2nW$ with $V_{Ref} = 100mV$.

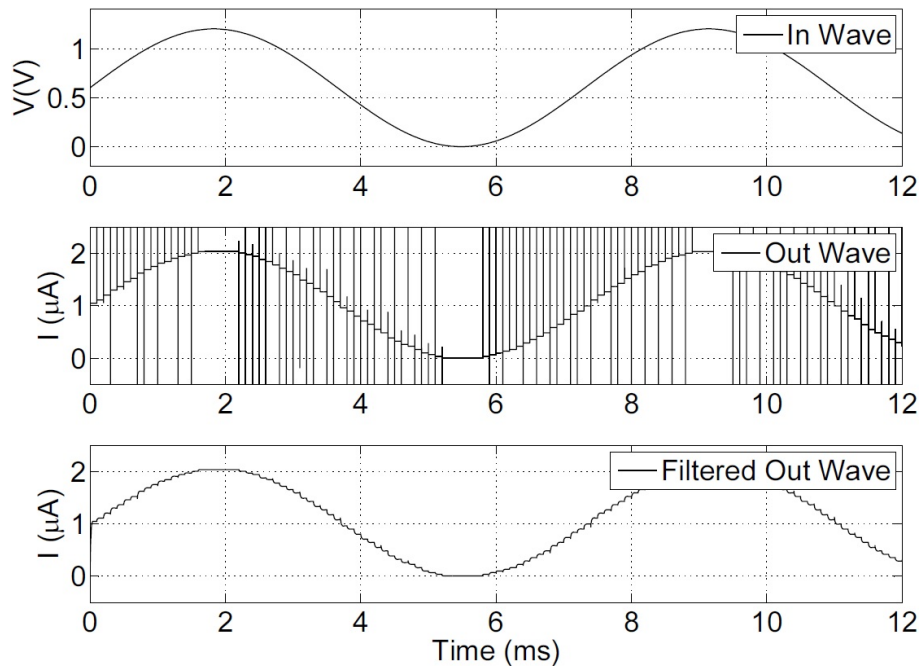


Figure 4.24: ADC input and the 6-bit SVT DAC output waves. The sampling frequency is 10 kS/s and $V_{Ref} = 200mV$.

The original source of glitching that appears in Fig. 4.24 is a subject for further studies.

4.3.1 DAC Performance in Time Domain with Low- V_T transistors

For the 8-bits converter we also simulated its behavior over time. As early explained the converter loses around 5-bits of effectiveness due the intrinsic nonlinearity, which can be seen in Fig. 4.25, where the distortion appears in the output wave. In this case, the converter showed a same AC and DC power consumption of $30\mu W$ with $V_{Ref} = 200mV$ and $3.2\mu W$ with $V_{Ref} = 100mV$.

Now, for the 6-bits LVT DAC, with its time behavior showed in Fig. 4.26, the loss due to intrinsic nonlinearity is not visible and will appear only performing the Discrete Fourier transform (DFT) that will be shown in next section. Same AC and DC Power consumption of $2.7\mu W$ with $V_{Ref} = 200mV$ and $280nW$ with $V_{Ref} = 100mV$ were achieved.

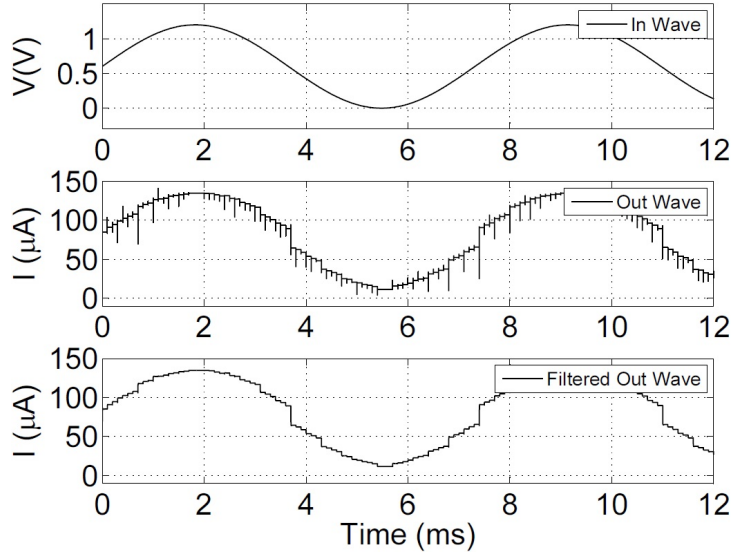


Figure 4.25: ADC input and LVT DAC output waves. 8-bits of resolutions and sampling frequency of 10 kS/s at $V_{Ref} = 200mV$.

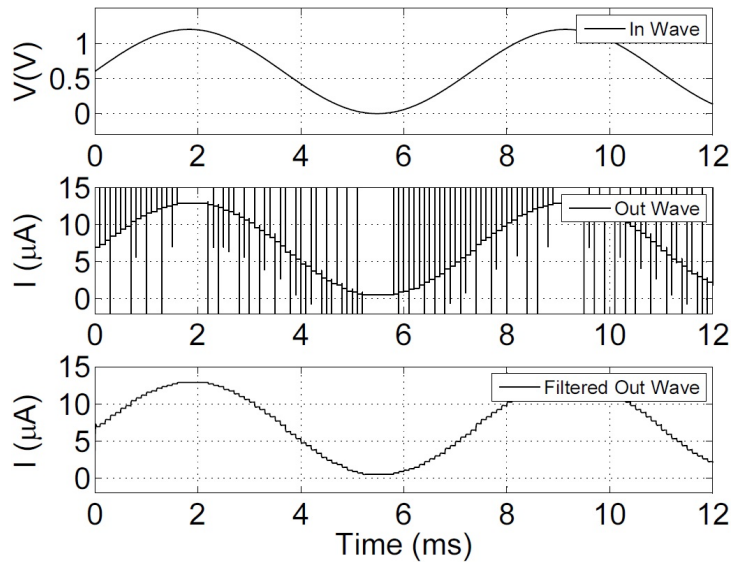


Figure 4.26: ADC input and LVT DAC output waves. 6-bits of resolutions and sampling frequency of 10 kS/s at $V_{Ref} = 200mV$.

4.3.2 DAC Performance in Time Domain with Zero- V_T transistors

Now, for the 6-bit converter with Zero- V_T , the input and output waves are depicted in Fig. 4.27. Here, the intrinsic nonlinearity error is visible on every half period. Again, the DFT will show more accurately the ENOB loss on this converter. The circuit presented a same AC and DC power consumption of $4.5\mu W$ for $V_{Ref} = 200mV$ and $750nW$ for $V_{Ref} = 100mV$.

All these results were simulated on typical. Even not showing the variability effects it served to understand a little better the nonlinearity effects, and also to estimate the power consumption. In next section we performed the discrete Fourier transform (DFT) of the output signals and estimated the ENOB. Again, since we already proved in previous section that variability is under control, the DFT will show the converter behavior on frequency domain and also give us an estimate on sampling frequency limits.

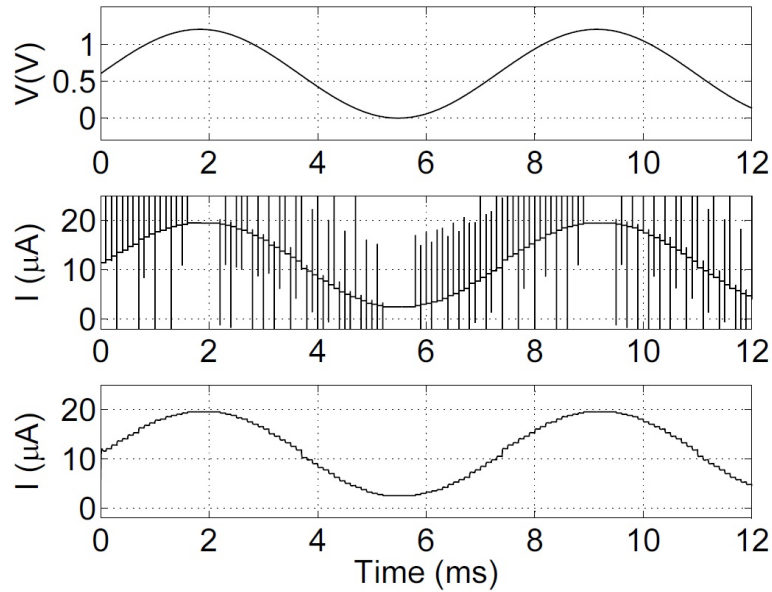


Figure 4.27: ADC input and 6-bit ZVT DAC output waves. The sampling frequency is 10 kS/s and $V_{Ref} = 200mV$.

4.4 DAC Performance in Frequency Domain

The analysis in frequency domain shows just the distortion due to intrinsic nonlinearity and nothing about mismatch. Although this effect is not our focus, we included this section to illustrate the FFT usage as a way of analyze the maximum sampling rates.

For the SVT converter, using the Spectrum Measurement tool on Virtuoso, we can perform the discrete Fourier transform (DFT) of the output signal (Fig. 4.28). At first glance we see a difference of 44dB between the signal frequency and the Third Harmonic Frequency, difference that will decrease for other converters due to an increase on the intrinsic nonlinearity.

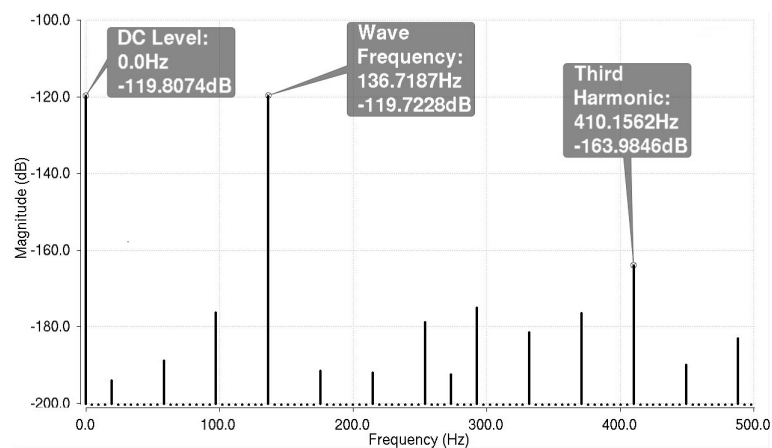


Figure 4.28: Discrete Fourier Transform of the 6-bit SVT DAC output signal at 10 kS/s and $V_{Ref} = 200mV$.

We then implemented a routine that calculates the ENOB while varying the sampling frequency. As we increase the ADC sampling frequency, the measured ENOB starts to decrease. With a supply voltage of 200mV the maximum ENOB obtained was 5.8 bits for f_S values below 3 MS/s on post-layout simulation. As can be seen in Fig. 4.29,

when the ENOB starts to decrease it creates a tendency. If we extend this decreasing tendency its possible to estimate a maximum sampling frequency value for the circuit on the intersection point with the maximum ENOB, that is 5.13 MS/s for $V_{Ref} = 200mV$.

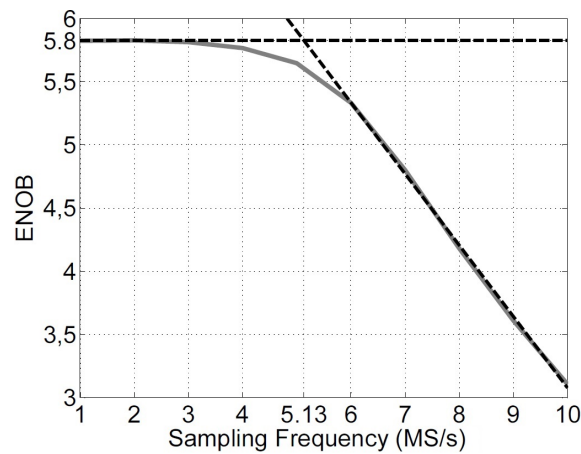


Figure 4.29: Variation of the ENOB with the sampling frequency ($V_{Ref} = 200mV$). 6-bit SVT DAC.

Now, for a supply voltage of $100mV$, the DFT of the output signal, showed in Fig. 4.30, presents a difference of 43dB between the the signal frequency and the Third Harmonic Frequency.

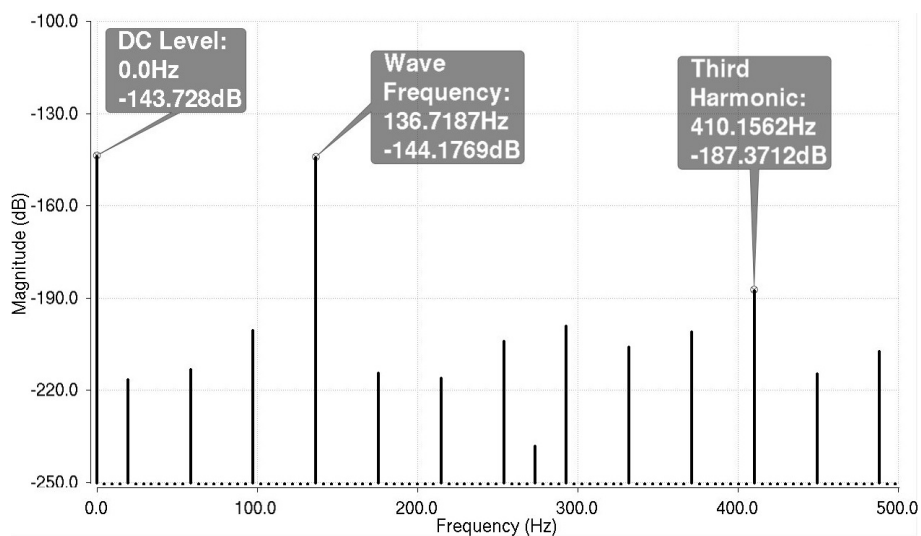


Figure 4.30: Discrete Fourier Transform of the 6-bit SVT DAC output signal at 10 kS/s and $V_{Ref} = 100mV$.

Again, for a sampling frequency below 1 MS/s the the maximum ENOB is 5.75 bits. Extending the decreasing part of the curve we can see that the maximum sampling frequency is reduced to 1.7 MS/s. We can conclude that for lower supply voltage, less current flows through the branches, as a consequence lower is the converter speed.

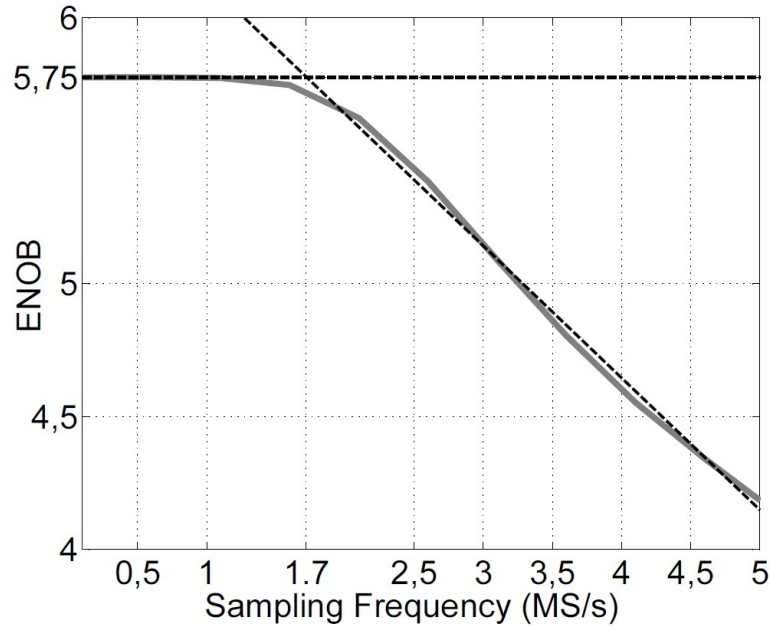


Figure 4.31: Variation of the ENOB with the sampling frequency ($V_{Ref} = 100mV$). 6-bit SVT DAC.

4.4.1 DAC Performance in Frequency Domain with Low- V_T transistors

Some adjustments on the test bench were carried out to perform a discrete Fourier transform (DFT) of the output signal (Fig. 4.32) on the 8-bits converter. We also evaluated just the performance with 200mV supply, mainly because the long simulation time. For the same reason we didn't tested the speed limitations of this converter but it maintained the same ENOB for a sampling frequency up to 4MS/s. The DFT shows a difference of 24.5dB between the signal frequency and the Third Harmonic Frequency. The calculated ENOB for this frequency is 3.1 bits. As expected the loss of almost 5-bits was previously seen in the INL results.

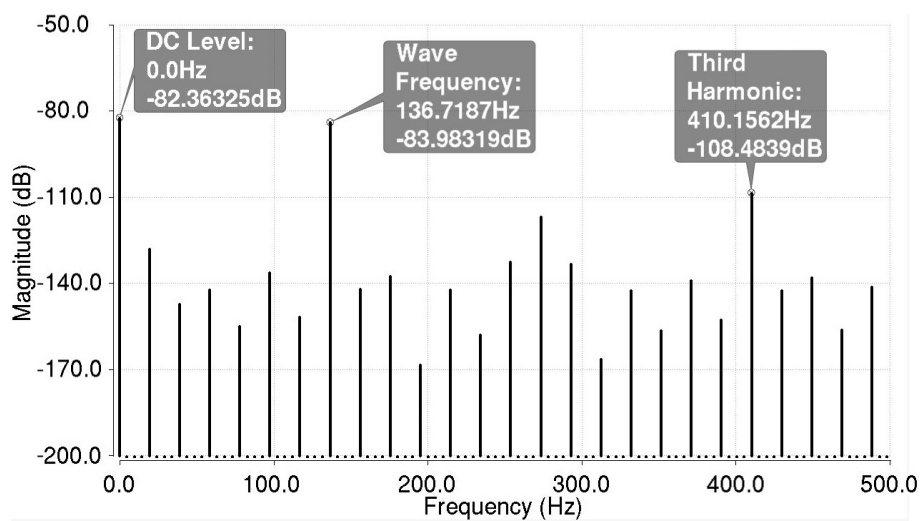


Figure 4.32: Discrete Fourier Transform of the 8-bit LVT DAC output signal at 10 kS/s and $V_{Ref} = 200mV$.

Same analysis was performed for the 6-bits converter and the DFT is presented in

Fig. 4.33. The nonlinear behavior is represented by the third harmonic signal showing a difference of 36dB with the wave frequency. The ENOB in this case is 5.4 bits.

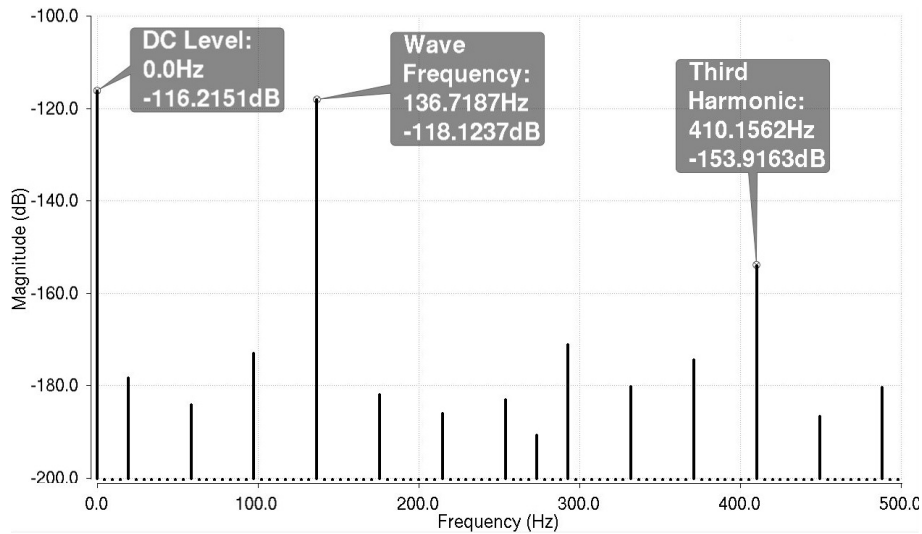


Figure 4.33: Discrete Fourier Transform of the 6-bit LVT DAC output signal at 10 kS/s and $V_{Ref} = 200mV$.

This circuit presented almost the same frequency behavior that the converter with standard MOSFETs. It maintains the ENOB constant until a sampling frequency of 6MS/s and achieve a maximum at 9MS/s. The 6-bit LVT DAC can operate with higher sampling frequency because more current flows trough it, which is quite obvious since it has the same transistors size as the 6-bit SVT DAC. What we get from here is that solving the intrinsic nonlinearity issue, this converter might become a good candidate for low voltage operation with higher speed.

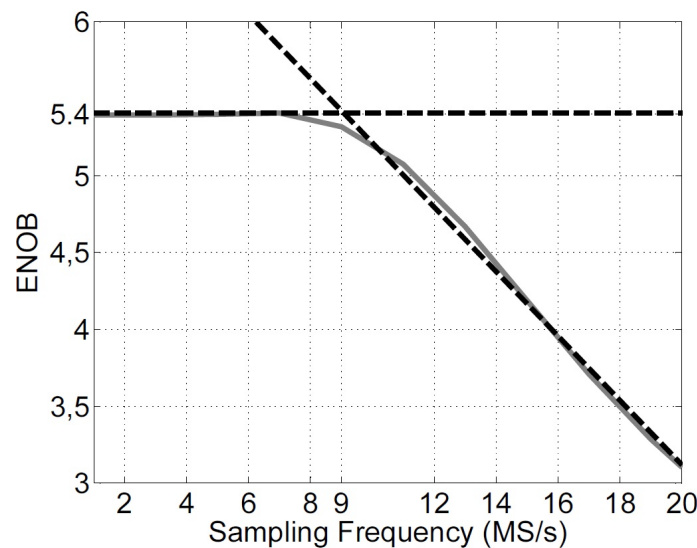


Figure 4.34: Variation of the ENOB with the sampling frequency ($V_{Ref} = 200mV$). 6-bit LVT DAC.

4.4.2 DAC Performance in Frequency Domain with Zero- V_T transistors

With the Zero- V_T DAC the analysis continues coherent. The DFT of the output signal is shown in Fig. 4.35. We can see a difference of 33.3dB between the the signal frequency and the Third Harmonic Frequency. The calculated ENOB for this frequency is 4.7 bits

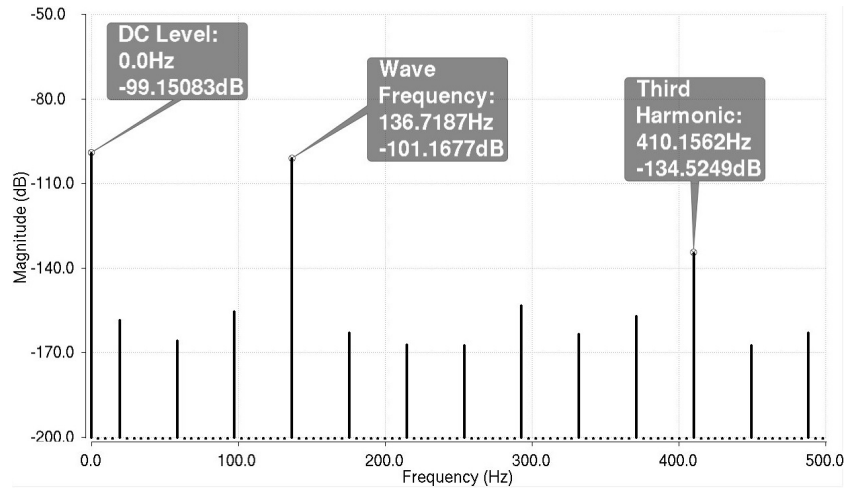


Figure 4.35: Discrete Fourier Transform of the 6-bit ZVT DAC output signal at 10 kS/s and $V_{Ref} = 200mV$.

This Zero- V_T converter presented even more speed capability at cost of higher consumption. It maintained constant the ENOB until 10 MS/s and a maximum estimated at 13.5 MS/s. Lets keep clear that this results are just for the typical case and still lacks the intrinsic nonlinearity correction, but still, there's room for improvement when the subject is conversion speed.

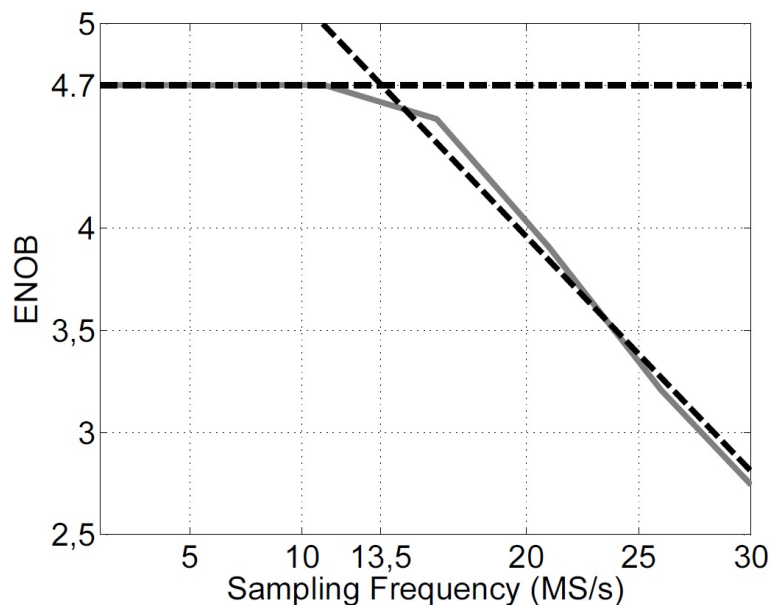


Figure 4.36: Variation of the ENOB with the sampling frequency ($V_{Ref} = 200mV$). 6-bit ZVT M-2M DAC.

4.5 Results Discussion

The aforementioned results corroborate that the M–2M DAC is a promising topology for very low voltage applications, making possible the implementation of 6 to 8 bits DACs in usual CMOS technologies that can operate in the MS/s range with supply voltages as lower than 200mV.

As shown in this work, there are two main difficulties that impact in the reduction of the accuracy, or effective number of bits (ENOB) of this DAC topology: intrinsic nonlinearity of the ladder and MOSFET mismatch variability.

The intrinsic nonlinearity was not the focus of this work because, as a deterministic effect, it can be reduced through some design strategies that were presented in chapter 3: using a symmetrical ladder, or resizing the transistors to optimize the linear current division, or also by applying a data predistortion in the digital values to be converted.

Since the intrinsic nonlinearity can be corrected, this work focused on the MOSFET mismatch variability impact, presenting in chapter 4 a methodology that can be used to establish a tradeoff among accuracy, supply voltage and device area, in the design of M–2M MOSFET ladders. This methodology was developed using an all–region MOSFET mismatch model, being used in the design of some M–2M DAC ladders of 6 and 8 bits using standard, low and zero threshold voltage MOSFETs (SVT, LVT and ZVT). The post-layout parasitics of these DACs were extracted and their dynamic performance was also simulated besides their static behavior.

From the simulation results it became clear that the use of lower V_T MOSFETs results in lower mismatch errors in the DAC current divisions, since the MOSFETs operate in higher inversion levels with the same supply voltage. Also, the use of lower V_T MOSFETs imply in more critical intrinsic nonlinearity for the asymmetrical ladder, but it can be corrected by the presented techniques in section 3.3.1.

Tables 4.1 and 4.2 compile the post-layout simulation results of all converters designed in this work. In these tables we are showing the INL and ENOB separated for the errors caused by mismatch only which is our main concern, and for the total errors including the intrinsic nonlinearity if not corrected.

We calculated the ENOB based on Eq. 4.2, which is found in BAKER (2010) and was adapted to our case.

$$ENOB = \log_2\left(\frac{I_{Ref}}{INL}\right) - 1 \quad (4.2)$$

where I_{Ref} is the current generated by V_{Ref} and the INL is not normalized to LSB.

Table 4.1: Comparison between performances of all converters designed in this work with $V_{Ref} = 200mV$. Results for post-layout extraction simulated on Virtuoso.

Supply Voltage	200mV	200mV	200mV	200mV
Transistor Type	Standard	Low- V_T	Zero- V_T	Low- V_T
Resolution	6-bit	6-bit	6-bit	8-bit
σ_{INL} (LSB) ¹	0.3	0.15	0.08	0.15
$3 \times \sigma_{INL}$ (LSB) ¹	0.9	0.45	0.24	0.45
ENOB (3σ) ¹	5.1	5.8	7.1	8.1
INL (LSB) (3σ) ²	± 1.2	± 1.4	± 1.74	-14.5/+27.5
ENOB (3σ) ²	4.7	4.5	4.2	2.5
Max Sampling Frequency (MS/s)	5.13	9	13.5	-
Power Consumption (μW)	0.4	2.7	4.5	30
Area (mm^2)	0.024	0.024	0.0246	0.195

Table 4.2: Comparison between performances of all converters designed in this work with $V_{Ref} = 100mV$. Results for post-layout extraction simulated on Virtuoso.

Supply Voltage	100mV	100mV	100mV	100mV
Transistor Type	Standard	Low- V_T	Zero- V_T	Low- V_T
Resolution	6-bit	6-bit	6-bit	8-bit
σ_{INL} (LSB) ¹	0.4	0.2	0.1	0.25
$3 \times \sigma_{INL}$ (LSB) ¹	1.2	0.6	0.3	0.75
ENOB (3σ) ¹	4.7	5.2	6.9	7.4
INL (LSB) (3σ) ²	± 1.55	± 1.8	± 2.2	-15.7/+17.7
ENOB (3σ) ²	4.4	4.1	3.9	3
Max Sampling Frequency (MS/s)	1.7	-	-	-
Power Consumption (μW)	0.0132	0.28	0.75	3.2
Area (mm^2)	0.024	0.024	0.0246	0.195

We found a bunch of works about AD converters operating at low voltage but we did not found anyone about DACs. For this reason we created Tab. 4.3 comparing the standard 6-bit converter designed in this work with some state of art ADCs already published. Let's highlight some things that can actually be compared. In terms of supply voltage we are working on the same level and the INL is almost the same that in DALY; CHANDRAKASAN (2009). Area and power are quite hard to compare since ADCs consider other circuits in its design. Our work has better power consumption than two others but is still far from LIN; HSIEH (2015), where they focused on reducing the DAC power consumption achieving $0.035 \mu W$ total and $0.01 \mu W$ just on the DAC, tested at 90kS/s, while our consumption was evaluated at 10kS/s.

On Tab. 4.4 we compiled some high speed DACs, which is a very common field of study, and compared with our low consumption DAC. The high sampling frequencies are achieved at cost of high consumption and since they are working at nominal supply, their

¹MOSFET mismatch errors only (intrinsic ladder nonlinearity removed).

²MOSFET mismatch and intrinsic ladder nonlinearity considered together.

¹MOSFET mismatch errors only (intrinsic ladder nonlinearity removed).

²MOSFET mismatch and intrinsic ladder nonlinearity considered together.

INL is quite low, so mismatch is not an issue. Even so, we can see that our consumption is far below the others maintaining a reasonable area.

To conclude, the variability effects given by mismatch were predicted by our methodology with reasonable accuracy. This is supported by the small difference between analytical and Monte Carlo simulated results. Besides, we can say that for weak inversion our results are even more accurate, because the mismatch model was built upon an all-region MOSFET model.

The DACs designed with 6 bits SVT, 8 bits LVT and 6 bits ZVT were fabricated in the IBM 130nm RF process and will be characterized as soon as possible.

Table 4.3: Comparison between state of art ADCs and this work.

(*)simulation results	LIN; HSIEH (2015)	DALY; CHANDRAKASAN (2009)	WISMAR et al. (2006)	This work	Unit
Converter Type	SAR ADC	Flash ADC	$\Sigma\Delta$ ADC	M-2M DAC	-
Technology	90	180	90	130	nm
Supply Voltage	0.3	0.4	0.2	0.2	V
Resolution	10-bit	6-bit	8-bit	6-bit	-
INL	-0.66/+0.4	-0.9/+0.72	-	0.9*	LSB
ENOB	8.4	5.05	7.6	5.1*	-
Silicon Area	0.031	1.96	0.02	0.024	mm^2
Power Consumption	0.035 (0.01 on DAC)	1.66	0.44	0.4*	μW

Table 4.4: Comparison between other DACs and this work.

(*)simulation results	CHAKIR et al. (2015)	CHEN; CHANG (2012)	JUNG et al. (2008)	This work	Unit
Converter Type	Current Steering	Current Steering	Current Steering	M-2M DAC	-
Technology	180	90	180	130	nm
Supply Voltage	1.8	1.2	1.8	0.2	V
Resolution	6-bit	6-bit	6-bit	6-bit	-
Power Consumption	945	8320	6000	0.4*	μW
Silicon Area	0.006	0.045	0.0576	0.024	mm^2
Sampling Frequency	300M	3G	1.25G	5.1M (Typical)*	S/s
ENOB	-	-	5.97	5.1*	-
INL	-0.1/+0.04	+ -0.07	+ -0.1	0.9*	LSB

5 CONCLUSIONS

In this work we made use of a known topology to develop a digital to analog converter operating at very low supply voltage. For this circuit, the error caused by the mismatch is the most critical effect and more difficult to deal with. We proposed a methodology that can estimate errors caused by MOSFETs mismatch operating at low supply voltages related to their active area. Furthermore, the mismatch model used is based on a MOSFET model valid in all operating regions, thus enabling an accurate analysis of the converter when working in weak inversion.

The method was validated by Monte Carlo post-layout simulation in Cadence tool Virtuoso, using converters with 6 and 8 bits of resolution, voltage supplies of 100mV and 200mV, and different transistors (standard and lower V_T devices). During the results evaluation was perceived an additional effect given by the asymmetry of our topology. The converter intrinsic nonlinearity eventually inserts a certain amount of error, which is larger when lower V_T transistors are used. It was also said that this effect can be easily mitigated with simple correction techniques such as: resizing the transistors to optimize the linear current division, use of symmetrical ladder network or applying a data predistortion in the digital values to be converted.

The obtained results are promising. A 6-bit converter with standard transistors can operate below 200mV of supply voltage, keeping an INL of 0.9 LSB for 3σ , maximum sampling frequency of 5 MS/s and occupying an area of $0.024mm^2$. Furthermore, it is possible to make use of lower V_T devices to improve some performances, for example, a 6-bit converter using Low- V_T devices presented an INL of 0.45 LSB (if correcting the intrinsic nonlinearity) and a maximum sampling frequency of 9 MS/s. Of course that the speed is higher at cost of higher consumption.

Another important fact of these low V_T converters is that for a same supply (when comparing to standard V_T) the inversion level is higher, which implies in less error given by the mismatch allowing a converter design with smaller area.

5.1 Future Works

The next step of this study is measure the manufactured circuits. Throughout the text we said that three converters were sent to tape-out: 6-bit SVT M–2M DAC, an 8-bit LVT M–2M DAC and a 6-bit ZVT M–2M DAC. The total area occupied is $1.4mm \times 0.2mm$ divided in $1.2mm \times 0.16mm$ for the 8-bits LVT DAC, $0.24mm \times 0.1mm$ for the 6-bits SVT DAC and $0.246mm \times 0.1mm$ for the 6-bits ZVT DAC. To measure the circuits a bring-up PCB is being designed to access pins and an interface with a computer will be made, as explained in Fig. 5.1. The idea is to insert a serial signal on the shift register and excite the three converters in sequence. There are 15 chips to be measured.

In sequence, some points raised in this work should be evaluated, for example the construction of a symmetrical network to solve the intrinsic nonlinearity issue. Then, we intend to include the digital block using low voltage logic MELEK et al. (2014).

After that, the design of low supply voltage comparators would be investigated for implementation of low voltage A/D converters.

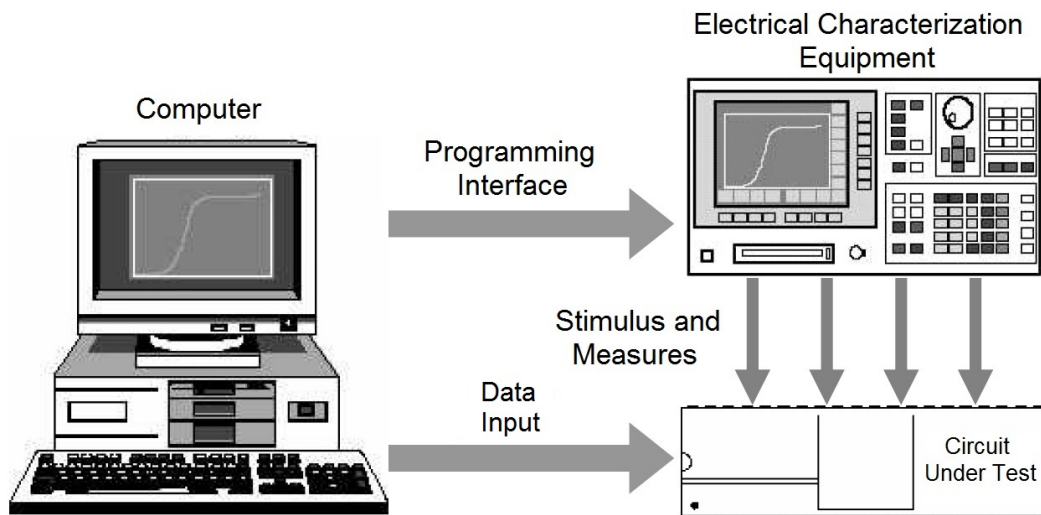


Figure 5.1: Test setup for measurements.

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APPENDIX A LIST OF PUBLICATIONS

SPEROTTO, I., KLIMACH, H. and BAMPI, S. "MOS-only M-2M DAC for Ultra-Low Voltage Applications". VI Latin American Symposium on Circuits and Systems (LAS-CAS'15), Montevideo, Uruguay. February 2015.

SPEROTTO, I., KLIMACH, H. and BAMPI, S. "Design and Linearity Analysis of a M-2M DAC for Very Low Supply Voltage". 15th Microelectronics Students Forum (SFORUM'15), Salvador, Bahia. September 2015.

SPEROTTO, I., KLIMACH, H. and BAMPI, S. "Design and Linearity Analysis of a M-2M DAC for Very Low Supply Voltage". 2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS'15), Cairo, Egypt. December 2015.

APPENDIX B MISMATCH MODEL CONSIDERATIONS

A comparison between the mismatch model used in this work (Eq. 3.3) and the Pelgrom's mismatch model used by the Cadence tool, Virtuoso is important to see if the results are behaving as expected.

A routine was implemented on Matlab in order to calculate the coefficient of variation $\frac{\sigma_{I_D}}{I_D}$ as a function of the gate voltage of a standard NMOS transistor, configured as shown in Fig. B.1, in the IBM 130 nm process.

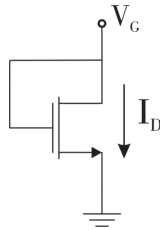


Figure B.1: Standard NMOS transistor diode connected.

We then ran Monte Carlo simulations of the same transistor under same biasing with 100 points on each biasing voltage and depicted the two approaches on Fig. B.2 as a function of gate voltage, which is directly related to the inversion level (i_f).

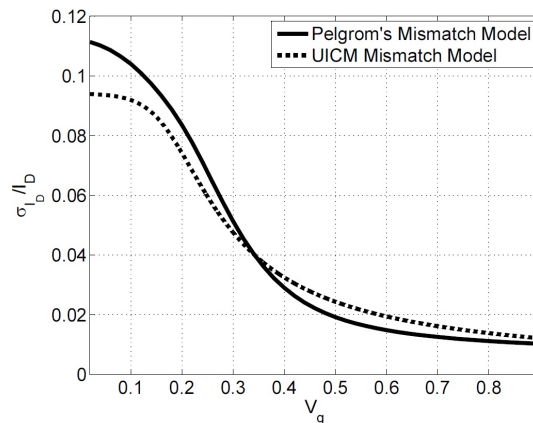


Figure B.2: Comparison between the UICM Mismatch model used in this work and the Pelgrom's Mismatch model.

It becomes clear that for low gate voltages our model is more optimistic. In this technology the threshold voltage is around $200mV$, so we roughly can say that our model has a better behavior in moderate and weak inversion ($i_f < 100$) and is slightly worst in strong inversion.

APPENDIX C MATLAB CODE

In this appendix we present the Matlab code used to calculate every step detailed in chapter 3. We explain briefly each part of the code taking as basis the standard 130 nm process.

First we define all variables needed as shown in C.1. The most important here is to extract the correct values from PDK. Most of them can be found in the foundry documents, but some of them must be extracted from the design kit itself with aid of the Virtuoso tool.

Variables like V_{ref} , V_g and N are of our choice, or depends on the application. We can set the aspect ratio on this code, but at first, like previously demonstrated, it's interesting to make a design space exploration. Since mismatch is directly related to the area, we can make the "Area" variable as a vector, this way building graphics like the ones showed in figures 3.13 and 4.7.

Parameters V_t , μ and I_{sq} were extracted using the Virtuoso tool and T_{ox} , ϵ_s , K_{Vt} and $B_{I_{sq}}$ were taken on the foundry documents. The other parameters are widely known (ϕ_t , q , etc.) and variable MC must be the same number of Monte Carlo simulations we intent to perform on Virtuoso.

When considering a normal distribution sample, the reliability of the statistical parameters (mean and standard deviation) is related to the sample size (N) from the following approximate equation.

$$Reliability = \frac{1}{\sqrt{N}} \quad (C.1)$$

In the simulations we are using $N = 500$ samples, resulting an approximate error of 4,4% in the statistical calculation.

Listing C.1: Code part 1: variables and parameters definition.

```
% Variables definition.
Vref=200e-3; % Supply.
Vg=200e-3; % Gate biasing.
Vs=0; % Source terminal supply (Always zero in this case).
Vt=0.1967; % NFET transistors threshold voltage, considering Vsb=0.
W=25; % Transistor Width (um).
L=10; % Transistor Length (um).
N=6; % Converter number of bits.
S=W./L; % Aspect ratio.
Area=W.*L; % Transistor area (um^2).
MC=500; % Monte Carlo runs.

% Process parameters and constants.
n=1.35; % Slope Factor. Between 1.2 e 1.3 for 0<Vg<1.5. Given by 1+(gamma/(2*sqr(Vp+2*Phi_f))).
u=440e8; % Channel effective mobility (um^2/V*s).
Tox=3.03e-3; % Oxide thickness (um).
Es=3.4*8.854e-18; % Permissiveness.
Cox=Es/Tox; % Oxide Cap. (F/um^2).
phi_t=26e-3; % Thermal voltage (V).
q=1.602e-19; % Electron charge.
K_vt=1.35e-2; % Pelgrom's Avt (V*um). This parameter gives a 3 sigma result.
Bisq=3e-6; % Mismatch parameter (specific current). K_beta on the PDK.
```

```

Io=u*n*Cox*(phi_t^2)*exp(1); % Constant.
Isq=243.7472e-9; % Specific Current.
Is=Isq.*(W./L); % Specific Current for different aspect ratios.
Nx=(n*Cox*phi_t)/q; % Mismatch equation constant.
Noi=(K_vt*Cox/q)^2; % Mismatch parameter, approximated by K_vt.

```

The second listing (C.2) is responsible for the current weighting related to the sensitivity. The sensitivity of each branch related to the others are represented by the straight and reverse mitigating factors. The matrix is shaped by the number of bits previously defined with a maximum of 8 bits, but this can be easily increased by adding some rows and columns to it.

Listing C.2: Code part 2: sensitivity matrix.

```

% Mitigation factors (straight).
bb=2/3;
cc=2/3;
dd=2/3;
ee=2/3;
ff=2/3;
gg=2/3;

% Mitigation factors (reverse).
hh=1/3;
ii=1/3;
jj=1/3;
kk=1/3;
ll=1/3;
mm=1/3;
nn=1/2;

% Sensitivity Matrix
MV = [ -1      0      0      0      0      0      0      0
        nn     -1     bb     bb*cc     bb*cc*dd     bb*cc*dd*ee     bb*cc*dd*ee*ff     bb*cc*dd*ee*ff*gg
        nn/2   hh/2   -1     cc     cc*dd     cc*dd*ee     cc*dd*ee*ff     cc*dd*ee*ff*gg
        nn/4   hh/4   ii/2   -1     dd     dd*ee     dd*ee*ff     dd*ee*ff*gg
        nn/8   hh/8   ii/4   jj/2   -1     ee     ee*ff     ee*ff*gg
        nn/16  hh/16  ii/8   jj/4   kk/2   -1     ff     ff*gg
        nn/32  hh/32  ii/16  jj/8   kk/4   ll     -1     gg
        nn/64  hh/64  ii/32  jj/16  kk/8   ll/2   mm     -1     ];

MV = MV(1:N,1:N);

```

In listing C.3 we calculate all inversion levels and mismatch variations of the ladder transistors using the UICM equations presented in section 3.1.

Listing C.3: Code part 3: M–2M ladder solution.

```

% Equating.
% Inversion level
i_f=Io./Is.*(W./L).*exp((Vg-Vt-n.*Vs)/(n.*phi_t));
i_r(1,:)=Io./Is.*(W./L).*exp((Vg-Vt-n.*Vref)/(n.*phi_t));

% Solving M-2M ladder.
for i=1:N
    i_x(i,:)=(i_f+i_r(i,:))./2;
    i_r(i+1,:)=i_x(i,:);
    Vd(i,:)=(Vg-Vt)./n - phi_t.*(log(sqrt(1+i_r(i,:))-1)+sqrt(1+i_r(i,:))-2);
    Vx(i,:)=(Vg-Vt)./n - phi_t.*(log(sqrt(1+i_x(i,:))-1)+sqrt(1+i_x(i,:))-2);
    Id(i,:)=Is.*(i_f-i_x(i,:));
    Sia(i,:)=sqrt((Noi./(W.*L.*(Nx.^2))).*(1./(i_f-i_x(i,:))).*(log((1+i_f)/(1+i_x(i,:))))+Bisq^2);
    Sib(i,:)=sqrt((Noi./(W.*L.*(Nx.^2))).*(1./(i_x(i,:)-i_r(i,:))).*(log((1+i_x(i,:))/(1+i_r(i,:))))+Bisq^2);
    Sigma_ia(i,:)=Sia(i,:).*Id(i,:);
    Sigma_ib(i,:)=Sib(i,:).*Id(i,:);
end

```

The simple code showed in listing C.4 generates a random vector with MC values and a standard deviation σ that was calculated in the previous code.

Listing C.4: Code part 4: sample space generation.

```
for l=1:N
vector(1,:) = random('normal',0,Sigma_ia(1),[1 MC]);
end
```

In listing C.5 we calculate the output current of the converter. In the first line we multiply the random vector by the sensitivity matrix creating a new matrix with the real variation. Then we sum the real variation to the current on each branch. Lines 3, 4 and 5 of this code part are responsible to create a vector with all 2^N possible combinations of current outputs. Finally the code calculates the Full Scale and normalize it to the LSB.

Listing C.5: Code part 5: output current calculation.

```
for j=1:MC
Real_var2(:,j) = sum(bsxfun(@times,vector(:,j)',MV),2);
Ix2(:,j) = wrev(Id) + wrev(Real_var2(:,j));
m = (dec2bin(0:(2^N)-1)=='1'); % Matrix of values summed with the real variation (Real_var)
M = flip1r(m); % Binary matrix of N bits.
% Horizontal flip of "m".
I_out2(:,j) = sum(bsxfun(@times,M,Ix2(:,j)'),2);
FS2(:,j) = max(I_out2(:,j)) - min(I_out2(:,j));
I_lsb2(:,j) = FS2(:,j)/(2^N);
end
```

Listing C.6 present the linearization process. First getting the minimum and maximum values of the output and then drawing a straight line between them. This code as well calculate the Integral nonlinearity (INL).

Listing C.6: Code part 6: linearization process.

```
for k=1:MC
x(:,k)=min(I_out2(:,k));
y(:,k)=max(I_out2(:,k));
z(:,k)=(y(:,k)-x(:,k))/(2^N-1);

lin(:,k)=[x(:,k):z(:,k):y(:,k)];

INL(:,k)=(I_out2(:,k) - lin(:,k));
INL2(:,k)=(I_out2(:,k) - lin(:,k))/I_lsb2(:,k);
end
```

The last code (C.7) calculates the standard deviation of the INL. All relevant values and vectors were plotted and showed throughout this work.

Listing C.7: Code part 7: standard deviation.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%Error standard deviation%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
desvio=std(INL');
desvio2=std(INL2');
```

APPENDIX D SUMMARY IN PORTUGUESE

D.1 Introdução

Neste capítulo são apresentados os principais assuntos que serviram como motivação para a realização deste trabalho, tais como a redução na tensão de alimentação ao longo do tempo e circuitos que operam com baixíssima tensão de operação. É realizada uma pequena revisão da evolução dos conversores quando relacionados a tensão de alimentação. Finalmente explicitamos os principais objetivos dessa dissertação e descrevemos a estrutura do trabalho.

D.1.1 Redução da Tensão de Alimentação em Circuitos Eletrônicos

Nas últimas décadas temos observado um incrível aumento na densidade de integração e na complexidade computacional de circuitos digitais. A redução no tamanho de elementos essenciais de circuitos integrados, tal como o tamanho mínimo de canal dos transistores, se deu através dos avanços tecnológicos na fabricação destes. Para ilustrar temos a Fig. 1.1, que apresenta a evolução do tamanho mínimo de canal, iniciando nos anos sessenta, e se projetando dentro do século 21.

Uma análise na redução do tamanho dos dispositivos (*scaling*) realizada por RABAEY (2002) mostrou de que maneira a tensão de alimentação tem sido afetada pela redução no tamanho mínimo dos dispositivos. Diferentes cenários relacionados ao *scaling* foram apresentados, como *full scaling*, *general scaling* e *fixed-voltage scaling*. Na verdade, *full scaling* não é uma opção interessante. Primeiramente, para que os novos dispositivos sejam compatíveis com as tecnologias existentes, a tensão não pode ser dimensionada arbitrariamente. Fornecer múltiplas tensões de alimentação ao sistema acaba por encarecer muito o custo de produção. Como resultado, as tensões não pode ser reduzidas diretamente com o tamanho dos dispositivos, dessa maneira os projetistas preferem aderir a padrões bem definidos de tensão de alimentação e nível de sinal. Conforme ilustrado na Fig. 1.2, 5 V era o padrão para todos componentes digitais no início dos anos 90, portanto um modelo de tensão fixo para o *scaling* foi seguido.

Com a introdução do nó tecnológico de $0.5\mu m$, os novos padrões de 3.3V e 2.5V trouxeram mudanças. Hoje em dia tem se observado uma relação mais próxima entre tensão de alimentação e tamanho dos dispositivos, auxiliados pelo modelo de *scaling* de tensão fixa. O “*International Technology Roadmap for Semiconductors*” ITRS (2013) é responsável por prever aspectos importantes da indústrias de semicondutores. Neste caso estamos interessados na tensão de alimentação, sendo assim, utilizando o modelo de *scaling* de tensão fixa, a compilação mais recente do avanço da tensão de alimentação em relação ao nó tecnológico é apresentado na Tab. 1.1.

Esta análise fornece uma visão mais ampla dos avanços tecnológicos da industria

de semicondutores, o que nos leva a próxima seção onde apresentamos alguns circuitos elétricos trabalhando com baixíssima tensão de alimentação.

D.1.2 Circuitos eletrônicos para baixíssima tensão de alimentação

A evolução contínua das tecnologias CMOS é o principal fator por trás da operação a baixa tensão, rapidamente atingindo alimentações abaixo de 1 V para nós de tecnológicos abaixo de 130 nm. Os sistemas atuais, operados por bateria, ou os futuros auto-alimentados e auto-sustentáveis requerem muito baixo consumo de potência, em torno de alguns nA até alguns μA dependendo da função a ser executada RABAEY et al. (2007).

A energia disponível é muito pequena, portanto é muito importante que o projeto de um dispositivo computacional ou de comunicação tenha baixíssimo consumo de potência. Vamos apresentar agora alguns circuitos e soluções sobre este tópico. Com a evolução dos MEMS e das tecnologias de semicondutores se tornou possível a integração completa entre aquisição, computação e comunicação em dispositivos cada vez menores. Isso abre portas para um desenvolvimento ubíquo em áreas de difícil acesso. Nestes casos a substituição de baterias é virtualmente impossível e a reposição de energia através da extração (*energy harvesting*) é essencial. Mais recentemente, pesquisadores tem identificado amplas possibilidades de extrair energia do ambiente e desta maneira foram desenvolvidos extratores muito eficientes. Ainda assim, a energia disponível é muito pequena, portanto circuitos com baixíssimo consumo, tanto para computação quanto para comunicação, são de absoluta necessidade.

Naturalmente que algumas questões mais complicadas aparecem quando se tratando da entrega eficiente de energia para o circuito. A eficiência do extrator normalmente depende das condições de operação. Por exemplo: o ambiente pode ter pouca luz; é necessário armazenamento de energia se os ciclos operacionais do extrator estão fora de fase; as tensões e correntes entregues pelo extrator normalmente não são compatíveis com as necessidades do circuito. Para superar esses problemas é comumente utilizada a arquitetura mostrada na Fig. 1.3.

A partir deste diagrama podemos relacionar inúmeras aplicações em uso hoje em dia. Através de sensores de vibração, solar e térmicos, conforme mostrados na Fig. 1.4, podemos extrair a energia e converter temporariamente em um reservatório de energia. Essa energia armazenada pode ser utilizada para acionar diferentes tipos de circuitos.

É preciso ter em mente que os níveis de energia são realmente baixos, sendo assim estes circuitos devem ter baixo consumo. Apenas para esclarecer, a Fig. 1.5 foi tirada do site da empresa *Texas Instruments* e mostra a energia estimada que pode ser extraída de diferentes fontes.

Uma aplicação muito interessante é de um monitor de pressão intra-ocular (IOPM), mostrado na Fig. 1.6, que foi implantado no olho de um paciente com glaucoma. Este dispositivo foi apresentado por CHEN et al. (2011) e utiliza uma bateria de filme fino de lítio com capacidade de corrente de 1 μAh . A vida útil deste dispositivo é de 28 dias sem se utilizar de técnicas de *energy harvesting*. Para aumentar a vida útil deste dispositivo utilizou-se uma célula integrada de captação de energia solar com uma área de 0.07mm^2 que recarrega a bateria. Devido a esta célula solar, o circuito adquire autonomia energética com apenas 10 horas de luz ambiente ou uma hora e meia de luz solar.

Tudo isso foi dito para reforçar a importância deste trabalho. Circuitos de baixo consumo são sem dúvida uma das áreas de pesquisa mais importantes atualmente.

D.1.3 Conversores de Sinal Digital e Analógicos

De todos os circuitos que podem servir de material de estudo operando em baixa tensão, esta dissertação se concentra em conversores de dados. Este tipo de circuito aparece em inúmeras aplicações como eletrônicos de consumo, comunicações, computação e controle, instrumentação, etc.. Os conversores de dados surgiram na década de 80 como solução para processamento de sinal. Processamento digital de sinais (DSP) se mostrou mais eficiente e acabou por substituir diversas aplicações de circuitos analógicos. O diagrama de blocos da Fig. 1.7 mostra como são usados comumente conversores A/D e D/A.

A conversão envolve a quantização da entrada que necessariamente introduz uma pequena quantidade de erro. Ao invés de realizar uma conversão simples, um conversor analógico para digital (ADC) normalmente realiza conversões (“amostra” a entrada) periodicamente. Como resultado tem-se uma sequência digital de valores que foram convertidos do tempo contínuo e amplitude analógico para tempo discreto e amplitude digital do sinal. A operação inversa é realizada por um conversor digital para analógico (DAC).

A performance de um conversor pode ser avaliada de diversas maneiras. Resolução, tensão de alimentação, frequência de amostragem, consumo de potência e área são usualmente os mais importantes quando se projeta um conversor. Há ainda outras preocupações ligadas às já mencionadas como o processo tecnológico, que afeta diretamente a tensão de alimentação e a área, Não-linearidade Integral e Diferencial (INL e DNL), número efetivo de bits (ENOB), distorção harmônica entre outros.

Conforme mostrado por JONSSON (2010), a tensão de alimentação pode variar em torno de uma ordem de magnitude para o mesmo nó tecnológico para conversores de dados analógicos para digital (ADCs). A Figura 1.10 é uma compilação de trabalhos mostrando a máxima tensão de alimentação aplicada a cada conversor e sinalizando a evolução dos conversores estado-da-arte ao longo do tempo. Considerando que conversores digital para analógico são uma parte essencial em conversores A/D a mesma regra se aplica a eles.

Pesquisas mais recentes estão focando em conversores de baixo consumo para aplicações específicas. O *Flash* ADC desenvolvido por DALY; CHANDRAKASAN (2009) opera na faixa de 0.2 V a 0.9 V e tem 6-bits de resolução. O objetivo deste conversor é ser eficiente energeticamente e possui uma figura de mérito (FoM) de 125 fJ/passos-de-conversão a 0.4 V, onde atinge um ENOB de 5.05 a uma frequência de amostragem de 400 kS/s. É importante ressaltar que esta topologia utiliza um conversor D/A de realimentação capacitiva com 5-bits de resolução para cancelar os *offsets* dos comparadores.

Hoje em dia, circuitos energeticamente eficientes estão se tornando mais e mais importantes. Sensores que detectam e monitoram sinais biomédicos são um exemplo deste tipo de circuito. Os sinais adquiridos são usualmente digitalizados por conversores A/D com moderada resolução (8 – 12 bits) e taxa de amostragem de (1 – 1000 kS/s). Dentre várias arquiteturas de conversores A/D, o conversor do tipo SAR (aproximações sucessivas) tem uma melhor eficiência energética. Ele ainda se beneficia da redução do tamanho mínimo dos dispositivos porque é composto principalmente de circuitos digitais que se tornam mais rápidos em tecnologias mais avançadas. LIN; HSIEH (2015) desenvolveu um SAR ADC com 0.3 V de alimentação e 10 bits de resolução. Eles utilizaram uma técnica de chaveamento no DAC sem tensão de modo comum de maneira que o consumo de chaveamento foi reduzido em 83%. O diagrama do circuito é apresentado na Fig. 1.11 e ele atingiu um FoM of 1.78 fJ/passos-de-conversão.

D.1.4 Motivação

Já demonstramos a importância dos conversores de sinal dentre os diversos circuitos eletrônicos e também mostramos uma forte tendência a obter circuitos operando com baixíssima tensão. Circuitos que operam dentro dessas especificações normalmente apresentam grandes desafios de projeto. Este trabalho foca em conversores D/A, mais especificamente na topologia CMOS R–2R *ladder*. Esta topologia em particular parece ser bastante apropriada para trabalhar com operação em baixíssima tensão pois os transistores podem realizar a conversão trabalhando na região de sub-limiar e triodo. Ao longo deste trabalho será demonstrada uma metodologia de projeto que estabelece relações de compromisso entre resolução, área, frequência de amostragem e tensão de alimentação.

D.1.5 Organization

Este trabalho é organizado da seguinte maneira: uma revisão na evolução dos conversores de dados é realizada no capítulo 2. O modelo de MOSFETs utilizado e o projeto do conversor D/A operando em baixa tensão é apresentado no capítulo 3. Os resultados das simulações pós-layout são apresentados e discutidos no capítulo 4. No capítulo 5 são feitas as conclusões e nos apêndices são feitas algumas considerações sobre o modelo de *mismatch*.

D.2 Resumo do texto

O segundo capítulo contempla a revisão bibliográfica do trabalho. Primeiramente é feita uma revisão minuciosa da rede R–2R desde os primeiros conversores deste tipo até estudos mais recentes sobre seu comportamento. Na sequência é feita uma revisão da topologia que é o foco deste trabalho, a rede M–2M, onde é explicado o uso de transistores invés de resistores bem como uma análise da evolução de seu uso e os estudos realizados em cima desta rede. Por fim é feita uma revisão geral de todos os tipos de conversores trabalhando com baixa tensão de alimentação.

O terceiro capítulo trata do projeto do circuito em si. Primeiramente é mostrado o modelo de MOSFETs utilizado (UICM) SCHNEIDER; GALUP-MONTORO (2010), bem como seu correspondente modelo de descasamento GALUP-MONTORO et al. (2005). Mostramos o princípio de divisão binária de corrente que ocorre no conversor em questão partindo das propriedades de divisão de corrente explanadas por BULT; GEELLEN (1992). Na sequência é descrito o funcionamento completo da rede M–2M e todas suas características pertinentes ao seu uso em baixa tensão. São explicadas também algumas características não-lineares intrínsecas à topologia e maneiras de resolver este problema. A metodologia de projeto também é explicada neste capítulo. O método para encontrar todos os níveis de inversão intermediários e a sensibilidade da rede é detalhadamente explicado com um exemplo prático usando como base o processo tecnológico de 130 nm. Mostramos também cuidados relativos a determinação do comprimento de canal mínimo que deve ser utilizado para evitar erros de segunda ordem. Por fim mostramos o espaço de projeto que relaciona o erro de não linearidade integral do conversor com a área de um transistor e sua resolução. Por fim é mostrado como erros de *offset* e ganho aparecem no conversor.

No quarto capítulo são apresentados os resultados de simulação em layout extraído. Primeiramente mostramos o erro de *mismatch* para três conversores de 6 e 8 bits com 3 diferentes dispositivos MOS. Os resultados de desempenho no domínio do tempo são

mostrados na sequência. Por fim, uma análise em frequência, mostrando a transformada de Fourier discreta, estima as velocidades de operação dos conversores projetados. Ainda neste capítulo fazemos uma compilação dos resultados obtidos e comparamos com conversores estado-da-arte já fabricados. Os resultados são mostrados nas tabelas 4.1, 4.2, 4.3 e 4.4.

D.3 Conclusão

Neste trabalho utilizamos uma topologia bastante conhecida para desenvolver um conversor D/A operando com tensões de alimentação baixíssimas. Para este circuito o erro causado pelo *mismatch* é o efeito mais crítico e mais difícil de lidar. Propusemos uma metodologia que estima o erro causado pelo *mismatch* dos MOSFETs operando com tensões muito baixas em relação a sua área ativa. Além disso, o modelo de *mismatch* utilizado é baseado em um modelo de MOSFETs válido em todas regiões de operação, proporcionando uma análise precisa do conversor quando operando em inversão fraca.

O método foi validado através de simulações Monte Carlo na ferramenta da Cadence, Virtuoso, utilizando conversores de 6 e 8 bits de resolução, tensões de alimentação de 100mV e 200mV, e diferentes tipos de transistores. Durante a avaliação dos resultados percebemos um efeito adicional devido a não-simetria da topologia utilizada. Este efeito chamado de não-linearidade intrínseca eventualmente insere uma certa quantidade de erro, que se torna maior quando utilizamos transistores com tensão de limiar mais baixas. Foi demonstrado também que este efeito pode ser mitigado com simples técnicas, tais como o redimensionamento dos transistores visando otimizar a divisão linear de corrente, o uso de uma rede simétrica ou ainda aplicar uma pré-distorção nos valores digitais a serem convertidos.

Os resultados obtidos são promissores. Um conversor de 6-bits com transistores padrões da tecnologia pode operar com tensão de alimentação abaixo de 200mV mantendo um INL de até 0.9 LSB para até 3 σ , uma frequência de amostragem máxima de 5 MS/s ocupando uma área de $0.024mm^2$. Além disso, é possível utilizar transistores com tensão de limiar reduzida para melhorar a performance, por exemplo, um conversor com os mesmos 6-bits fazendo uso destes transistores apresentou um INL de 0.45 LSB (quando corrigida a não-linearidade intrínseca) e máxima frequência de amostragem de 9 MS/s. Naturalmente que a velocidade é maior ao custo de uma maior consumo.

Outro ponto importante é que estes conversores com transistores de menor tensão de limiar apresentam um maior nível de inversão para uma mesma tensão de alimentação, em se comparando com os transistores padrão da tecnologia. Isto implica em um conversor com menor erro de *mismatch* e por consequência a possibilidade de se utilizar uma área menor.

D.3.1 Trabalhos Futuros

O próximo passo é medir os circuitos fabricados. Ao longo deste trabalho dissemos que três conversores foram fabricados: um com 6 bits de resolução utilizando transistores padrão, um com 8 bits e transistores de reduzida tensão de limiar e outro de 6 bits com tensão de limiar em torno de zero. A área total ocupada é de $1.4mm \times 0.2mm$ dividida em $1.2mm \times 0.16mm$ para o conversor de 8 bits e $0.24mm \times 0.1mm$ para cada um dos outros 2 conversores de 6 bits. Para medir os circuitos uma placa de circuito impresso (PCB) está sendo desenhada para acessar os pinos e uma interface com o computador será feita conforme exemplificado na Fig. 5.1. A ideia é inserir um sinal em série no

registrador digital que por sua vez acionará os três conversores na sequência. Existem 15 amostras para serem medidas.

Na sequência alguns pontos elucidados neste trabalho devem ser melhor analisados, como por exemplo a construção de uma rede simétrica para resolver as questões de não-linearidade intrínsecas. Então pretendemos incluir uma lógica digital que também funcione com baixa tensão de alimentação MELEK et al. (2014).

Depois disso será investigado o projeto de conversores operando em baixa tensão com o objetivo de fazer conversores A/D também operando com baixa tensão.