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CMOS linear RF power amplifier with fully integrated power combining transformer

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“Great ambition is the passion of a great character.
Those endowed with it may perform very good or very bad acts.
All depends on the principles which direct them.”

— Napoleon Bonaparte

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ABSTRACT

This work presents the design of a fully integrated Radio-frequency (RF) linear Power Amplifier(PA) in complementary metal-oxide silicon (CMOS) technology. In this work we analyse the challenges in CMOS PA design as well as the state-of-the-art solutions. One such challenge presented by this technology is the low supply voltage and high-loss passives, which pose severe limits on the output power and efficiency achieved with traditional PA design methods and load impedance transformation networks. This issue is addressed by the use of on-chip, highly efficient power combining networks such as the one in this work: A series combining transformer (SCT).

The problem of using CMOS becomes even more critical for recent communications standards that require high transmitter linearity such as the ones used for wireless local area network (WLAN) or 3G and 4G mobile communications. This requirement is such that the PA operate at a high power back-off from its optimum operating point, degrading efficiency. To address this problem linearization techniques such as digital pre-distortion can be used in order to decrease the necessary power back-off. In this work an analog technique of AM-PM distortion compensation is used to linearize the capacitance at the input of the amplifier's transistors and reduce this type of distortion that severely impacts the error vector magnitude (EVM) of the signal.

The design process is detailed and aims to make evident the trade-offs of PA design and particularly the impact of harmonic termination and the quality of passives on the load transformation network, the series combining transformer design is optimized for common-mode impedance tuning used for 2nd harmonic termination. The circuit has only a single amplifying stage due to its area being limited to 1.57 x 1.57 mm^2 and the design is very constrained by this fact.

The PA simulated performance is analyzed under various metrics. It achieves a simulated maximum output power of 24.4 dBm with a drain efficiency of 24.53% and power added efficiency (PAE) of 22%. The PA has a very flat power gain of 15.8 ± 0.1 dB throughout the 2.4 GHz industrial, scientific and medical (ISM) band and is unconditionally stable with $\mu \geq 4.9$. The PA has a compression point of $OP1dB = 20.03$ dBm and the signal has a non-linear phase shift of $\Delta\phi = 1.2^o$ up to this output power. A two-tone intermodulation test with 3dB back-off from OP1dB has a ratio of third-order intermodulation to fundamental of $IMD3 = 24.22$ dB, and lower and upper fifth order intermodulation to fundamental of $IMD5_{Lower} = 48.16$ dB and $IMD5_{Upper} = 49.8$ dB.

Finally the PA is shown to satisfy the requirements for operation within the institute of electrical and electronic engineers (IEEE) 802.11g standard. It achieves an average output power of

$15.4\ dBm$ while having an EVM of 5.43% or $-25.3\ dB$ while satisfying the output spectrum mask for all channels.

Keywords: RF CMOS. Linear Power Amplifiers. RF Power Amplifiers. Power Combiner. WLAN. Integrated transformers.

Um amplificador de potência RF CMOS linear com combinador de potência totalmente integrado

RESUMO

Este trabalho apresenta o projeto de um amplificador de potência (PA) de rádio-frequência (RF) linear em tecnologia complementar metal-oxido silício (CMOS). Nele são analisados os desafios encontrados no projeto de PAs CMOS assim como soluções encontradas no estado-da-arte. Um destes desafios apresentados pela tecnologia é a baixa tensão de alimentação e passivos com alta perda, o que limita a potência de saída e a eficiência possível de ser atingida com métodos tradicionais de projeto de PA e suas redes de transformação de impedância. Este problema é solucionado através do uso de redes de combinação de impedância integradas, como a usada neste trabalho chamada transformador combinador em série (SCT).

Os problemas com o uso de tecnologia CMOS se tornam ainda mais críticos para padrões de comunicação que requerem alta linearidade como os usados para redes sem-fio locais (WLAN) ou padrões de telefonia móvel 3G e 4G. Tais protocolos requerem que o PA opere em uma potência menor do que seu ponto de operação ótimo, degradando sua eficiência. Técnicas de linearização como pré-distorção digital são usadas para aumentar a potência média transmitida. Uma ténica analógica de compensação de distorção AM-PM através da linearização da capacitância de porta dos transistores é usada neste trabalho.

O processo de projeto é detalhado e evidencia as relações de compromisso em cada passo, particularmente o impacto da terminação de harmônicos e a qualidade dos passivos na rede de transformação de carga. O projeto do SCT é otimizado para sintonia da impedância de modo comum que é usada para terminar o segundo harmonico de tensão do amplificador. O amplificador projetado tem um único estágio devido a área do chip ser limitada a 1.57 x 1.57 mm^2, fato que impacta seu desempenho.

O PA foi analisado através de simulação numérica sob várias métricas. Ele atinge uma potência máxima de saída de 24.4 dBm com uma eficiência de dreno de 24.53% e Eficiência em adição de potência (PAE) de 22%. O PA possui uma curva de ganho plana em toda faixa ISM de 2.4 GHz, com magnitude de 15.8 $\pm$ $0.1dB$. O PA tem um ponto de compressão de $OP1dB = 20.03$ dBm e o sinal tem um defasamento não-linear de $\Delta\phi = 1.2^o$ até esta potência de saída. Um teste de intermodulação de dois tons com potência 3dB abaixo do OP1dB tem como resultado uma relação entre intermodulação de terceira ordem e fundamental de $IMD3 = 24.22$ dB, e de quinta ordem inferior e superior e fundamental de

$IMD5_{Inferior} = 48.16\ dB$ e $IMD5_{Superior} = 49.8\ dB$.
Por fim, mostra-se que o PA satisfaz os requerimentos para operar no padrão IEEE 802.11g. Ele atinge uma potência média de saída de $15.4\ dBm$ apresentando uma magnitude do vetor erro (EVM) de 5.43%, ou $-25.3\ dB$ e satisfazendo a máscara de saída para todos os canais.

Palavras-chave: RF CMOS, Amplificador linear, Amplificador de potência RF, Transformador integrado, WLAN, Combinador de potência.

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LIST OF ABBREVIATIONS AND ACRONYMS

AC	- Alternate Current
ADC	- Analog-to-Digital Converter
ADS	- Advanced Design System
CMOS	- Complementary Metal-Oxide Semiconductor
DAC	- Digital-to-Analog Converter
DAT	- Distributed Active Transformer
DC	- Direct Current
DSP	- Digital Signal Processor
EER	- Envelope Elimination and Restoration
EM	- Electromagnetic
ENIG	- Electroless Nickel Immersion Gold
EVM	- Error Vector Magnitude
FEC	- Forward Error Correction
FR4	- Fire Resistant class-4
GaAs	- Gallium Arsenide
GaN	- Gallium Nitride
GF	- Global Foundries
GME-AMS	- Grupo de Micro-Eletrônica - Analog e Mixed-Signal
GSG	- Ground-Signal-Ground
GSM	- Global System for Mobile communications
HASL	- Hot Air Solder Leveling
HEMT	- High Electron Mobility Transistor
IEEE	- Institute of Electrical and Electronic Engineers
IF	- Intermediary Frequency

IoT	- Internet-of-Things
ISM	- Industrial, Scientific and Medical
LNA	- Low Noise Amplifier
OFDM	- Orthogonal Frequency Division Multiplexing
PA	- Power Amplifier
PAE	- Power Added Efficiency
PCB	- Printed Circuit Board
PCT	- Parallel Combining Transformer
PER	- Power Enhancement Ratio
QAM	- Quadrature Amplitude Modulation
QFN	- Quad-Flat no leads
RF	- Radiofrequency
RMS	- Root-Mean Squared
SCT	- Series Combining Transformer
SMA	- SubMiniature version A
SMD	- Surface Mounted Device
SoC	- System-on-Chip
TSMC	- Taiwan Semiconductor Manufacturing Company
UFRGS	- Universidade Federal do Rio Grande do Sul
UFSC	- Universidade Federal de Santa Catarina
WCDMA	- Wideband Code-Division Multiple Acess
WLAN	- Wireless Local Area Network

CONTENTS

1 INTRODUCTION

Since its inception the mobile communications market has seen unprecedented growth, transforming everything from banking to the entertainment industry. The great driver of this growth is the continued improvement of radio electronics that is made ever more cheaper and with more data throughput. Digital communication standards are also another force behind this trend, allowing for optimized use of the electromagnetic spectrum and keeping the data rates growing while at the same time permitting a greater number of concurrent users.

In the 1990s, the 2G cellular standards era, a main source of this continued growth was the implementation of radio transceiver parts on CMOS technology and the continued integration of these parts on a smaller chip-set as the technology nodes advanced and made this possible. Continued integration and innovative radio topologies kept driving the prices down until the point where all the digital, analog and RF radio components but the power amplifier were integrated on a single chip. Integrating the PA chip with the transceiver at the time was not possible as the PA wasn't even available in CMOS technology.

This is because the power amplifier is by far the hardest radio transceiver block to integrate in CMOS. The PA function in the transmitter chain is to deliver the signal to the antenna with the necessary power for transmission while not distorting it above a certain threshold that is dependant on the communication standard used. Its design requires simultaneously low-loss passives and high-voltage devices and it is usually implemented in a high cost technology that is tailor-made for high-power RF applications such as Gallium-Arsenide (GaAs) or Gallium-Nitride (GaN). CMOS is cheap and has reached transition frequencies well beyond 100GHz (BENNETT et al., 2005) but it is optimized for digital circuits and presents high substrate losses as well as low supply voltage devices, limiting substantially the possible output power for classical PA topologies. Nevertheless CMOS is the only technology with enough integrability of digital and analog parts to even attempt at producing a single-chip radio (ZAMPARDI, 2010).

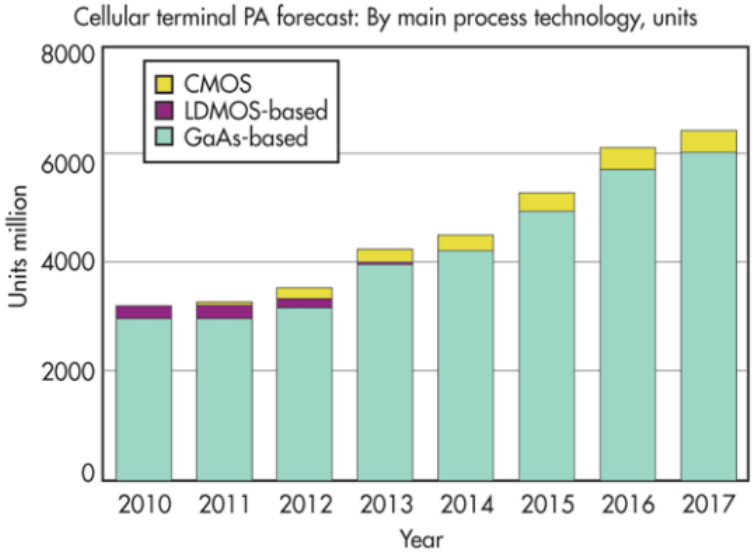
With all this in mind, a competitive CMOS PA was the goal of many researchers during that decade. This effort culminated on the first Watt-level RF power amplifiers fully integrated in CMOS that made their debut in 2001 academically (AOKI et al., 2002a) and 2002 commercially. It used a novel power-combining technique called distributed active transformer (DAT), and a switched amplifier class to achieve high output power with low voltage supply, but the latter was only possible because its application, the Global System for Mobile Communications (GSM) cellular standard, can cope with great amounts of distortion. At the end of the 2G era

these PAs achieved commercial success, but when newer standards arrived, which make use of techniques such as orthogonal frequency division multiplexing (OFDM) in order to increase spectral efficiency, the requirements for linearity were so high that the main mobile market came back to GaAs amplifiers. The CMOS PA lived on applications such as Bluetooth and WLAN eventually being able to become fully integrated with the rest of the radio in a system-on-chip (SoC) and is now the standard solution in these markets.

It was mainly through the innovations of start-up companies that CMOS PAs started making their way back in the 3G (WCDMA) market, companies such as Amalfi Semiconductor (now acquired by RFMD), Black Sand Technologies (TECHNOLOGIES, 2009) (acquired by Qualcomm), and Javelin Secomiconductor (WAGNER, 2012) (acquired by Avago) made 3G CMOS PAs off-the-shelf components.

The first 4G (LTE) CMOS PA was presented in 2013 (CARSON; BROWN, 2013) academically and in 2014 commercially(by Qualcomm). On the Watt-level power front the PAs are becoming increasingly complex and the combined use of digital techniques such as digital predistortion and cartesian feedback, as well as architectural innovations such as outphasing and polar modulation and RF techniques such as new power combiner layouts and harmonic tuning are what make CMOS competitive with other technologies in modern digital communication standards. This slow growth dynamics in the cellular market can be seen in figure 1.1.

Figure 1.1: PA cellular market growth up to 2014 and projection.

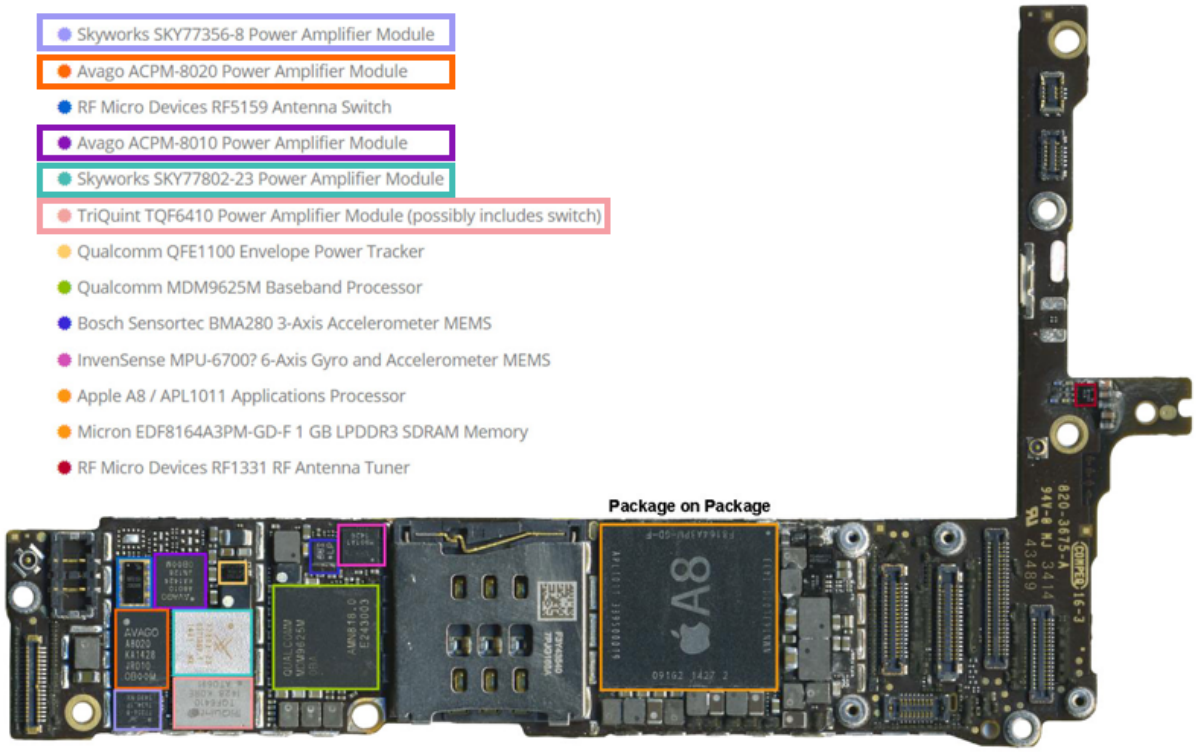


Source: (DELISLE, 2014).

The fact is that, due to the diversification of standards that a single device must communicate with, many of the chips in a mobile device phone are PAs. This can be seen in figure 1.2

which shows a single-side of a modern smartphone printed circuit board (PCB). This is contrary to the integrability trend and is a force driving up the prices of mobile devices. The solution is to provide cheaper individual PAs and try to integrate them as much as possible. The first solution is achieved with CMOS PAs and the second with wide-bandwidth PAs.

Figure 1.2: A view of an iPhone 6 printed circuit board (PCB).



Source: (TECHINSIGHTS, 2015).

Another market that CMOS radios and PAs are helping grow is the Internet of Things (IoT) market. On the front the focus is on very low power, high-efficiency and low-cost PAs and in this niche the CMOS PAs are paramount. Architectures such as RF digital-to-analog converters (RF DAC) and envelope modulation are very well possible to integrate with the rest of the transceiver at these power levels.

1.1 Objectives

It is because of these reasons and trends that CMOS PA research is still a hot topic in mobile whether in high-power or low-power applications. This work focus on the mid to high power architecture branch, and aims, given limitations such as access to technology and chip area to develop a fully integrated RF CMOS PA. The proposed amplifier should work in the 2.4 GHz ISM band and must be linear enough for a WLAN application. It should be fully integrated in standard CMOS, requiring no external matching components, which means the amplifier will have some sort of power combining. The design process is to be well documented as to make a guide for future projects. The specific target performance values are defined and justified in the chapter 3.

This work is one of the of initial works on power amplifiers by the GME-AMS/RF (Grupo de Microeletrônica - Analog and Mixed Signal / RadioFrequency) research group at Universidade Federal do Rio Grande do Sul (UFRGS), being the second master thesis on that topic from the group, and has as objective the development of know-how on RF Power Amplifiers design, simulation and measurement, creating the basis for the development future state-of-the-art amplifiers.

1.2 Organization

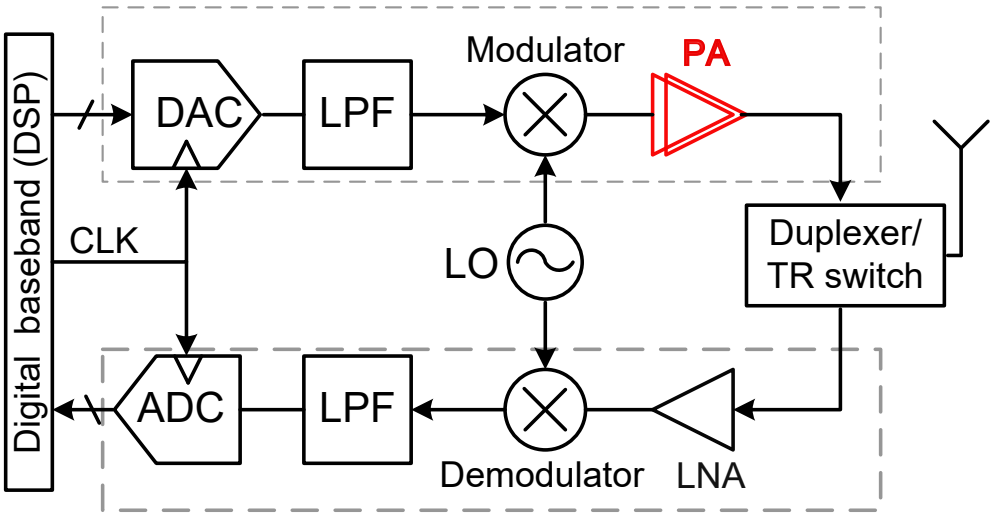
This thesis is divided as follows: The chapter 2 presents a review of the theory of RF Power amplifiers, with the focus on CMOS amplifiers, and a review of the current state of the art of these PAs. On chapter 3 the design process of the PA is presented, from the definition of specifications based on tapeout restrictions going through choice of topology, floorplan and the design of the active and passives parts of the PA. Chapter 4 focuses on the test bring-up structure, the PCB design and wire-bonding for chip-on-board for RF measurements. Chapter 5 presents the PA performance results. Finally chapter 6 concludes the document, reviewing the progress made through this work and highlighting the main lessons learned, followed by proposals of future works on the power amplifier field of study.

2 RF POWER AMPLIFIERS REVIEW

A typical transceiver block diagram is shown in figure 2.1. It is composed by a digital signal processor (DSP), a transmitter and a receiver. When in receiver mode, the signal flows through the duplexer to the receiver chain, getting amplified by the low-noise amplifier (LNA), then translated in frequency to an intermediary frequency (IF) or base-band in the demodulator and converted to the digital domain in the analog-to-digital converter (ADC) for further processing in the digital domain. In the transmit mode the signal originates on the digital domain, it is converted to the analog domain in a digital-to-analog converter (DAC) and upconverted to the transmit frequency in the modulator, then the PA amplifies the signal to the necessary output power for the transmission and its output is connected to the antenna through the duplexer.

Due to the fact that the PA has to deliver a high-power signal, its power consumption usually has the biggest impact on the consumption of the whole transceiver. That is the reason why the efficiency of the power amplifier is one of its most prioritized characteristics as it tends to dominate the efficiency of the system and be a direct limiter on battery life for mobile applications. To illustrate this, suppose that the PA has to deliver a $500\ mW$ average output power signal to the duplexer and has a 20% efficiency. That means that the PA has a power consumption of about $2.5\ W$. If the same PA had a 50% efficiency it would consume $1W$. The $1.5\ W$ saved in this case is very probably more than the rest of the transceiver combined. Also, this difference can mean whether the PA can be integrated with the rest of the transceiver due to the smaller heat dissipation that reduces thermal reliability issues on the chip.

Figure 2.1: Typical transceiver block diagram.



Source: (ALAVI, 2014).

2.1 Power amplifier figures of merit

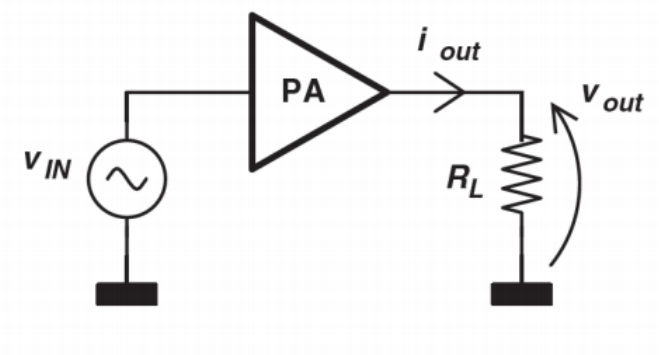
This section defines various measures that can be used to ascertain the performance of a power amplifier.

2.1.1 Output power

This is arguably the most important measure of a power amplifier, it is the active power delivered to the load. In RF and microwave design there is usually a characteristic system impedance, used in line, filters, antennas and other interfaces. The most common value for this impedance is $50\ \Omega$. The instantaneous output power is defined as the product of the output voltage V_{out} and current I_{out} through the load as seen in figure 2.2, such as:

$$p_{out}(t) = v_{out}(t)\ i_{out}(t) \tag{2.1}$$

Figure 2.2: Output current and voltage.



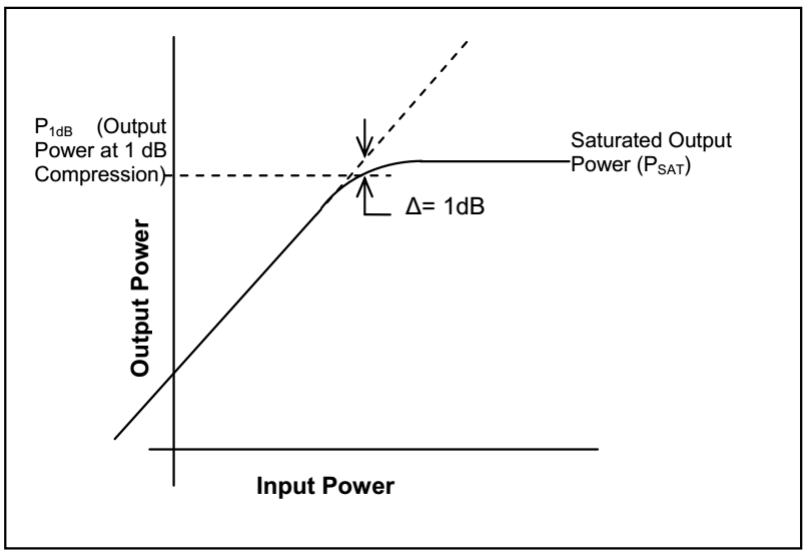
Source: (REYNAERT; STEYAERT, 2006).

Assuming a purely real linear load, the power delivered to a load R_L is given by:

$$p_o = \frac{V_{o,rms}^2}{R_L} \tag{2.2}$$

Where $V_{o,rms}$ is the root mean square (RMS) voltage over the load. The power over the fundamental and harmonic frequencies are both jointly calculated in this equation. As only the

Figure 2.3: Amplifier output power characteristics.



Source: (MINICIRCUITS, 2015).

power in the fundamental frequency should be irradiated, the harmonic frequencies should be filtered out. The power delivered only in a single tone signal is given by 2.3.

$$p_o = \frac{V_o^2}{2R_L} \tag{2.3}$$

where V_o is the peak output voltage in the frequency of interest.

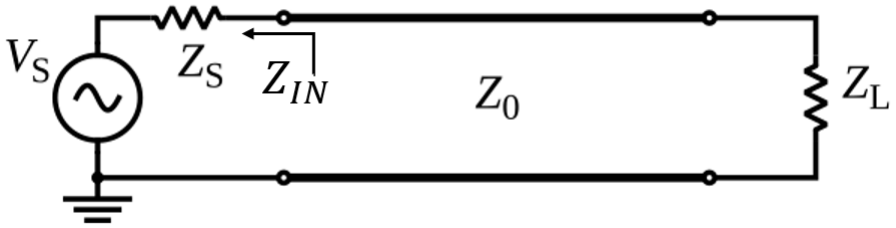
In figure 2.3 it is presented a P_{out} x P_{in} saturation characteristics of a power amplifier. Through this graph it is possible to explain some output power measurements. The absolute maximum power that an amplifier can deliver to a load is defined as the saturated output power, commonly denoted as P_{Sat}. The amplifier rarely operates close to that value due to linearity requirements that will be discussed in depth in 2.1.4, although the exact value of it's operating output power is highly dependant on the type of signal that is amplified, that is, the communication standard, this quantity is called average output power and is denominated P_{avg}. The power back-off P_{bkf} is defined as the ratio between the saturated output power and average output power.

2.1.2 Impedance matching and power gain

The PAs interfaces with off-chip transmission lines both at the output and input must be well designed in order to guarantee the circuit performance and robustness. For this it is necessary to understand how an impedance interface works in microwave circuit design. In figure 2.4 it is presented a diagram of such interface, the signal source has internal impedance Z_S, the transmission line has a characteristic impedance Z_0, the load is an impedance of Z_L, and Z_{IN} is the impedance seen by the signal source. When a microwave signal encounter an impedance interface it is separated into a transmitted wave and reflected wave. The condition for all of the power to be contained in the transmitted wave is that the impedances are complex conjugates of one another, this is called maximum power impedance matching, or, more often, simply impedance matching, illustrated in our example in equation 2.4.

$$Z_{IN} = Z_S^* \tag{2.4}$$

Figure 2.4: Signal delivered to load through a transmission line.



Source: (WIKIPEDIA, 2017).

The quality of the matching is expressed by a quantity called "return loss", defined by the ratio of the reflected power and the incident power. For a purely real source impedance $Z_S = R_S$, the return loss is given by 2.5.

$$\Gamma = \left| \frac{Z_{in} - R_S}{Z_{in} + R_S} \right|^2 \tag{2.5}$$

A mismatch in both sides of a transmission line create a standing wave that has a higher peak voltage value than if the impedances were matched. This effect is quantified in the value called Voltage Standing Wave Ratio (VSWR) and is important in PA design because mismatches on the PA output and input create these standing waves and they can stress the circuit until

breakdown or other harmful effects. A way to calculate this ratio using the insertion loss is given in 2.6.

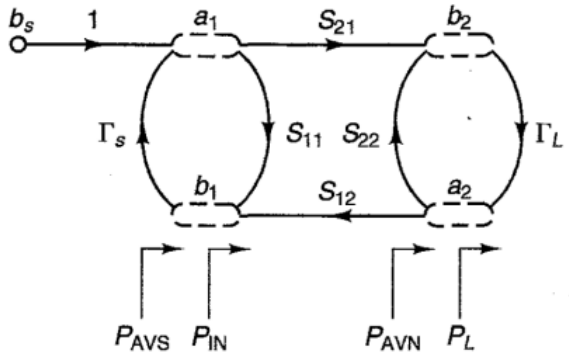
$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{2.6}$$

Impedance matching is not only important because of VSWR reasons. A PA expect an specific load impedance at its output, usually $50\ \Omega$. If this impedance deviates from this expected value, the amplifier's performances such as the output power, efficiency and linearity degrades and the PA might not meet the required protocol standards.

At the input the matching is important because the amplifier is driven by the output of another amplifier and a mismatch degrades the performance of the latter.

Another important fact regarding matching is the definition of power gain. Although many semiconductor devices such as MOS transistors presents a near open circuit at its input in lower frequencies. At high frequencies it is necessary power to drive these transistors. The input impedance is modelled as a resistor in series with the C_{gs} capacitor, this resistor is due to the physical resistance of the gate and bulk conductors which have RF current flowing in them to form the channel (NIKNEJAD, 2014). This gives rise to one of the main performance factors of a power amplifier which is the power gain. The power gain is the ratio of the power delivered to the load and the power dissipated at the input of the amplifier. There are many ways to define this gain formally (GONZALEZ, 1996). One of these ways is through the use of linear two-port network analysis and S-parameters as shown in figure 2.5, they are defined using power incident waves on port 1 and 2, a_1 and a_2 and power reflected waves, b_1 and b_2 respectively, in equations 2.7 to 2.10.

Figure 2.5: Two-port network power waves diagram.



Source: (GONZALEZ, 1996).

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \tag{2.7}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{2.8}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{2.9}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2.10}$$

figure 2.5 also defines the power in the input port (P_{IN}) calculated by equation 2.11 and the power delivered to the load (P_L) calculated by equation 2.12.

$$P_{IN} = \frac{1}{2}|a_1|^2 - \frac{1}{2}|b_1|^2 \tag{2.11}$$

$$P_L = \frac{1}{2}|b_2|^2 - \frac{1}{2}|a_2|^2 \tag{2.12}$$

With these in mind we formally define power gain, also know as operating power gain, as:

$$G_P = \frac{P_L}{P_{in}} \tag{2.13}$$

The theoretical maximum value for this quantity is achieved when both input and output are perfectly matched. This is called the maximum available gain or G_{Max} and is defined as the power gain when $\Gamma_s = 0$ and $\Gamma_L = 0$. In a passive network such as a transformer, the inverse of G_{Max} is used to quantify the minimum theoretical insertion loss of this network, which is the loss when both ports are presented with ideal impedances.

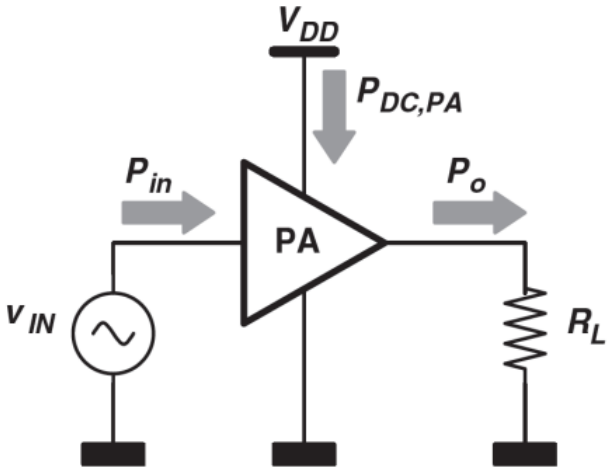
2.1.3 Efficiency

The are many ways to define the efficiency of an amplifier, they are all measures to convey the capacity of the PA of efficiently turning consumed DC (Direct Current) power ($P_{DC,PA}$) into RF output power at the frequency of interest (P_O), as is illustrated in figure 2.6. The most intuitive way to define a PA efficiency is the so called drain efficiency (η_D) which is defined in

equation 2.14 as the ratio of output power to the consumed DC power.

$$\eta_D = \frac{P_O}{P_{DC,PA}} \tag{2.14}$$

Figure 2.6: PA Power diagram.



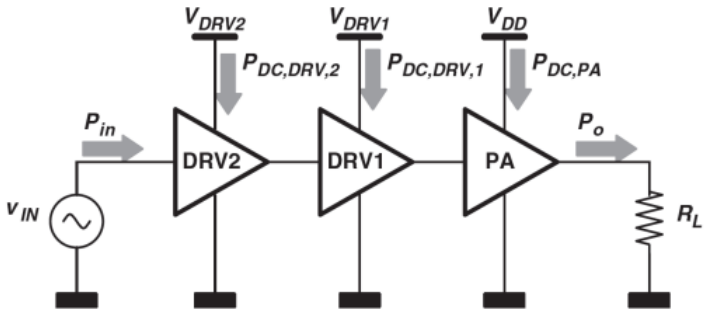
Source: (REYNAERT; STEYAERT, 2006).

The drain efficiency, although simple to be calculated and measured, lacks to include the input RF power necessary to drive the amplifier. To create a more useful efficiency measure for the system designer it is necessary to investigate how this input RF power is generated. This can be thought of as being done through cascading amplifiers that increases the signal power from a small value, insignificant in the system efficiency point of view, all the way to the RF output power. This can be seen in figure 2.7 which shows a chain of three amplifiers, usually denominated one output stage (PA) and two preceding drivers (DVR1 and DVR2). The efficiency of this amplifier chain can be calculated as seen in equation 2.15.

$$\eta_{chain} = \frac{P_O}{P_{DC,PA} + \sum_{i=1}^{n-1} P_{DC,DVRi}} \tag{2.15}$$

The number of drivers necessary in the chain depends on the power gain of the amplifiers, so it is natural that a measure of efficiency of a single individual amplifier that is relevant to the system designer also has to take into account the power gain of the amplifier. The most usual efficiency definition that also depends on the gain is the power added efficiency (PAE) and is defined in the following manner: Assume that all of the amplifiers have the same gain and drain efficiency, when the chain is long enough the whole system efficiency is going to

Figure 2.7: Cascading PAs power diagram.



Source: (REYNAERT; STEYAERT, 2006).

converge to the power added efficiency of a single amplifier, this happens because amplifiers at the beginning of the chain have an increasingly small contribution to the overall dissipated power of the system. The PAE can be obtained from equation 2.15 by making n go to infinity and $P_{DC,DRVi}$ be equal to $P_{DC,PA}$ divided by i gains. The resulting definition can be seen in equation 2.16.

$$\eta_{PAE} = \lim_{n\to\infty} \frac{P_O}{P_{DC,PA} + \sum_{i=1}^{n-1} P_{DC,PA}/G_{P,PA}^{i}} \tag{2.16}$$

The infinite series converges when the gain is higher than 1 and the equation becomes 2.17, which is a well known expression for the PAE as a function of the gain.

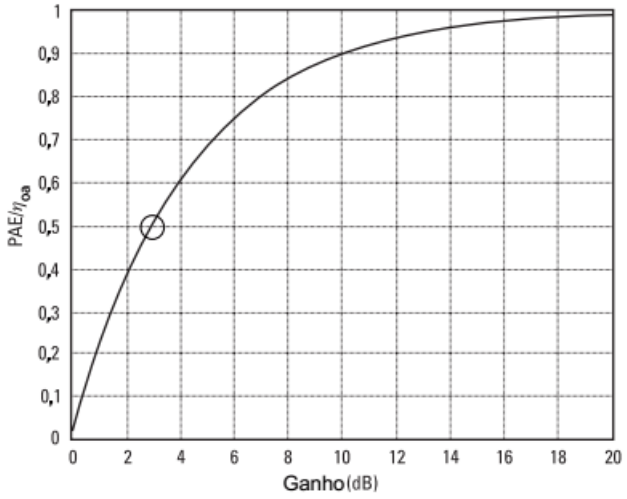
$$\eta_{PAE} = \frac{P_O}{P_{DC,PA}} \frac{G-1}{G} \tag{2.17}$$

A very common expression for the PAE is given in eq 2.18, although the previous method really shows why the PAE is important as a system measure, while this expression is usually shown without further explanation, it is easy to obtain this equation from equation 2.17.

$$\eta_{PAE} = \frac{P_O - P_{in}}{P_{DC,PA}} \tag{2.18}$$

Finally, we can see from equation 2.17 that when the gain is high, the PAE is close to the drain efficiency. The relationship is illustrated in 2.8 where one can see the importance of power amplifier gain in the overall system performance.

Figure 2.8: relationship between PAE, drain efficiency and gain.



Source: (ROGERS; PLETT, 2010).

2.1.4 Linearity

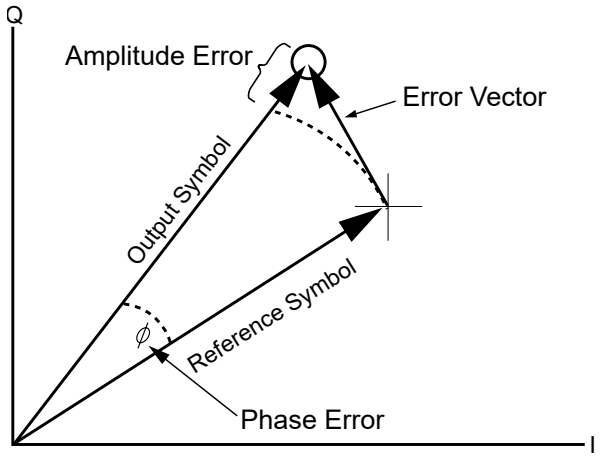
Another issue relevant to PAs is that it is necessary to amplify the signal power without corrupting the signal content so that it can still be decoded at reception. Two issues can degrade signal performance: noise and nonlinear distortion. The former is not a big issue for PAs because the signal levels are large at transmission and so the contributed noise is not significant, that is, after reception, the receiver noise will dominate the noise contribution on the link. The latter is the big problem of signal corruption on PAs. The signals that the PA must deal with are large and the circuit itself usually goes into deep non-linear transistor regions such as cut-off and, for MOSFETS, triode regions to improve the PA efficiency, as will be seen in section 2.2.

There are many types of non-linear distortion and full dynamical analysis is very often impractical. A common technique in small-signal circuits is to ignore dynamical effects and model the whole circuit non-linearity as a static system. This method might be practical in a low-noise amplifier where the signal and distortion is comparatively small but it will yield large prediction errors when applied to a PA. A more common approach is the quasi-static, in this approach the non-linear behavior is divided in AM-AM non-linearity and AM-PM non-linearity. AM-AM non-linearity is defined as when the amplifier gain depends on the input signal amplitude and arises from gain expansion or compression. This behavior comes naturally from transistor transconductance linearity that suffers from issues such as exponential behavior or saturation. AM-PM non-linearity is defined as when the output signal phase shift depends on the input signal amplitude and usually comes from a transistor input capacitance non-linear

characteristic. The AM-PM non-linearity effect is a great contributor of distortion in MOS amplifiers, such as amplifiers in CMOS or GaAs p-High Electron Mobility Transistor (pHEMT) technologies, that would not be predicted in a static model.

The impact of the amplifier non-linearity on the signal causes two problems: signal information corruption and out-of-band emissions. To understand the impact of signal distortion it is necessary to understand how information is encoded in the signal, that is: The modulation scheme and how AM-AM and AM-PM non-linear behavior affects differently each modulation schemes (RAZAVI, 2011). Communication standards will have their own linearity requirements based off on the amount of signal distortion that can be tolerated. Signals that have very little variable envelope such as GSM and Bluetooth are very robust against AM-AM non-linearity while signals with variable envelope, quantified in a high peak-to-average ratio, such as WLAN and LTE are severely corrupted by amplitude distortion, because they use OFDM and quadrature-amplitude modulation (QAM) to increase spectral efficiency. This leads to different types of PAs being used in different applications, such as switched PAs that have high efficiency but high AM-AM distortion being widely used in GSM but not being able to be used in WLAN or LTE, such issue will be discussed in more detail in section 2.2.

Figure 2.9: EVM definition.



Source: (SANTANA, 2016).

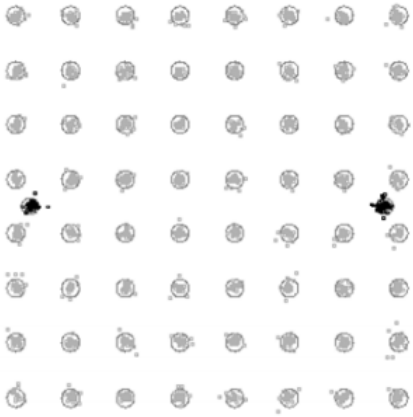
$$EVM_{RMS} = \frac{\sum_{i=0}^{N} \frac{1}{N}(IQ_{ideal(i)} - IQ_{real(i)})^2}{\sum_{i=0}^{N} \frac{1}{N}(IQ_{real(i)})^2} \tag{2.19}$$

To measure and certify the PA linearity performance under a certain standard it is necessary take into account the full dynamical behavior, either through numerical simulations or

physical measurements of the PA output signal while the circuit is fed with a sample of the standard input signal. The input signal consists of a digital communication standard series of symbols encoded on the amplitude and phases of one or multiple carriers. To measure the output signal distortion it is used the error vector magnitude. While to measure out-of-band emissions a spectrum measurement is compared to a compliance spectrum mask and integrated power on the adjacent and alternate channels is measured (ACPR, adjacent channel power ratio) and compared to the standard specifications.

The EVM is defined as the root mean square (RMS) of the error between the output and reference symbols, the method is illustrated in figure 2.9 and is mathematically expressed in 2.19, where IQ_{ideal} is the i-th reference symbol and $IQ_{real(i)}$ is the i-th output symbol. This is calculated for a large number of symbols to reduce statistical uncertainty and can be expressed in $\%$ or dB. A constellation test of a PA under 802.11g 54Mbps 64QAM signal is exemplified in figure 2.10.

Figure 2.10: 64QAM signal constelation.

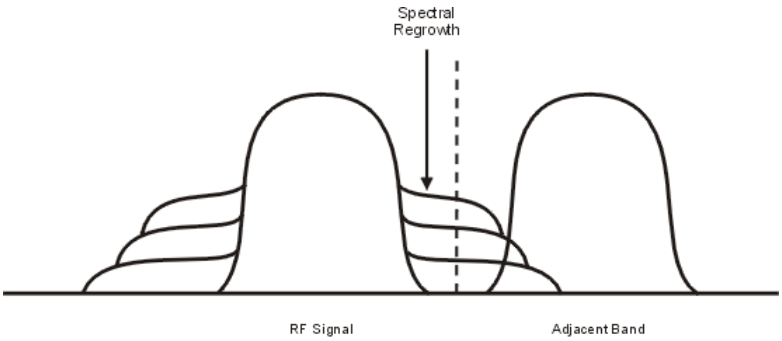


Source: (KANG; HAJIMIRI; KIM, 2006).

The effect of spectral regrowth is the cause for near frequency out-of-band emissions. This effect makes the transmitted signal have sidebands that can interfere in the adjacent channel as can be seen in 2.11, in order to control this interference the standard can provide two tests that the PA must comply. ACPR defines how much integrated power can be transmitted in the adjacent channel and is defined as the power ratio of the power transmitted in the adjacent channel and the power transmitted in the main channel as shown in equation 2.20.

$$ACPR = \frac{P_{adj}}{P_{main}} \tag{2.20}$$

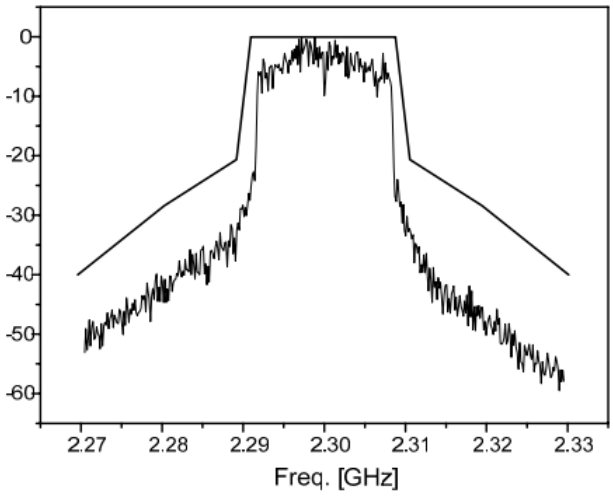
Figure 2.11: spectral regrowth illustration



Source: (KEYSIGHT, 2017).

Finally there is a spectrum mask that the transmitted spectrum must comply, this mask defines the maximum output power density in regions both near and far to the transmitted channel. A 802.11g output spectrum mask is shown in figure 2.12.

Figure 2.12: 802.11g spectrum mask.



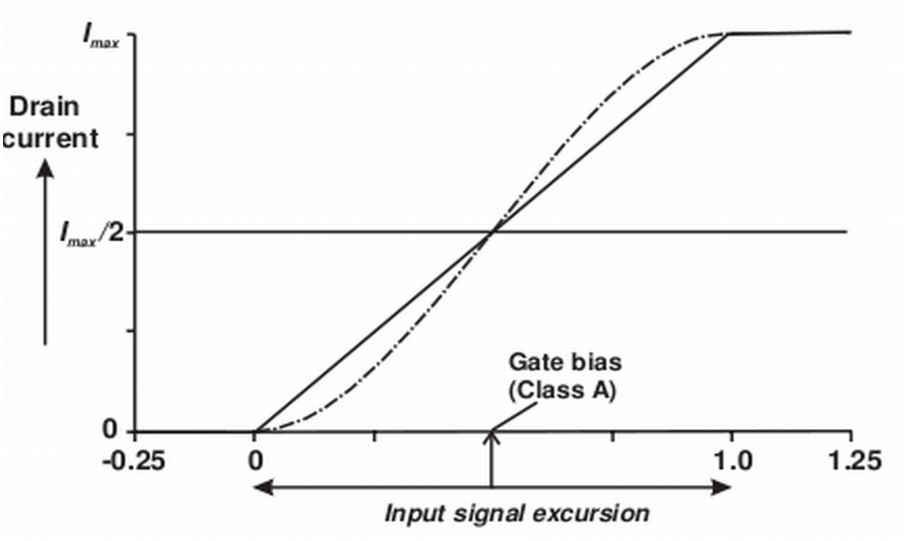
Source: (KANG; HAJIMIRI; KIM, 2006).

2.2 Power Amplifier linear operating classes

Power amplifiers are implemented with active devices such as MOS transistors that have an output current controlled by an input voltage. These devices, when viewed under large-signal variations are heavily non-linear, presenting very distinct operating modes such as cutoff, "linear amplification" (called saturation region in a MOS transistor) and triode. To manage these large

non-linearities the device must be properly biased with quiescent voltages at both the output and input. When a single transistor is presented with a output DC bias, its simplified normalized output current versus normalized input voltage is as presented in figure 2.13.

Figure 2.13: Transistor large-signal simplified models.



Source: (CRIPPS, 2006).

In this figure the dashed line represents a 3rd order polynomial approximation of the transistor behavior, while the solid line represents the so called piecewise transistor model, this model separates the transistor behavior in the cutoff region for a normalized input gate-source voltage bellow zero, the conduction region for an input signal between zero and one and triode (generally called output current saturation) for an input signal higher than one. Although greatly simplified, the whole of the classical analytic theory of PA operation is based off on this model. Throughout this section we will mathematically analyze PA classes using the piecewise model, while pointing out some effects that are not present in this model and are known through numerical simulations and experimentation.

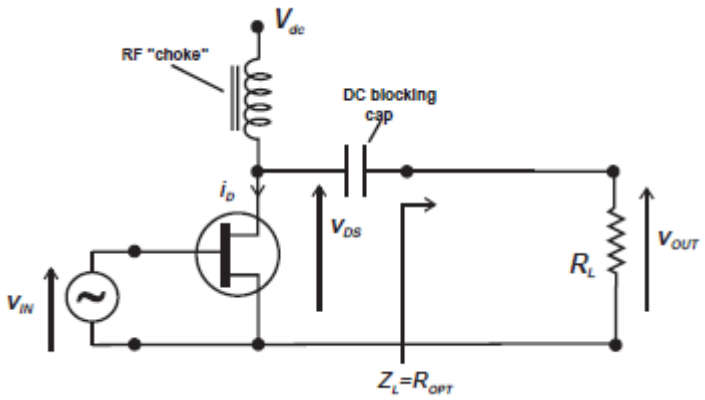
This model is only useful for the PAs classes that operate at least part of the its conduction cycle within the linear part. There also exists switching PAs, these operate with the active device always deep into a non-linear region and can be understood in an entirely different manner and using mathematical models that won't be presented in this work. That is because switching PAs suffer heavily from AM-AM non-linear distortion and can't be used in a modern communication standard without some complex linearizing technique that prevent the solution of being integrated into a single chip. Until 2013 the only single-chip watt-level linear PAs presented were of the classical PA classes (JOHANSSON; FRITZIN, 2014), although

there is substantial research to try and integrate polar modulated PAs or Envelope Elimination and Restoration (EER) PAs in a single CMOS chip.

2.2.1 Class A PA

A Class A PA is an amplifier where the active device is always operating on the linear region of its curve as defined earlier. That is, if the input signal is a sinusoid and not exceed the boundaries of this region, then the output signal has no harmonic distortion. An example of optimal class-A bias point can be seen in figure 2.13.

Figure 2.14: Transistor biased for RF amplification.



Source: (CRIPPS, 2006).

Figure 2.14 shows a single transistor biased for use as a Class-A RF Power amplifier. We must determine R_{opt} for maximum output power and efficiency. For this condition to be met V_{DS} must swing between $2V_{DC}$ and nearly zero as shown in the waveforms in figure 2.15. This means R_{opt} is defined as in equation 2.21 and the efficiency of the amplifier in this condition is given by equation 2.23. The output power in this condition is given by 2.24 The remaining 50% of supplied power is dissipated in the transistor.

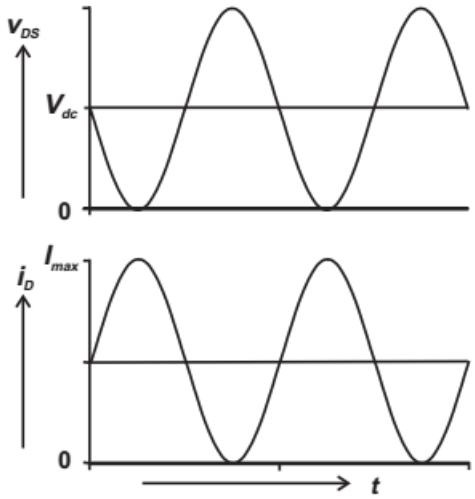
$$R_{opt} = V_{DC}/(I_{max}/2) \tag{2.21}$$

$$\eta = \frac{V_{DC}^2/(2R_{opt})}{V_{DC}^2/R_{opt}} \tag{2.22}$$

$$= 50\% \tag{2.23}$$

$$P_{out} = V_{DC}^2/(2R_{opt}) \tag{2.24}$$

Figure 2.15: Class-A amplifier waveforms.



Source: (CRIPPS, 2006).

In order to present the optimal impedance at the output of the amplifier, it is necessary to transform the usual $50\ \Omega$ impedance of antennas and transmission lines to this impedance, for this it is necessary to use a impedance transforming network, also called matching network. The impedance presented at the output of the power amplifier does not need to be equal to the output impedance of the amplifier. In fact the optimal impedance found by 2.21 is called load-line match and can be used even in other more non-linear classes of amplifiers. In fact the output impedance of the device very hard to define when the amplifier goes into cutoff for part of the cycle as it is time-varying (CRIPPS, 2006). The impedance transformation network characteristics are fundamental to the PA performance and design constraints, and are going to be detailed in 2.3.

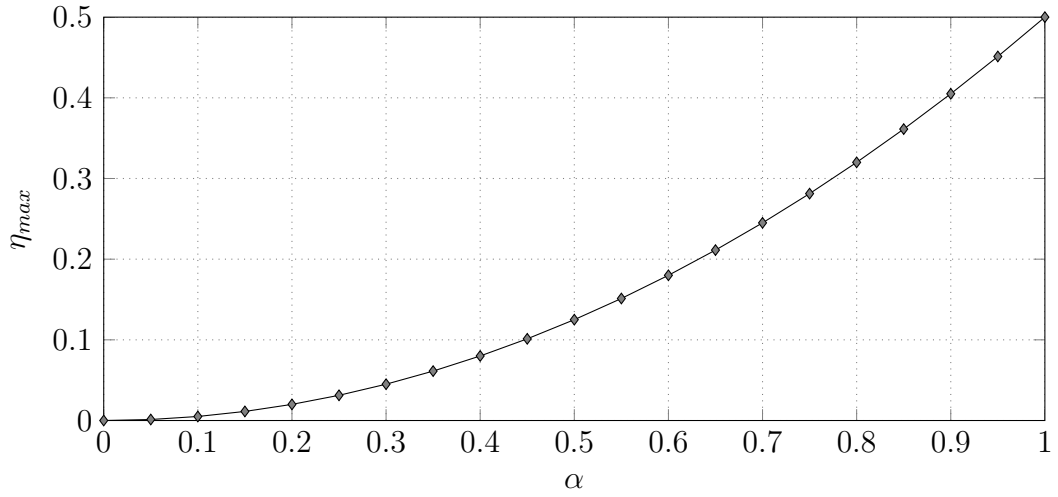
A modulated signal that presents high peak-to-average ratio will be severely distorted if it is not presented at input with a average power level backed-off from the maximum input swing. This makes important to understand how the amplifier efficiency changes when a input

voltage signal does not make the output rail-to-rail. This behavior is presented in the equation 2.26 where V_P is the peak output voltage and $\alpha = V_P/V_{DC}$. A graph detailing the back-off efficiency behavior can be seen in 2.16.

$$\eta = \frac{V_P^2/(2R_{opt})}{V_{DC}^2/R_{opt}} \tag{2.25}$$

$$= 0.5\alpha^2 \tag{2.26}$$

Figure 2.16: Class-A back-off efficiency.



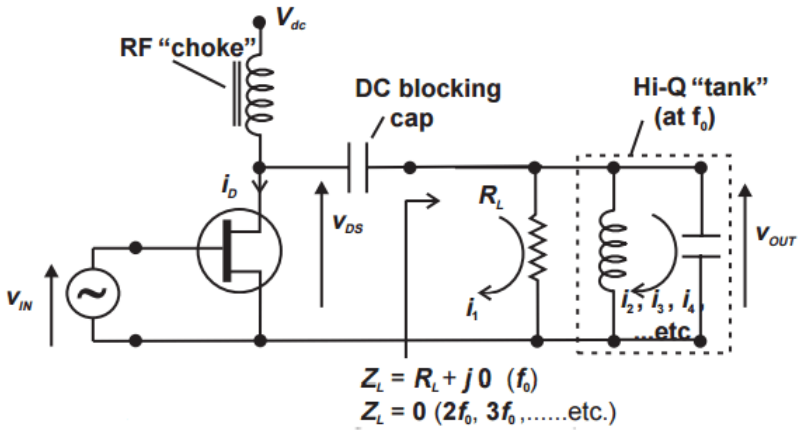
Source: The author.

Further aggravating this problem, transistors require a minimum drain/collector voltage to operate linearly requiring even more back-off to not get into the triode region (called saturation in bipolar transistors), this voltage is called knee voltage. This problem is worse in MOSFETs than bipolar transistors, and tends to get worse as technology nodes progress because the knee voltage becomes a higher percentage of the supply voltage as these latter voltages decreases and also depends on the input signal amplitude (hence, the amplifier gain). To illustrate, a typical $130nm$ node has a supply of $1.2\ V$, suppose an output voltage of $V_P = 800\ mV$ is the maximum to keep the MOSFET transistor saturated (that is, in the linear region for MOSFETS), then the amplifier maximum efficiency in this condition is 22.2% if there is no further loss on the matching network. In reality there is no discrete barrier between the linear and triode regions and the transistor gets more nonlinear as the signal increases, so this effect further increases the linearity-efficiency trade-off that plagues PA design.

2.2.2 Class AB, B and C PA

In order to improve the efficiency of the amplifier, one must consider using the non-linear regions of operation of the transistor. Amplifiers that have a sinusoidal input signal and that makes the transistor go into cut-off for part of the signal cycle are called reduced conduction angle amplifier modes. These are divided in AB, B, or C amplifier classes depending on what percentage of the signal cycle the transistors are in cut-off. To operate in these amplifiers classes it is not enough only to bias the transistor near or into the cut-off region. It is necessary a higher input signal amplitude to drive the amplifier into the edge of saturation and take full advantage of the capacity for improved efficiency. There's also a necessity for terminating harmonic frequencies with shorts at the load, as this maintains the output signal voltage sinusoidal even with high harmonic content on the current. This is easier to do in discrete systems with transmission line terminations and is rarely satisfactorily achieved in monolithic amplifiers. The following analysis assumes that these terminating conditions are ideal for simplification and is still reasonably valid, specially for a first design iteration. A more detailed analysis of the impact of non-ideal terminations can be found in (CRIPPS, 2006). The circuit to be analysed is shown in figure 2.17.

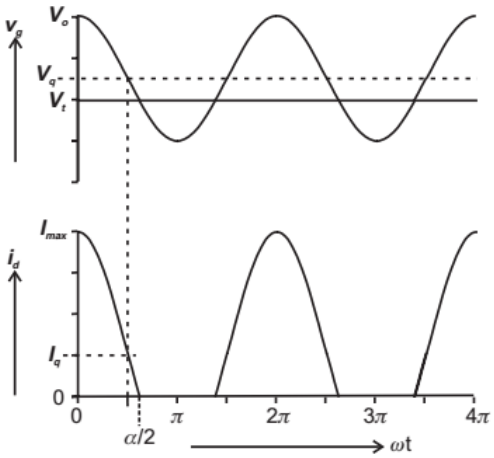
Figure 2.17: Reduced conduction angle single transistor amplifier.



Source: (CRIPPS, 2006).

A class AB amplifier is one that has reduced conduction angle and is biased above the cut-off point of the transistor, that is, has a non-zero bias current. A class B amplifier is biased exactly at the cut-off point. A class-C amplifier is biased bellow the cut-off point and has a nearly zero bias current. Even bellow the threshold voltage the transistor current never actually

Figure 2.18: Class-AB amplifier waveforms.



Source: (CRIPPS, 2006).

reaches zero as in the piecewise model. The resulting waveforms are shown in figure 2.18 for a class-AB amplifier, the waveforms for the classes B and C are similar but the current waveform is a sinewave truncated at higher levels. It is necessary to find the current waveform frequency components to determine the efficiency and output power capabilities of the amplifier. For this let us normalize values as $V_t = 0$ and $V_O = 1$, then the normalized input signal amplitude is defined as in 2.27 so that it changes and guarantees that the peak output current always reach I_{max}.

$$V_{IN} = 1 - V_q \tag{2.27}$$

$$i_d(\theta) = I_q + I_p cos(\theta),\ -\alpha/2 < \theta < \alpha/2 \tag{2.28}$$

$$= 0,\ -\pi < \theta < -\alpha/2\ ;\ \alpha/2 < \theta < \pi \tag{2.29}$$

The conduction angle is α and denotes the portion of the RF cycle that the device is conducting. The RF current can be written as in equation 2.29 where $I_p = I_{max} - I_q$ and $cos(\alpha/2) = -\frac{I_q}{I_p}$.

We then are able to rewrite the current expression inside the conduction region as 2.30 and proceed with the Fourier analysis. The DC current component can be calculated from 2.31 while fundamental and higher harmonics can be calculated from 2.32.

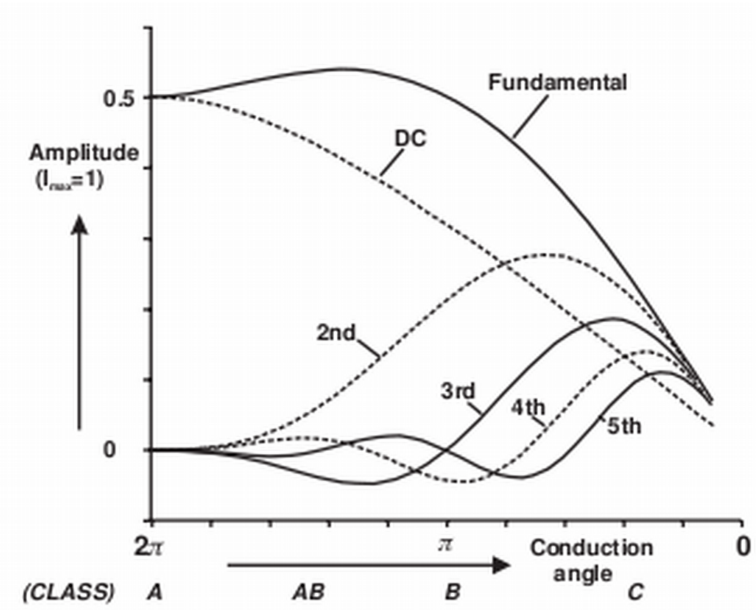
$$i_d(\theta) = \frac{I_{max}}{1 - cos(\alpha/2)}(cos\theta - cos(\alpha/2)) \tag{2.30}$$

$$I_{DC} = \frac{1}{2\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - cos(\alpha/2)} (cos\theta - cos(\alpha/2)).d\theta \tag{2.31}$$

$$I_n = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - cos(\alpha/2)} (cos\theta - cos(\alpha/2))cos(n\theta).d\theta \tag{2.32}$$

These magnitudes up to $n = 5$ are plotted in the graph 2.19. Taking into consideration that 3rd and 5th order distortion are the most harmful for both EVM and spectral regrowth (CRIPPS, 2006), in this graph it is possible to see a optimum bias point for the linearity behavior and RF output power for a power amplifier that is $\alpha = 240^o$. This point is approximate because of the piecewise model assumption but it is a well-known fact that there is a optimal bias point in the class-AB region for many devices, usually in moderate inversion for a MOS transistor, and most of the classical linear PAs designed are biased in class-AB to take advantage of this point.

Figure 2.19: Reduced conduction angle amplifier current harmonic content.

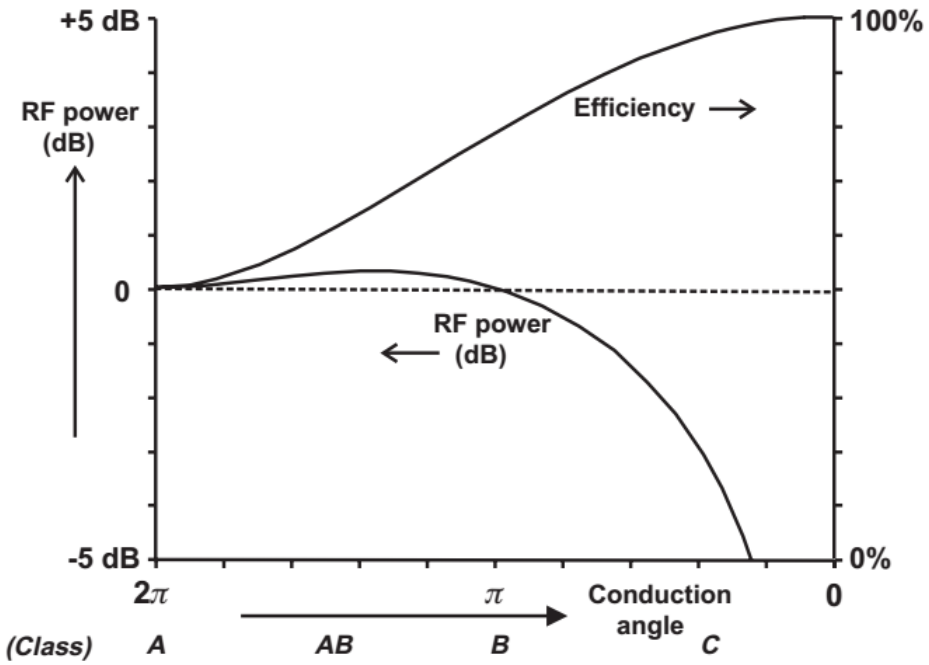


Source: (CRIPPS, 2006).

The output power advantage for class-AB can be seen in figure 2.20 as well as the efficiency over several bias points. Another interesting information is the high level of second-harmonic content throughout the whole class-AB, this means that the behavior shown in the figure can be heavily influenced by the impedance termination at this harmonic. The voltage

harmonics created by a non-zero 2nd harmonic impedance termination can severely degrade maximum output power, efficiency and specially linearity by driving the transistor early into triode. A more detailed analysis of the non-zero impedance termination on a class-AB amplifier can be found in (CRIPPS, 2006).

Figure 2.20: Reduced conduction amplifier normalized output power and efficiency.



Source: (CRIPPS, 2006).

2.3 Load impedance transformation

The major impairments for designing a power amplifier in sub-micrometer CMOS technologies are the low transistor breakdown voltage and the high loss of on-chip impedance transformers. Sub-micrometer transistors have breakdown voltages on the order of $4 - 6\ V$(AOKI et al., 2002a), and that value can go even lower for thin-oxide devices in recent technology nodes. In eq. (2.33) we can see that the power delivered to a $50\ \Omega$ load for a sinusoidal voltage waveform with maximum output swing is only 40-$90\ mW$, where P_{out} is the output power, V_{Swing} is the output voltage swing and R_{Load} is an arbitrary load resistance. To achieve higher output power a load impedance transformation must be done and this can be accomplished by

an on-chip transformer network or inductive-capacitive (LC) resonant matching network, both presenting high loss in standard CMOS due to the mid resistivity conductive substrate.

$$P_{out} = \frac{V_{Swing}^2}{2R_{Load}} \tag{2.33}$$

2.3.1 Resonant LC impedance transformation network

A single resonant LC impedance transformation network section is shown in figure 2.21. The dual version of this network can also be used but the version with the series capacitor has the advantage of providing DC decoupling and the use of a parallel inductor with one of the terminals connected to ground lessens its losses due to substrate coupling. The impedance transformation factor r is defined in equation 2.34 for the case of an ideal LC network, where R_{load} and R_{in} are the load and transformed impedance at port-1 and Q_l is the loaded quality factor as defined in 2.35, and L_p is the parallel inductor.

$$r = \frac{R_{load}}{R_{in}} = 1 + Q_l^2 \approx Q_l^2 \tag{2.34}$$

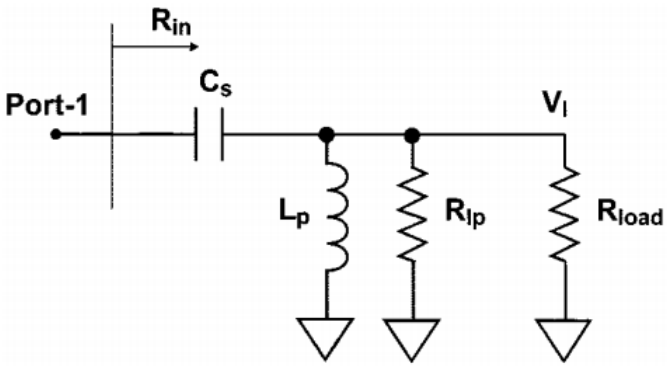
$$Q_l = \frac{R_{load}}{\omega L_p} \tag{2.35}$$

The value of the capacitance is such that it resonates with the inductor reactance and the impedance seem by the port-1 is purely real for class-AB PAs, other PAs topologies such as class-J uses non-zero load reactance. this capacitance can incorporate the drain capacitance of the transistor and its value is given by equation 2.36.

$$\frac{1}{\omega C_s} = \frac{\omega L_p}{1 + 1/Q_l^2} \approx \omega L_p \tag{2.36}$$

The efficiency of a LC-network with loss η is the ratio of the RF power delivered to the load and the input RF power and is derived in equations 2.37 - 2.42. The impedance transformation factor r is given by 2.41. It is also possible to calculate the efficiency of the section as a function of the inductor quality factor Q_{ind} and r as is shown in 2.42.

Figure 2.21: Resonant LC impedance transformation network with loss.



Source: (AOKI et al., 2002a).

$$\eta = \frac{P_{load}}{P_{in}} \tag{2.37}$$

$$= \frac{|V_{load}|^2/(2R_{load})}{|V_{load}|^2/(2(R_{load}||R_{lp}))} \tag{2.38}$$

$$= \frac{1/R_{load}}{1/R_{lp} + 1/R_{load}} \tag{2.39}$$

$$= \frac{1}{1 + R_{load}/\omega L_p Q_{ind}} \tag{2.40}$$

$$r = \frac{R_{load}}{(\frac{R_{load}||R_{lp}}{1+Q_{total}^2})} = \frac{(1 + \frac{R_{load}}{R_{lp}})^2 + Q_{ind}^2 \frac{R_{load}}{R_{lp}}}{1 + \frac{R_{load}}{R_{lp}}} \tag{2.41}$$

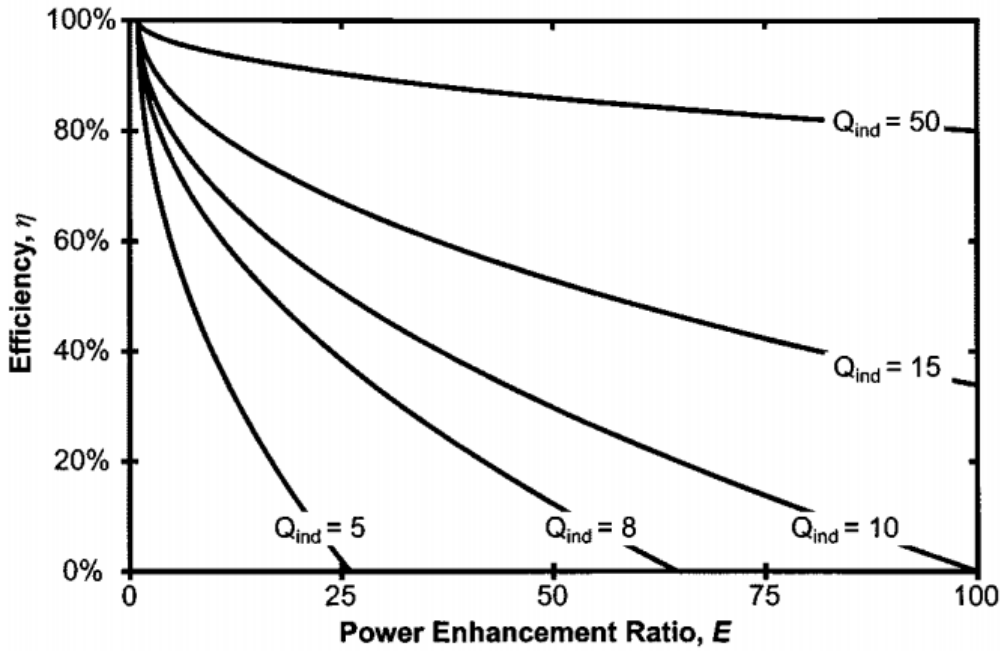
$$\eta = \frac{Q_{ind}^2 + 1}{Q_{ind}^2 + \frac{r + \sqrt{r^2 + 4Q_{ind}(r-1)}}{2}} \tag{2.42}$$

We can define a measure for any impedance transformation network called power enhancement ratio (PER) E as in 2.43. This measure is more useful than r as it takes into account the losses in the network and thus can act as a better predictor of the possible output power of a PA. In figure 2.22 the efficiency versus PER for a single LC-network is presented. The expression of the PER is in equation 2.44.

$$E = \frac{P_{network}}{P_{direct}} = \frac{P_{direct}.r.\eta}{P_{direct}} = r.\eta \tag{2.43}$$

$$\eta = 1 - \frac{\sqrt{E-1}}{Q_{ind}} \approx 1 - \frac{\sqrt{E}}{Q_{ind}} \tag{2.44}$$

Figure 2.22: LC η versus E.



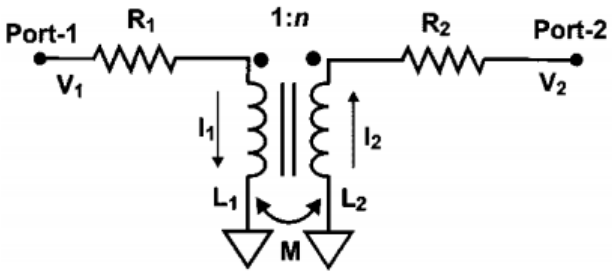
Source: (AOKI et al., 2002a).

It is evident from the graph that the use of LC networks poses a severe efficiency versus PER trade-off that makes it impractical for use in CMOS power amplifiers that have very low voltage supply and hence need a high PER to deliver a watt-level power to the load. For instance, for an output power of $1\ W$ for a $50\ \Omega$ load from a $2\ V$ power supply would require a PER on the order of 50 depending on the device knee voltage, this would mean a passive efficiency of 35% for a Q_{ind} of 10, which is a common value for CMOS integrated inductors. This means that another strategy must be used that is able to be integrated in MOS technology and provide a high impedance transformation ratio with a high efficiency, that is, a high PER.

2.3.2 Magnetic coupled transformer impedance transformation

Another straightforward way to transform an impedance value is through a magnetically coupled transformer. We can see a diagram of a $1 : n$ transformer in Figure 2.23, where the port-1 loss is modelled in R_1, port-2 loss in R_2, and the mutual inductance M is coupled with the coupling factor k. In equation 2.45 we can see how port currents can induce voltages in the

Figure 2.23: magnetically coupled transformer diagram.



Source: (AOKI et al., 2002a).

other port through M, which is defined in equation 2.46, we can also extract the approximate transformer turn ratio as seen in equation 2.47.

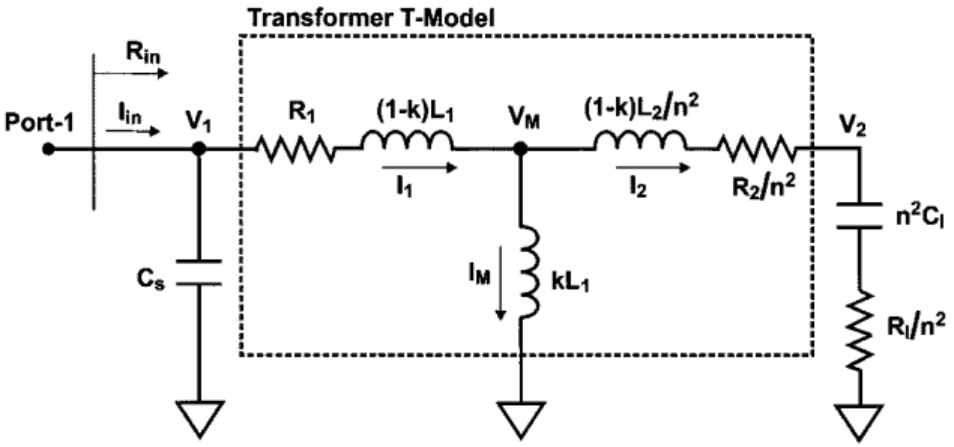
$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & -j\omega M \\ j\omega M & R_2 + j\omega L_2 \end{bmatrix} \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{2.45}$$

$$M = k\sqrt{L_1 L_2} \tag{2.46}$$

$$n = \sqrt{\frac{L_2}{L_1}} \approx \frac{I_1}{I_2} \approx \frac{V_2}{V_1} \tag{2.47}$$

In order to calculate the efficiency of the network we can define the quality factors of L_1 and L_2 with the respective resistances as $Q_{1,2} = \omega L_{1,2}/R_{1,2}$. In order to optimize the efficiency of these transformers it is necessary to put a capacitor on the output to resonate with the inductance at this port at the frequency of interest, this is because the output of the transformer is a signal source with a non-zero inductive impedance and the capacitance adapts the load impedance for it to present the complex conjugate of the source impedance. Also, to adjust the transformer input reactance for the driving amplifier, a capacitor is connected to its input. This is shown in figure 2.24 where the inductances have also been separated into the coupled part kL_1 seen by both ports and leakage inductances $(1-k)L_{1,2}$, this model is called T-model. This model can be used to calculate the optimal load capacitor C_l, the efficiency and the optimum inductances values. We assume $L_1 \approx L_2/n^2$. The optimum capacitor is given in 2.48. the efficiency is given by equation 2.50 and the optimum inductance is found by differentiating the previous equation and solving it for the minimum, and is given by 2.51. The admitance seen at the input of the amplifier is given by 2.52 (AOKI et al., 2002b).

Figure 2.24: Transformer T-model with tuning capacitors.



Source: (AOKI et al., 2002a).

$$C_l = \frac{1}{\omega L_2} \tag{2.48}$$

$$A = \frac{1}{\sqrt{\frac{1}{Q_2^2} + \frac{Q_1}{Q_2}k^2}} \tag{2.49}$$

$$\eta = \frac{R_l/n^2}{(\frac{\omega L_1/Q_2 + R_l/n^2}{\omega k L_1})^2 . \frac{\omega L_1}{Q_1} + \frac{\omega L_1}{Q_2} Rl/n^2} \tag{2.50}$$

$$\omega L_1 = \frac{A.R_l}{n^2} \tag{2.51}$$

$$Y_{in} \approx \frac{1}{1+A^2} \frac{Q_1}{\frac{Q_1}{k^2+Q_2}} (\frac{n^2}{R_l} + j\frac{1}{\omega L_1}) \tag{2.52}$$

The series resonant capacitor C_l can be substituted by a load parallel resonant capacitor C_{out}, this has the advantage of reducing the value of the optimal inductances, the new optimal inductance and output capacitance values can be seen in equations 2.53 and 2.54. With this optimum L_1' the maximum efficiency is given by 2.55. It is important to note that this value is independent of the impedance transformation ratio insofar as values such as K and $R_{1,2}$ are as well, which they are not. But this means that the magnetically coupled transformer has a much weaker trade-off between efficiency and PER than the LC transformation network. This can be seen in figure 2.25 which shows the transformer efficiency for many values of inductance and quality factors. The limitation comes from the layout, it is hard to make a high turn-ratio transformer to provide a high PER because it is hard to make a layout which a many turns spiral

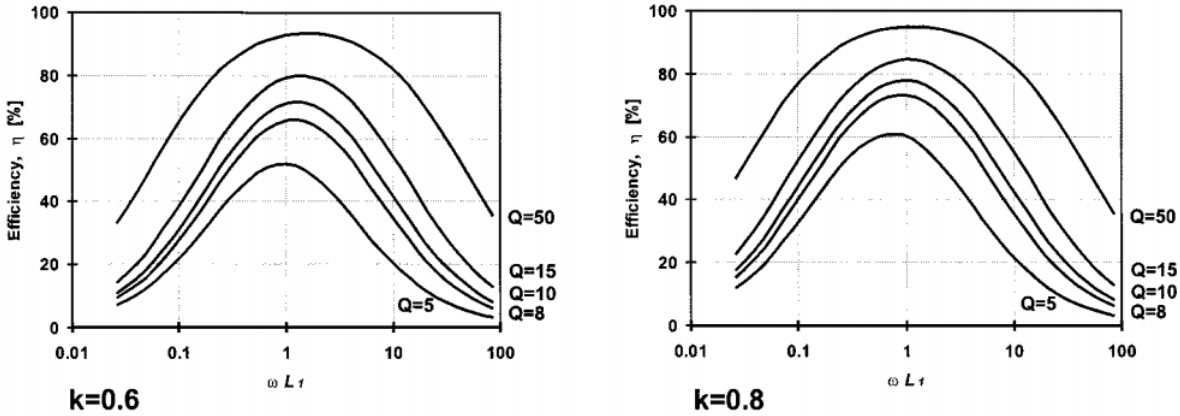
has a high-coupling factor with a few turns spiral. This means that while it is possible to make low insertion loss $1:1$ or even $1:2$ transformers but that their loss is still unpractical for high impedance transformation ratios.

$$\omega L_1' = \frac{A.R_l}{n^2(1+A^2)} \tag{2.53}$$

$$\frac{1}{\omega C_{out}} = \frac{A.R_l}{(1+A^2)} \tag{2.54}$$

$$\eta = \frac{1}{1+2\sqrt{(1+\frac{1}{Q_1Q_2k^2})\frac{1}{Q_1Q_2k^2}}\frac{2}{Q_1Q_2k^2}} \tag{2.55}$$

Figure 2.25: Transformer efficiencies.

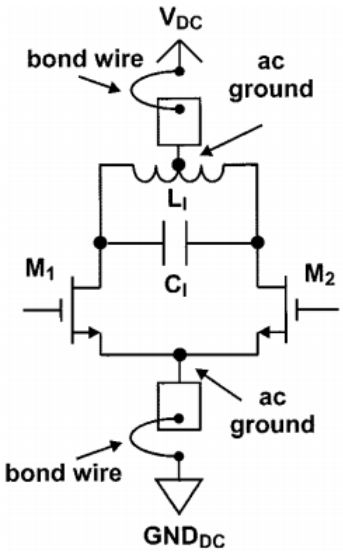


Source: (AOKI et al., 2002a).

A beneficial characteristic of using magnetically coupled transformers as impedance transformation networks is the natural balanced-unbalanced conversion. This can be done simply by driving the primary with a differential amplifier and having one of the secondary ports connected to the ground. This allows for double the output voltage amplitude and is the reason why it is possible to have a higher output power for a differential amplifier than for a single-ended amplifier given the same supply voltage. Another advantage of using a differential amplifier with a transformer is that the amplifier can be biased through the center tap of the transformer, which is an AC ground, this can be seen in figure 2.26. The use of alternate current (AC) grounds is fundamental in integrated power amplifier designs because of the high RF currents that flows through the circuit, if these currents are required to get out of the chip in their return path they cause voltages drop in the bond-wire inductances and degrade the circuits

performance. The use of a differential amplifier implies that the RF differential-mode currents flow only inside the chip, reducing bondwire parasitics effects.

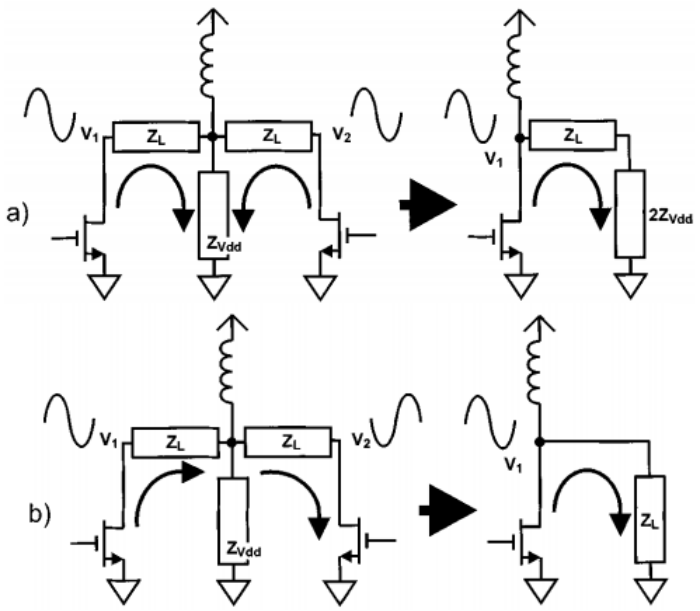
Figure 2.26: Differential amplifier biased through AC Ground in primary center tap.



Source: (AOKI et al., 2002b).

The center tap of the transformer not only can be used as an AC ground but also can be used to define the common mode impedance seen through its ports, and to create a return path for the RF common-mode current. This can be useful for amplifiers that have high frequency common-mode currents such as a class-AB amplifier with high second harmonic current content that cause bond-wire voltage drops. This is illustrated in figure 2.27, where the inductor is an ideal RF choke and thus it can be seen that, in that configuration, the common mode impedance is $Z_L + 2Z_{vdd}$ and the differential mode impedance is Z_L. This way Z_{vdd} can be a bypass capacitor to an internally connected ground to eliminate the common mode current going through bondwires and outside of the chip.

Figure 2.27: (a) Impedance seen by common mode current. (b) impedance seen by differential mode current.



Source: (AOKI et al., 2002b).

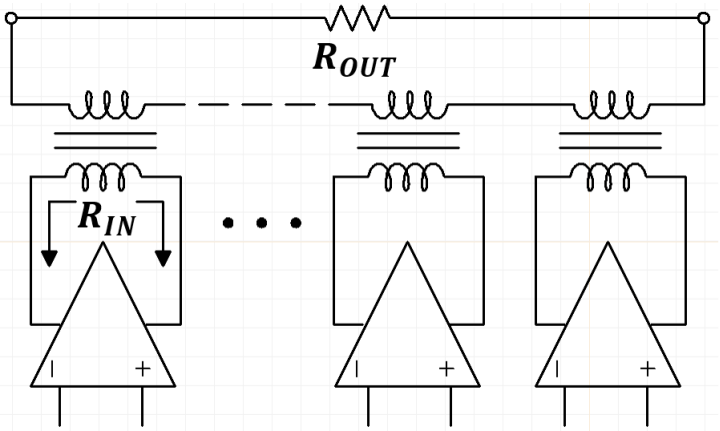
2.3.3 Series Combining Transformer impedance transformation

In order to further improve the possible PER and output power of integrated power amplifiers, networks that use many high-efficiency $1:1$ or $1:2$ transformers were created. These are called power combining networks and the common topologies are the parallel combining transformer (PCT) which have the secondary of the output transformer connected in parallel and series combining transformers (SCT) which have the output transformer secondary connected in series. A SCT is shown in figure 2.28, this network is more intuitive because it adds the output voltage, increasing the output power for a given voltage swing. It also works by reducing the impedance seen by each of the input amplifiers.

In the case of ideal transformers the differential impedance seen by each of the N combined amplifiers R_{IN} is given by 2.56. This means that this network increases the maximum achievable output power for a given technology by two mecanisms: the power combining through output voltage sum and by lowering the impedance at the output of the amplifiers. The PER of this network is given by 2.57 and can achieve high enough values in CMOS to have high efficiency watt-level power amplifiers (AOKI et al., 2002b).

$$R_{IN} = R_{Load}/N \tag{2.56}$$

Figure 2.28: Series Combining Transformer.

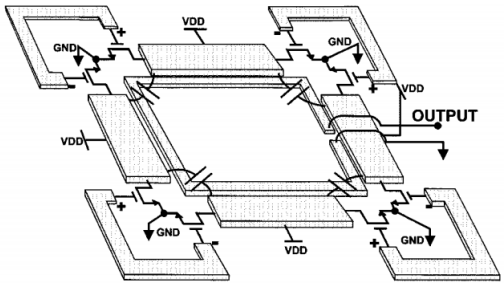


Source: The author.

$$PER = (2N)^2\eta \tag{2.57}$$

There are many ways to construct a SCT layout, and these impact greatly the resulting PA performance. The first one proposed was the distributed active transformer (DAT) that uses slab inductors and the fact that adjacent amplifiers driven in phase have similar currents. Its layout is shown in 2.29. The DAT layout doesn't allow for amplifiers to be turned on and off to achieve higher efficiency in a low power level, and consume a huge area, this problem was solved when spiral inductors SCTs started having a Q high enough to permit its use. This layout is shown in 2.30.

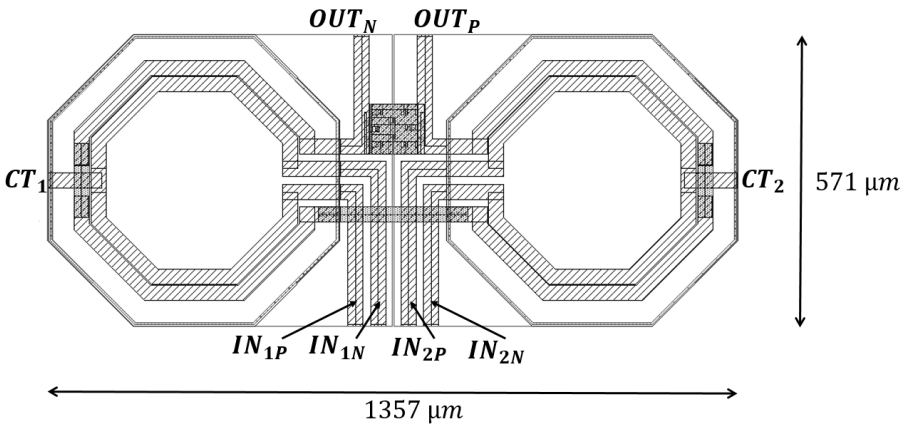
Figure 2.29: DAT Layout example.



Source: (AOKI et al., 2002b).

The SCT structure offer the same balanced-unbalanced conversion than a simple 1:n transformer. An important issue is that, for efficiently decoupling the power supply the SCT

Figure 2.30: Spiral SCT layout example, from this work.



Source: The author.

layout must provide low-impedance paths from the primary center-taps to the amplifiers differential ground for the decoupling capacitors.

2.4 Power Amplifiers state-of-the-art

	[1]	[2]	[3]	[4]	[5]	[6]	[7]
Technology	$90nm$	$90nm$	$180nm$	$90nm$	$40nm$	$130nm$	$65nm$
Supply (V)	3.3	3.3	4.5	3.3	1.5	3.3	3.3
Load Impedance transformation	On-Chip	On-Chip	Off-Chip	On-Chip	On-Chip	Off-Chip	Off-Chip
Frequency (GHz)	2.4	2.4	1.85	2	1.9	2.4	2-6
$P_{Sat}(dBm)$	30	33.5	-	-	28	31.6	22.4
$PAE_{Pk}(\%)$	33.1	37.6	-	-	34	39.6	28.4
Modulation	WiMAX	WLAN	LTE10M 16QAM	WCDMA	LTE 20M 16QAM	WCDMA/LTE 20M QPSK/16QAM	WLAN 20M-80M 64QAM/256QAM
$P_{avg}(dBm)$	22.7	25.7	26	28	23.4	28/27	13.24/10.63
$PAE@P_{avg}(\%)$	12.4	20	31.5	30	23.3	26/22.2	-
$ACLR@P_{avg}(dBc)$	-	-	-32	-34 35MHz offset	-30 EULTRA	-35/-32.1 5MHz Offset/EULTRA	-
$EVM@P_{avg}(dB)$	-25	-28	-	-	-23	-28.1/-32.9	-28/-32

[1] - ISSCC - (CHOWDHURY et al., 2009)
[2] - CICC - (AFSAHI; LARSON, 2010)
[3] - EuMIC -(PARK et al., 2012)
[4] - ISSCC - (KANDA et al., 2012)
[5] - ISSCC - (KAYMAKSUT; REYNAERT, 2014)
[6] - ISSCC - (AREF; NEGRA; KHAN, 2015)
[7] - ISSCC - (YE; MA; YEO, 2015)

Table 2.1: State-of-the-art Linear CMOS amplifiers

The table 2.1 shows a list of CMOS power amplifiers with their respective performances. The works on the table were chosen based on being PAs for linear communication standards and operating at the low GHz range. It is hard to compare directly the PAs in the literature because they have a wide range in their application spectrum in terms of output power, bandwidth, integrability, linearity, etc. The bibliography of High-end CMOS PAs is sparse because the

subject is complex and expensive to develop, usually a working PA occupies an entire chip with large area and is not rare for the amplifier to not properly function on the first tapeout.

We can see that the bulk of the CMOS power amplifiers publications are in the $180nm - 40nm$ range. It is easy to see how the voltage supply and output power scales with the node, the $180nm$ amplifier in (PARK et al., 2012) has a supply of $4.5\ V$ with the highest average output power of $26\ dBm$ while the $40nm$ amplifier in (KAYMAKSUT; REYNAERT, 2014) has the lowest supply of $1.5\ V$ and the lowest average output power of $23.4\ dBm$ besides (YE; MA; YEO, 2015).

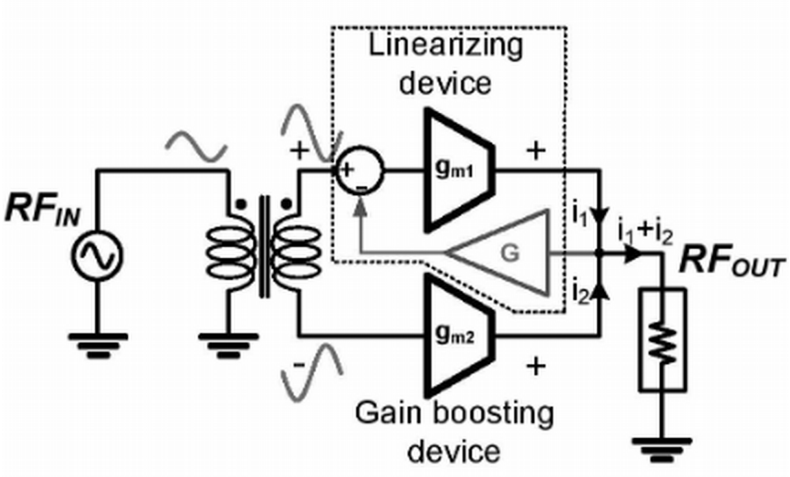
The amplifier from (YE; MA; YEO, 2015) doesn't use power combining and has a much different focus, it is supposed to replace many narrow-bandwidth amplifiers in the $2 - 6GHz$ range with a single wideband amplifier. It also has a focus in protocols that require extreme linearity such as wideband LTE and 802.11n/ac. (YE; MA; YEO, 2015) is also the only published CMOS amplifier to date to demonstrate operation with a 256QAM signal. That is why this amplifier is in this table even when its output power is an order of magnitude lower than the others.

The amplifiers in (AFSAHI; LARSON, 2010) (CHOWDHURY et al., 2009) (PARK et al., 2012) (YE; MA; YEO, 2015) are class AB. The chip in (KANDA et al., 2012) is actually a module with three WCDMA power amplifiers for triple-band operation in $800\ MHz$,$1.7\ GHz$ and $2\ GHz$, the one in $2\ GHz$ is taken for comparison but the paper does not specify any of the amplifiers classes of operation.

The amplifier in (KAYMAKSUT; REYNAERT, 2014) is a Doherty topology combining a class B and a Class A amplifier for high-efficiency at average output power. This work acts as a proof of concept of the interesting idea of transformer-based integrated Doherty amplifiers. This topology, when realized with $\lambda/4$ transmission lines, is extremely popular in the discrete amplifier market but these transmission lines have their sizes in the many cm range for low-gigahertz frequencies, which makes the classical topology unpractical to integrate.

The amplifier in (AREF; NEGRA; KHAN, 2015) is a novel topology that the authors named "class-O", it consists of a main amplifier that is responsible to deliver the bulk of the output power and another amplifier with RF feedback as can be seen in figure 2.31. The auxiliary amplifier has a much lower current capacity and is responsible to improve the linearity of the system. Despite the new architecture both individual amplifiers were biased in class AB for optimum linearity. This work is also a proof-of-concept for this technique so an external load tuner was used to present the amplifier with optimal load.

Figure 2.31: Class-O amplifier topology.



Source: (AREF; NEGRA; KHAN, 2015).

The oldest work on the list is (CHOWDHURY et al., 2009) from 2009. It is a two-stage fully-integrated class-AB amplifier that uses several techniques that have become widespread in linear PA design. It uses a complex network at the center tap of the output transformer that has low impedance at the second-harmonic while also having low Q for a high-frequency range, avoiding any high Q resonances with parasitic inductances from the DC-feed bond-wire that can cause common-mode instability.

3 RF POWER AMPLIFIER DESIGN

A power amplifier requires a large on-chip area and is a challenge on its own to integrate its load impedance transformation network, even without large area concerns. This meant that the usual MOSIS research yearly tapeout that the UFRGS GME-AMS (the research group that the student is part of) was not a viable for fabrication of this project since it is shared among many students and another tapeout venue without financing was necessary. Luckily for the student, Europractice and IMEC offers free IC fabrication for Brazilian students up to 5 seats per semester through the mini@sic program. This work was applied for a free prototyping through this program and was granted. The technology is a Taiwan Semiconductor Manufacturing Company (TSMC) $0.18\mu m$ CMOS with mixed-signal and RF enhancements such as one thick metal layer for RF passives that is a 2.3 μm aluminum layer. The chip area is 1570 μm x 1570 μm.

3.1 Power amplifier specifications

Given the constraints given by the tapeout specifications shown above, the student set out to find a communication standard for the proposed power amplifier. One of the requisites was that the standard required a highly linear PA, which removed from the list of possible standards many 2G mobile protocols such as GSM, and let open WLAN and 3G standards such as the ones shown in the survey in table 2.1. The 3G standards require average output power on the order of 25dBm, and a saturated output power on the order of 33dbm, depending on the necessary power back-off to meet mask and EVM requirements linearity requirements. For WLAN the power requirements are on the order of 10dB lower, for instance, the maximum average output power for the 802.11g is $40mW$. If we take into account area and technology constraints, and compare them to the 3G amplifiers reviewed in the literature which frequently have an area bigger than $4mm^2$, a WLAN power level is more suitable for the proposed PA. Also, due to the fact that the laboratory instruments such as RF signal source and Spectrum Analyzers bandwidth is limited to 3GHz the choice of WLAN standard is between 802.11g and bluetooth class 1, of which the first was chosen because it is a common standard for CMOS amplifiers in the literature and also has higher linearity requirements due to high number of OFDM sub-carriers and dense modulation standards.

The table 3.1 describes the requirements of the proposed amplifier.

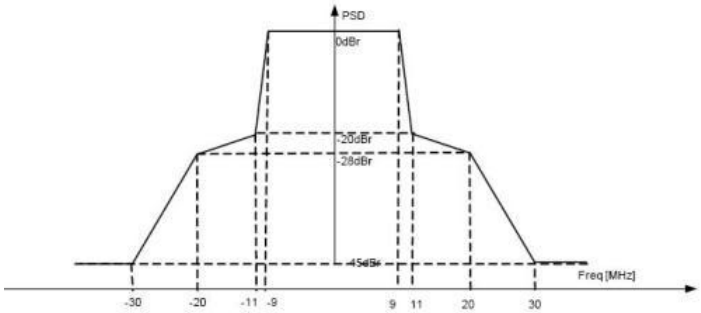
*Specification must be as high as possible for given chip area.

Spec	Value
Technology	$180nm$
Supply Voltage	$3.3\ V$
Frequency	$2.402 - 2.483\ GHz$
$P_{avg}*$	$16\ dBm(40\ mW)$
$P_{Sat}*$	$24\ dBm(250\ mW)$
$\eta_{max}*$	30%
$_{max}*$	28%
Power Gain*	$10\ dB$

Table 3.1: Proposed CMOS PA specifications

The overall ratio between the maximum saturated power and the average power, called back-off, depends on how linear the amplifier is or, equivalently, how "fast" it stops being linear and fully compress in a compression test. Because we cannot know precisely this a priori, we take a common value of 8dB back-off for the 802.11g standard, but this is not final, and only true masks and EVM tests can confirm that the amplifier can transmit that average output power. The EVM requirement for the standard can be seen in table 3.2, for a 64-QAM signal with 54Mbps rate the requirement is $EVM_{RMS} = 5.6\%$ or $EVM_{dB} = -25\ dB$. The required spectrum mask can be seen in figure 3.1.

Figure 3.1: 802.11g spectrum mask.



Source: (RF CAFE, 2015).

Rate (Mbps)	$EVM_{RMS}(\%)$	$EVM_{dB}(dB)$
6	56.2	-5
9	39.8	-8
12	31.6	-10
18	22.3	-13
24	15.8	-16
36	11.2	-19
48	7.9	-22
54	5.6	-25

Table 3.2: 802.11a/g EVM requirements

3.2 Topology and floorplan

Given the specifications in table 3.1, the designer must survey the possible topologies in order to chose one that can fit in the constraints and satisfy these specification requirements. Due to advantages such as high power enhancement ratio, high efficiency and high robustness against bondwire parasitcs for full integrability described in detail in 2.3.3, the chosen topology was a transformer power combining network. Between the SCT and the alternative PCT, the series combining was chosen because of it requires lower turn-ratio transformers, making its transformers easier to design in an technology with high passive loss for the same necessary PER. To define the number of combined amplifiers we must look at the supply voltage and the necessary output power. The supply voltage of the thick-oxide transistors of the technology is $3.3\ V$. For a knee voltage of $800\ mV$ that is reasonable for a cascode cell (PA designs often use cascode cell for increased stability, and in the case of CMOS to have high supply voltages of thick-oxide transistors while having high power gain of thin oxide transistors), we can calculate the maximum output power when directly connected to a $50\ \Omega$ load given by equation 2.3 can be seen in equation 3.1.

$$P_{out,50\Omega} = 2.5^2/(2 * 50) = 62.5\ mW = 17.95\ dBm \tag{3.1}$$

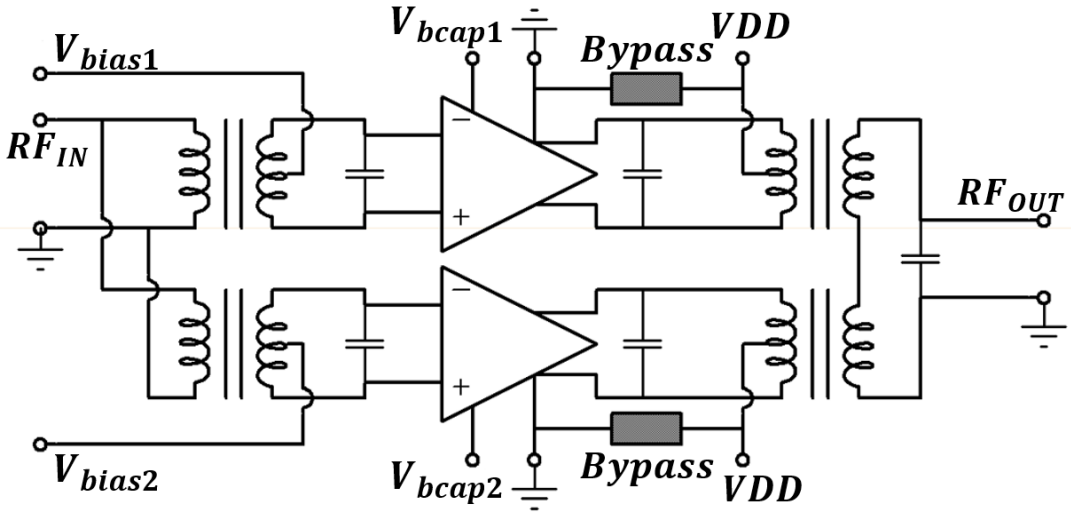
This means that a PER of 5 is necessary for a $25\ dBm$ output power. By combining two differential amplifiers (four active devices) in a SCT we have a PER given by 2.57 that is shown in equation 3.2. With $\eta = 70\%$ the maximum output power is $28\ dBm$, well above the necessary $24\ dBm$.

$$PER = 16\eta \tag{3.2}$$

The proposed topology can be seen in figure 3.2. In this diagram we can see tuning

capacitors at the input of the active cores for input matching, at the output of the amplifier for SCT for maximum efficiency as described in section 2.3.2, and also at the output of the active core to adjust the input impedance of the SCT seen by the amplifier. It is also possible to see bypass networks for 2nd harmonic tuning connected to the center taps of the SCT transformers and active core AC grounds.

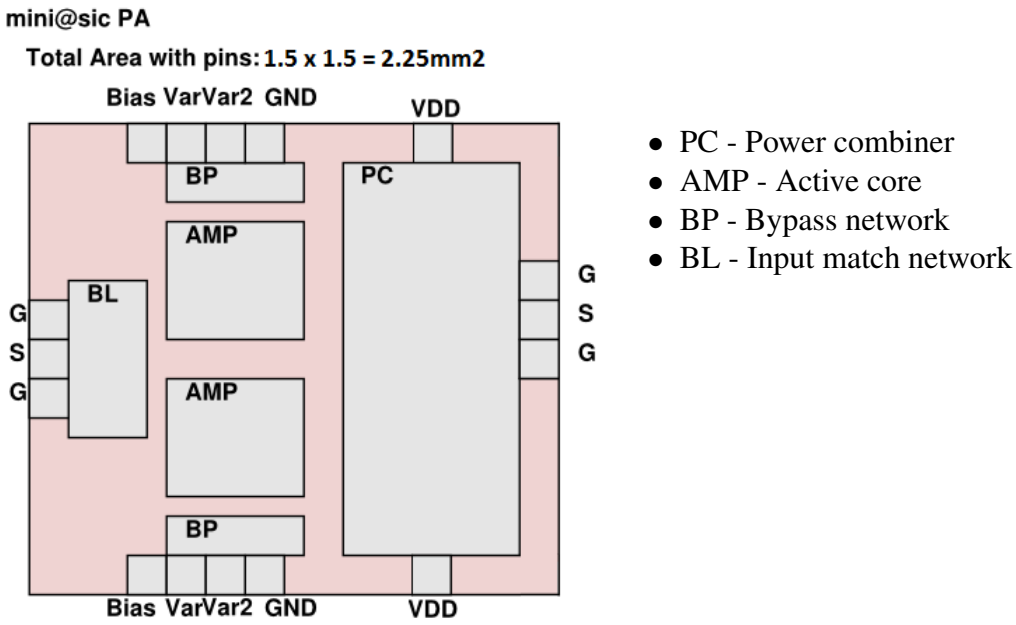
Figure 3.2: Power Amplifier block-level topology



Source: The author.

One can estimate the SCT area by looking at similar works like (CHOWDHURY et al., 2009), which has an SCT that combines two amplifiers with the area of approximately 400 x 850 μm. A proposed floorplan for the PA is shown in Figure 3.3, where PC is the power combiner. A bigger area was reserved for the combining transformer - around $0.5x1.2$ mm^2 than in the previously cited work. The field AMP denotes the area of each of the two amplifier active cores, BP is the 2nd harmonic tuning network and BL is the input matching and power splitter network. The amplifier is expected to be as symmetric as possible and the bias signals on the top and bottom of the amplifier are expected to be fed through wirebondings from a PCB direcly, which is a technique called chip-on-board packaging. The input and output RF signals are going to be accessed through GSG microprobes, to lessen the effect of bondwire parasitics.

Figure 3.3: Proposed power amplifier chip floorplan.



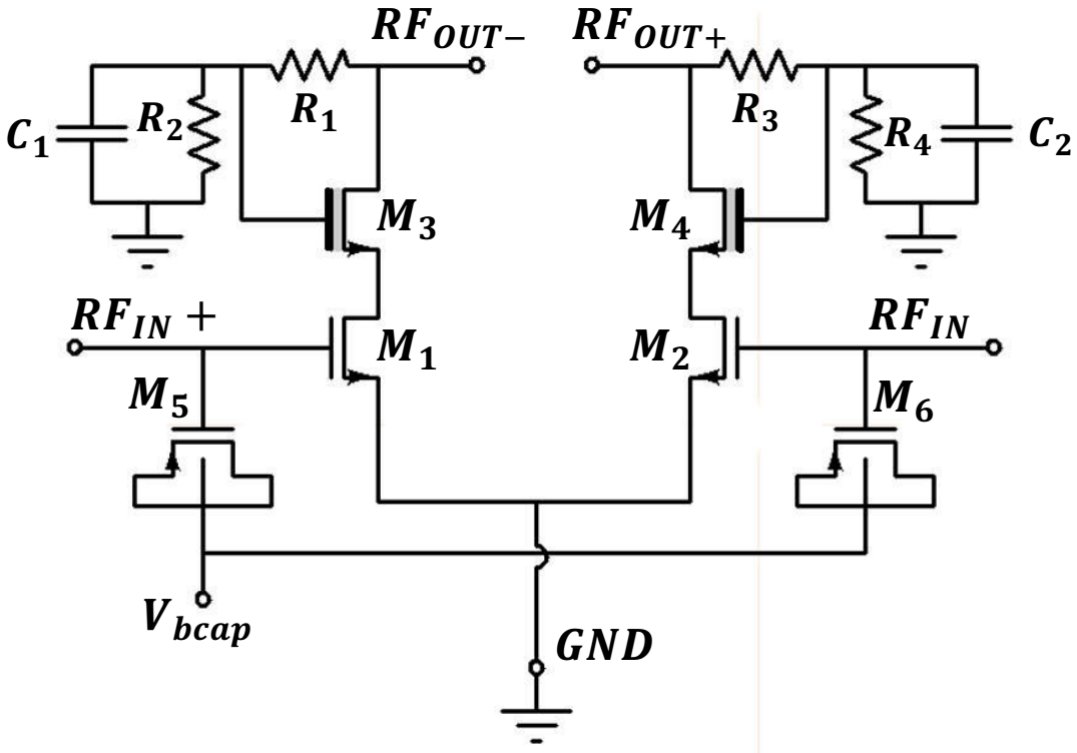
Source: The author.

3.3 Class-AB active core design

The proposed active core topology is a thick-thin oxide transistor cascode shown in Figure 3.4. $M_{1,2}$ are thin oxide transistors that act as common-source transcondutors in the amplifier, $M_{3,4}$ are thick oxide cascode devices that bear most of the high-voltage stresses of the output signal, protecting $M_{1,2}$ while $M_{5,6}$ are PMOS devices that linearizes the input capacitances of $M_{1,2}$ as described in detail in 3.3.1. Moving to the passives, the ratio $R_{1,3}$ and $R_{2,4}$ defines the gate bias of transistors $M_{1,3}$ while capacitors $C_{1,2}$ form a RC filter with the resistors such that the RF components on the gate of the transistors are reduced to an acceptable level. This was made as a way to reduce the number of bias pins and simplify the test bring-up infrastructure.

The design of the active and passive parts of the PA is iterative since one part requires the other for optimization, but it has to start somewhere. To do this the active part is designed as if it was driving an ideal SCT, that is a differential load impedance of $25\ \Omega$ (alternatively a $12.5\ \Omega$ single-ended to ground impedance each branch) and latter, both parts are simultaneously optimized. We start by defining the bias and size of $M_{1,2}$. As described in 2.2, the best bias condition for lowering 3rd harmonic distortion is in class-AB. The common-source transistors bias is set for a unity device, in this case the chosen transistor have $Width = 5\ \mu m$, this is to

Figure 3.4: Active core schematics



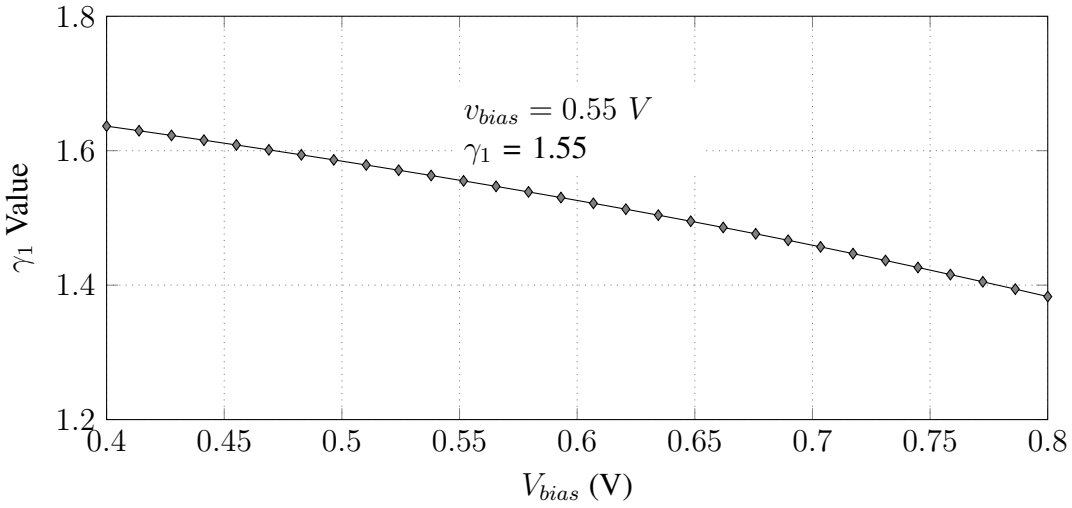
Source: The author.

keep the gate resistance low in the layout of the transistor cell. This transistor is driven with a given input signal swing of $V_{in} = 800\ mV$, a higher input voltage value results in a higher knee voltage and a lower value will require a bigger transistor to generate the same output current. The device is biased such that the relationship between quiescent and first harmonic current defined in 3.3 (KAZIMIERCZUK, 2014), where $\alpha_{conduction}$ is the conduction angle, γ_1 is the ratio of fundamental harmonic current I_1 and the quiescent current I_Q. Figure 3.5 shows a bias sweep where upon the transistor bias is chosen to be $V_{bias} = 550\ mV$.

$$\alpha_{conduction} = 240^o => \gamma_1 = \frac{i_1}{I_{DC}} = 1.57 \tag{3.3}$$

The harmonic currents can be seen in 3.6, where it is possible to see the minimum in third harmonic current and extract the DC and first harmonic currents. The unity transistor need to be scaled to give the necessary first harmonic output current for full voltage swing with a $12.5\ \Omega$ load. The current at the fundamental harmonic on the previous condition is $i_1 = 857\ \mu A$, the necessary current for a full voltage swing of $v_1 = 2.5\ V$ is given by equation 3.4. To achieve this current we must scale the transistor sizes by the same amount, with a total

Figure 3.5: Transconductor transistor γ_1 as a function of bias.

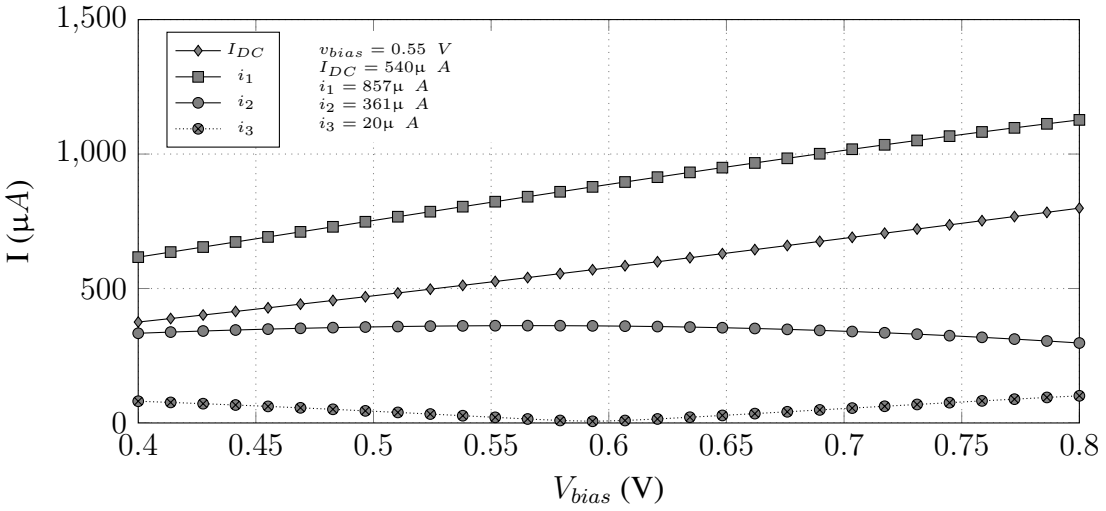


Source: The author.

number of 234 transistor cells to make up the necessary current and a total width of $1.17\ mm$, the final harmonic current is $195\ mA$ due to second order effects.

$$i_1 = 2.5/12.5 = 200\ mA \tag{3.4}$$

Figure 3.6: Transconductor harmonic currents as a function of bias



Source: The author.

After this, the cascode device size and bias must be chosen. This transistor is a $3.3V$ I/O device build from unity "transistors" with a channel length of $l = 350nm$ and a width of $5\mu m$, and it is designed with the constraint that it is capable of sustaining the output current

without driving the transconductor transistor into the triode region. For this both the bias and the number of fingers are adjusted simultaneously to find an optimal point. First a simulation is done to make the source voltage of this transistor equal to some value near the $1.2V$ of nominal supply voltage for the transconductor transistor and then another simulation with the driving signal of $v_{in} = 800mV$ and full load makes sure that the transistors are not getting into triode region by looking at the output current harmonic content.

The final number of fingers is 288 and the final width of the cascode transistors is $1.44mm$ for a gate bias voltage of $V_{G,Cascode} = 2.2V$.

3.3.1 AM-PM non-linearity compensation

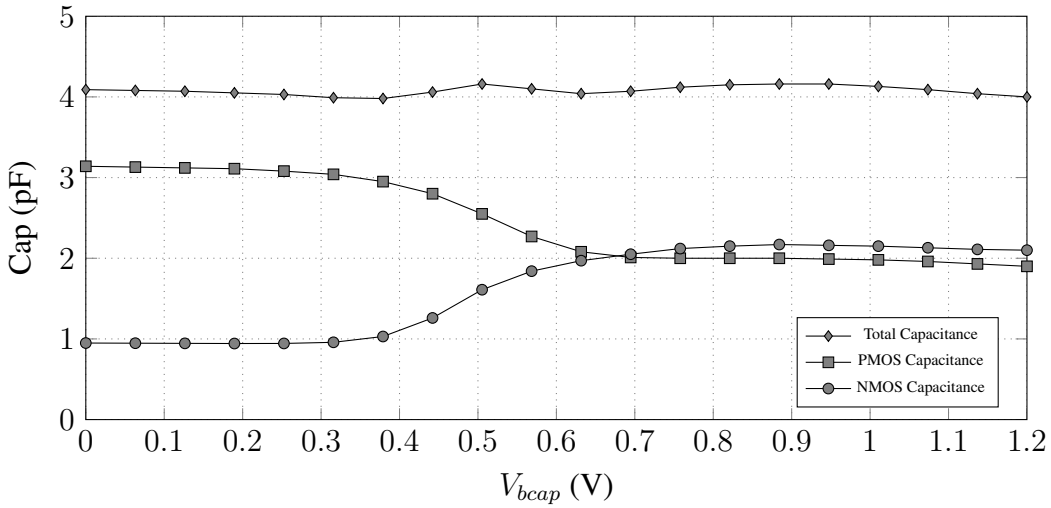
In schematics 3.4 transistors $M_{5,6}$ are PMOS devices that acts as non-linear capacitors, these devices can counterbalance the natural non-linearity of the input capacitance of NMOS transistors $M_{1,2}$ under large signal input. This technique was first demonstrated in (CHOWDHURY et al., 2009). The design method is purely by simulation, trying to adjust the inflection point of the compensation capacitance curve by changing V_{bcap} and its total value by the width of the PMOS transistors, which has the minimum channel length of $180nm$, the equivalent input capacitance of the amplifier is increased and approximately doubled. The input capacitance of the NMOS devices without compensation, the input capacitance of the PMOS devices and the final equivalent input capacitance with compensation can be seen in figure 3.7.

The final designed value for V_{bcap} is $1.08\ V$ and the total width is $1.8mm$ in the form of 2 multipliers of 30 fingers each with $30\mu m$.

3.3.2 Cascode Bias network and final transistor sizes

To finalize the active core schematics design it is necessary to design the RC filter that scale down the output signal to make the cascode bias network. For this the ratio of $R_{1,3}$ and $R_{2,4}$ defines the gate DC voltage as described by 3.5 and 3.6, and the RC constant must be high enough as reduce the ripple of the output signal on the DC bias and not degrade the PA

Figure 3.7: Input capacitance with non-linear compensation.



Source: The author.

performance - this happens when $M_{3,4}$ lowers their source voltage enough as to drive $M_{1,2}$ into triode - and it must have reasonable area for layout.

$$V_{G,Cascode} = 3.3\frac{R_{1,3}}{R_{1,3} + R_{2,4}} = 2.2V \tag{3.5}$$

$$R_{2,4} = 2R_{1,3} \tag{3.6}$$

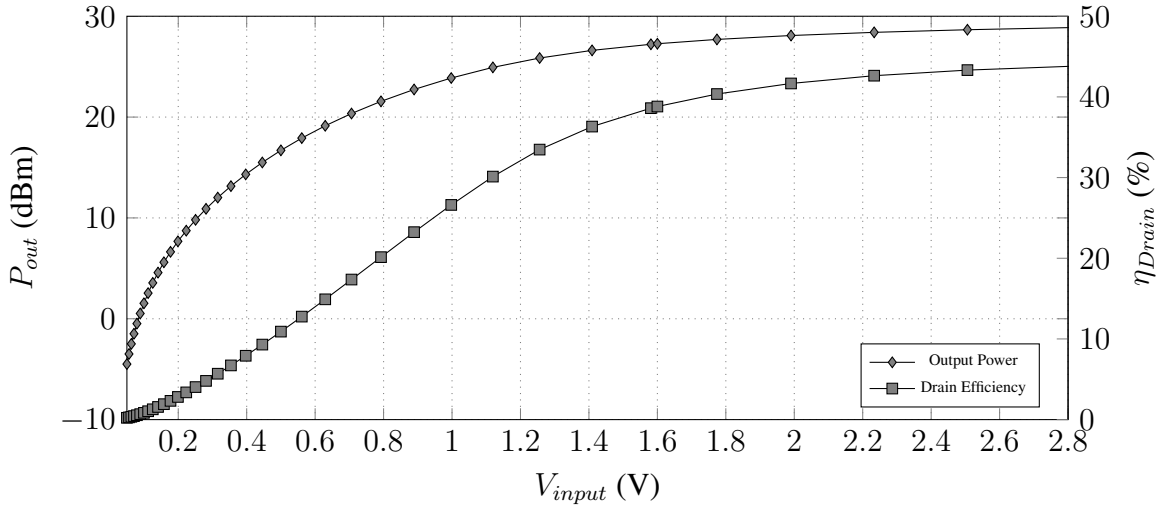
The capacitors $C_{1,2}$ are implemented as 8 parallel $30x30$ μm^2 MIM capacitors each with 1.79 pF for a total of 14.32 pF. The resistors $R_{1,2}$ are implemented as 10 series bars of high resistivity poly resistors of length 10 μm and width of 1 μm for a total resistance $117k$ Ω. Resistors $R_{2,4}$ are implemented with 20 series bars of the same unity resistor. The final values of the passives are shown in Table 3.3.

Table 3.3: Passive devices sizes

Passive	Value
$C_{1,2}$	14.32 pF
$R_{1,2}$	117 $k\Omega$
$R_{3,4}$	234 $k\Omega$

The results of output power and efficiency of the schematics with an ideal power combiner and driven by an ideal single-tone voltage signal source are presented in figure 3.8. The saturated output power is 28.8 dBm, the drain efficiency at this output power is 43.8%.

Figure 3.8: PA results from schematic active core and ideal load transformation network.

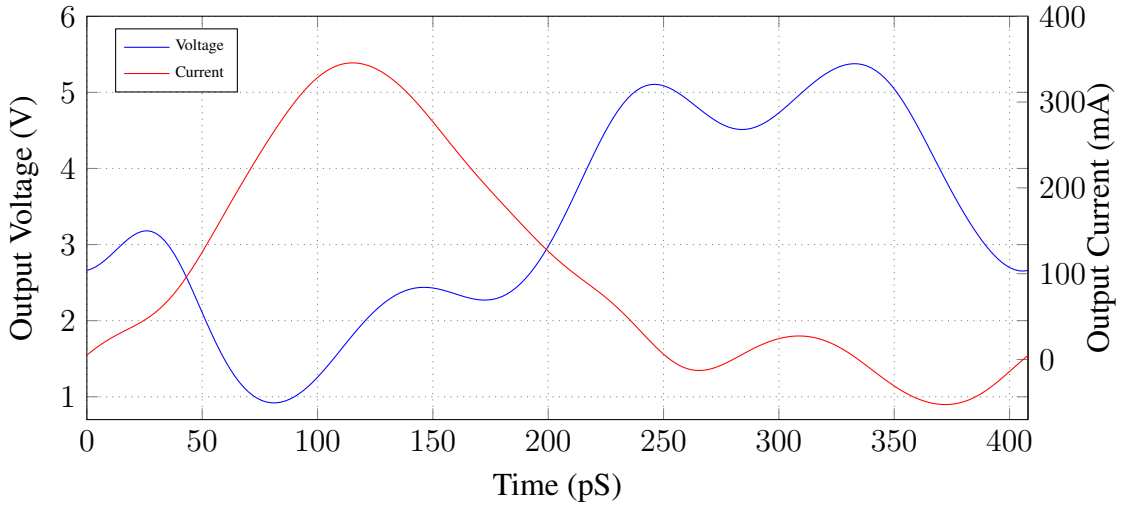


Source: The author.

The current and voltage waveforms at $V_{in,diff} = 1.6\ V$ or $V_{in,branch} = 800\ mV$ can be seen in figure 3.9, where the peak voltage is $V_{peak} = 5.37\ V$ and peak current is $I_{peak} = 345.1\ mA$. It is also possible to see that these waveforms does not visually conform to the expected class-AB waveforms, in this stage the design is terminated by an ideal tuned LC filter at the second harmonic, the first harmonic voltage content is $1.827\ V$, the second harmonic is $9.4\ mV$, the third harmonic is $14.95\ mV$ and the fourth harmonic $612.1\ mV$. The current harmonics are $I_1 = 166.3\ mA$, $I_2 = 64.35\ mA$, $I_3 = 1.5\ mA$, $I_4 = 18.12\ mA$. The fourth harmonic ($9.8\ GHz$) is responsible for most of the distortion seen in 3.9 as the class-AB amplifier generates high fourth harmonic current and this design isn't terminated in the fourth harmonic. Although the even harmonics such as second and fourth do not appear at the load due to these signals being common mode in a differential amplifier, the voltage waveforms at the drain of the transistors can drive them into triode and compress the gain. This degrades the performance by increasing odd mode non-linearity and decreasing efficiency, and can be thought of as the harmonic voltage consuming supply voltage headroom and making the current non-zero when the voltage is high. The forth harmonic problem will be alleviated when the circuit is in layout and a tuned power combiner is connected as load because of the limited bandwidth of the transformers, while the second harmonic problem will get worse as the ideal filter is replaced by second harmonic tuning network on the center tap of the transformers.

This active core design was optimized based on simulation after the introduction of the EM-simulated SCT presented in 3.4 The very final version of the amplifier active core transistor sizes are shown in 3.5. In this version the transconductor transistor was divided in 12 multipliers

Figure 3.9: Schematics single-ended branch current and voltage waveforms.



Source: The author.

of 18 fingers for a total of 216 unity transistors and the cascode transistor was kept with the same 12 multipliers of 24 fingers.

Table 3.4: Output power and PAE load-pull circles

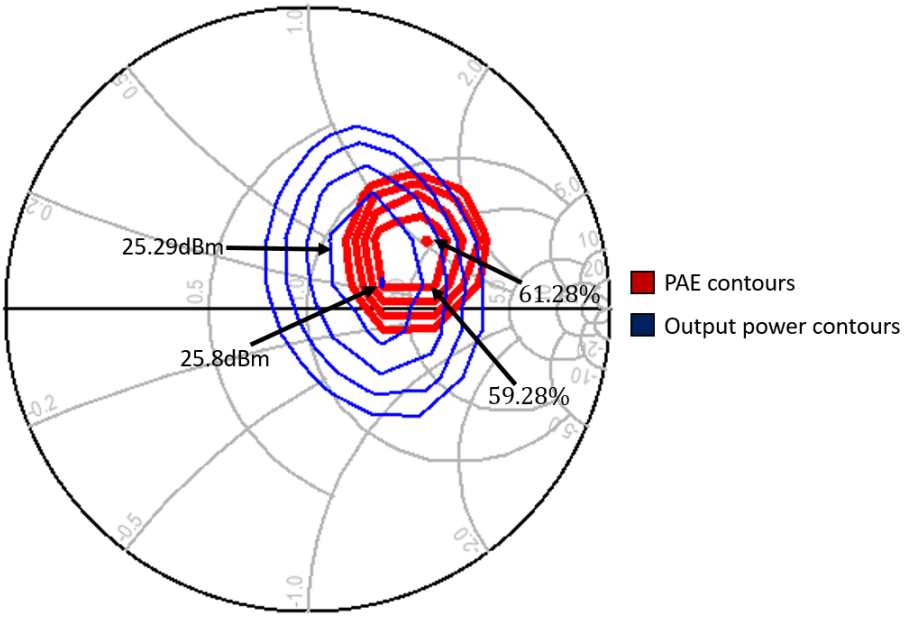
Table 3.5: Transistor sizes

Transistor	W (mm)	L (nm)
$M_{1,2}$	1.08	180
$M_{3,4}$	1.44	350
$M_{5,6}$	1.8	180

3.3.3 Active core load-pull

Load-pull simulation was performed on a single active core at the schematics level using Keysight Advanced Design System (ADS). The circuit is stimulated with a constant $1.6\ V$ differential input voltage - $800\ mV$ single-ended voltage as before - and the fundamental load is swept in the complex plane while all of the other harmonic loads are kept as zero (that is, a perfect short). The output power and PAE circles can be seen in figure 3.10. The impedances are normalized to $Z_0 = 25\ \Omega$ which is the expected impedance at the output of the amplifier. The maximal output power is $P_{o,max} = 25.8\ dBm$ and is achieved with the load impedance $Z_{max,po} = 41 + j6.7\ \Omega$. While the maximum PAE is $PAE_{max} = 61.28\ \%$ and is achieved with the optimal load impedance of $Z_{max,PAE} = 47.52 + j26.1\ \Omega$. To compare this power result to

Figure 3.10: Output power and PAE load-pull circles.



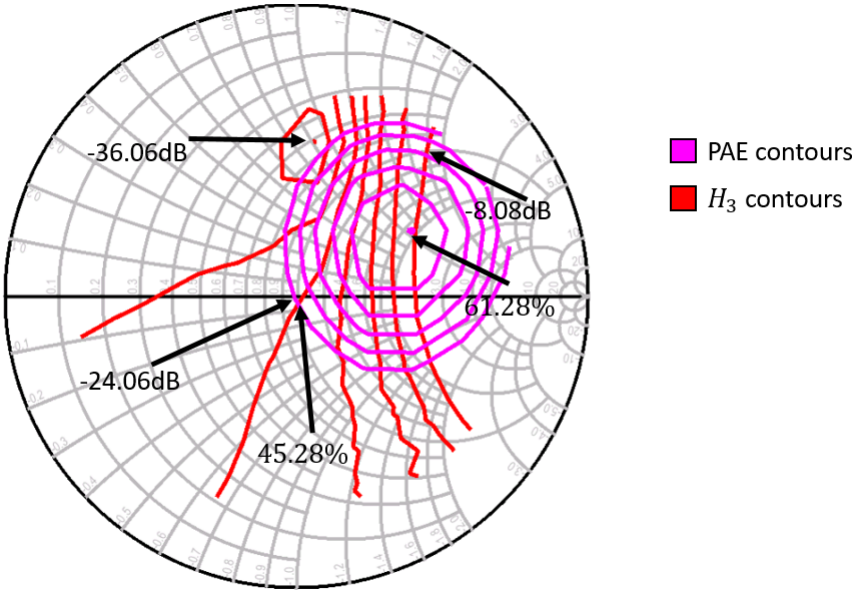
Source: The author.

the achieved previously we must add 3dB to compensate to the fact that this is a single active core while the previous $28.8\ dBm$ in the Harmonic Balance test-bench was achieved with two active cores ideally combined.

Harmonic tuning is important, by not terminating harmonics with short circuits the impedance seen is the reactance of the transistors drain capacitance at those harmonics. Simulation shows that not terminating the fourth harmonic of the signal as in the proposed topology degrades the PAE with the previous optimum load to 46.1%, while not terminating any harmonic at all degrades the PAE to 20% at the output power of $21.5\ dBm$, that is because the load circle shifts for these conditions due to the reduced voltage headroom for the amplifier.

What is not evident from the load-pull simulation is linearity. While the circles show that a higher drain impedance would result in higher efficiency, that is done by increasing the first harmonic voltage and thus driving the transistor further into triode. That is, it is evident that we can make the amplifier more efficient by making it more non-linear. A good and simple measure for linearity is the ratio of the third and first harmonic currents, this way we define H_3 as in equation 3.7. It is possible then to see the dependence of third harmonic non-linearity with the load in the load-pull in figure 3.11, where the linearity-efficiency trade-off is evident. The minimum value for H_3 is $-36.06\ dB$ and is achieved for a load impedance of $Z_{min,H3} = 15.32 + j22.73\ \Omega$. H_3 is degraded to $-8.06\ dB$ at the maximum PAE point which shows the

Figure 3.11: H_3 and PAE load-pull circles.



Source: The author.

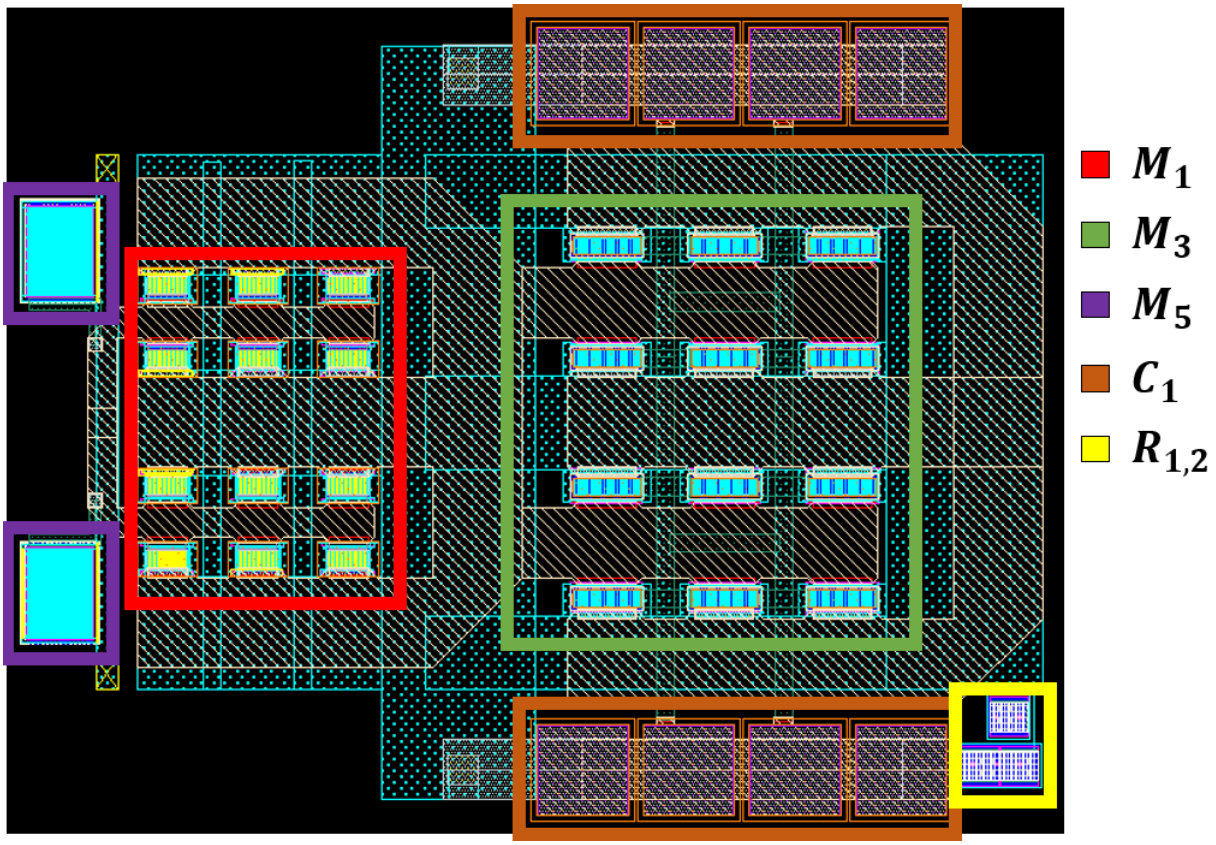
amplifier saturation. In the real use case the input power is not constant, that is, for a higher input power these circles will move, that is why the traditional load-pull design method wasn't used. The center point presents a good tradeoff between non-linearity and PAE with $H_3 = -24.06\,dB$ and $PAE = 45.28\%$.

$$H_3 = 20log(\frac{i_3}{i_1}) \tag{3.7}$$

3.3.4 Ative core layout

The transistor cell layout is based on the work in (WANG et al., 2010), in that work a novel layout is proposed where the power cell is partitioned and each part is placed at some distance from the others to help mitigate realiability issues caused by thermal effects such as hot carrier injection. The layout on the paper is for a 4 multiplier single power transistor, in this work we take that concept and propose a new cascode device layout as shown in figure 3.12. This layout focus on minimizing transistor terminals resistances, metal-1 acts as a ground plane except where the transistors cells are placed. Both gate and drain are connected through thick-metal traces for both the transconductor and cascode devices. It has an area of 350 x 270µ m^2

Figure 3.12: Cascode device layout with feeedback RC network and non-linear input capacitance compensation.

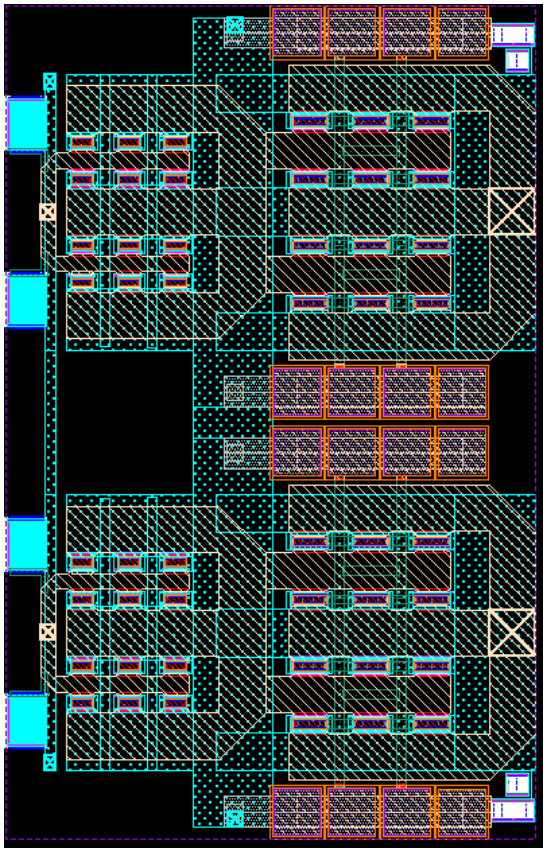


Source: The author.

The active core layout is shown in figure 3.13 and consists of two active devices mirrored for a symmetrical differential amplifier. It's total area is 350 x 550 μm.

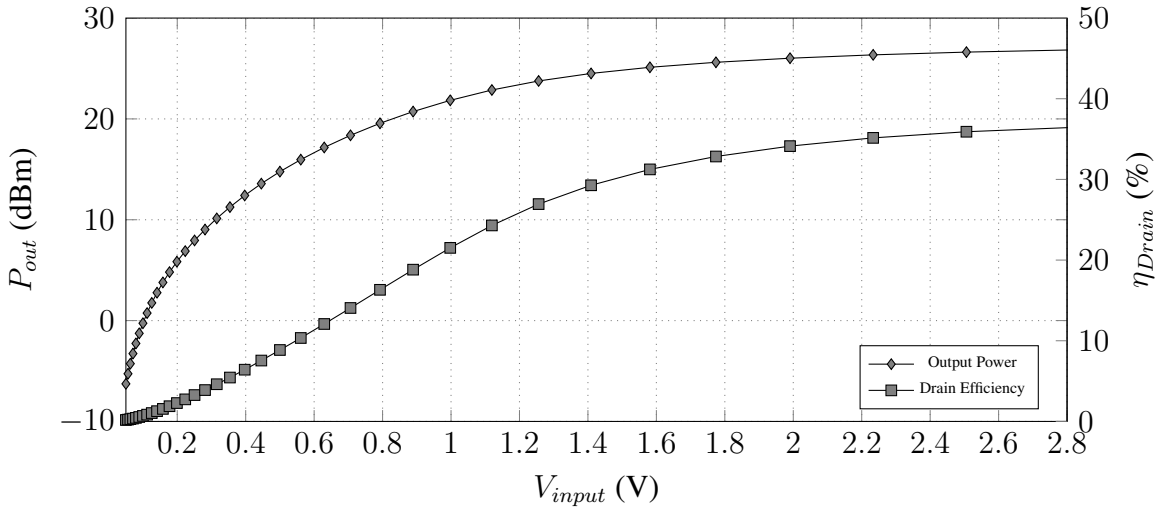
The results from the extracted layout with RC parasitics and ideal load transformation network can be seen in figure 3.14. The maximum output power is 26.8 dBm and maximum drain efficiency is 36.4%.

Figure 3.13: Active core layout.



Source: The author.

Figure 3.14: PA results with extracted layout of active core and ideal load transformation network.



Source: The author.

3.4 Power combiner

The power combiner is a symmetrical serial combining transformer and it consists of two identical transformers with primary driven by active cores and secondary connected in series. The transformer must be laterally coupled because the technology only offers one thick-metal layer: An aluminum layer with 2.3 μm and a sheet resitance of $17.73\ m\Omega/\square$, this also limits high-efficiency transformers to single-winding configuration. The design process begin by the design of the individual transformers, these are optimized for the operating frequency of $2.45\ GHz$ and under a load of $25\ \Omega$, and have a $1:1$ transformation ratio. From this one can find out the optimal inductance for both the primary and secondary as defined in equation 3.9, already presented in section 2.3.2. In order to do this we must assume the windings quality factors Q and coupling factor k. We select typical values of $Q = 12$ and $k = 0.8$. for these parameter values and under this impedance environment the optimal reactance of the transformer windings to minimize its insertion loss is given by 3.10, that at $2.45\ GHz$ corresponds to the inductance value shown in the same equation.

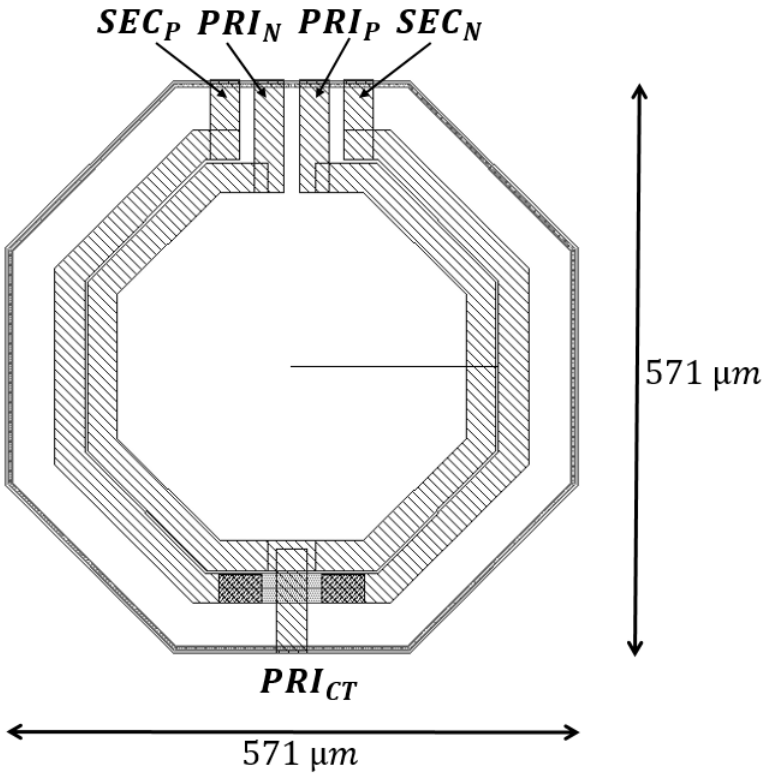
$$A = \frac{1}{\sqrt{\frac{1}{Q_2^2} + \frac{Q_1}{Q_2}k^2}} \tag{3.8}$$

$$\omega L_1 = \frac{A.R_l}{n^2(1+A^2)} \tag{3.9}$$

$$\omega L_1 = 11.87\Omega => L_1 = 771pH \tag{3.10}$$

The transformer has transformation ratio of $1:1$ to avoid using the lower metals as the technology has one thick-metal layer only, reducing parasitic resistance and loss. The necessary inductance value is large for a single-winding transformer so it is imagined that the this components area is going to be big. For instance, an inductor with trace width of $30\ \mu m$ and an inner diameter of $300\ \mu m$ has an inductance of approximately $670\ pH$ and one with an inner diameter of $400\ \mu m$ has an inductance of $1.2\ nH$. The designed inductor has a inductance that is close to the ideal with $L = 877\ pH$, the total outer area of this inductor, with guard ring, is 571x$571\ \mu m^2$, this inductor was chosen as a good compromise between inductance and area as the optimal inductance value varies with the windings Q. The transformer layout can be see in figure 3.15.

Figure 3.15: SCT unit transformer layout.

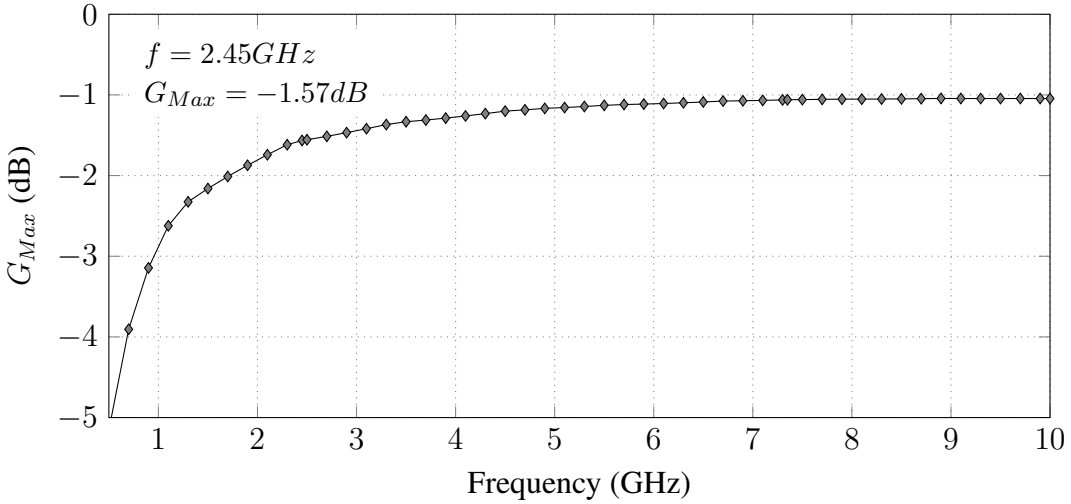


Source: The author.

The S-Parameters of the transformer were extracted using Keysight Momentum via EM simulation, for this simulation the S-parameters were extracted for a frequency of up to 10GHz with a fine mesh of 100 cells per wavelength. The parameter G_{Max} can be seen in the graph 3.16 and has a value of $-1.57\ dB$ at $2.45\ GHz$ which represents a maximum efficiency of 69.7%. The T-model parameters were also extracted from the S-Parameters and are presented in table 3.6. With these values we can calculate $Q_P = 10.32$ and $Q_S = 8.61$. The coupling factor and quality factors were lower than the expected, changing the optimal reactance. The presented version of the transformer was the best one in terms of loss after an iteration design process.

The untuned S-Parameters of the transformer presents little intuitive information about its behaviour, for instance, $S_{21,2.45GHz} = -7.31\ dB$, but this means little in practical terms because most of that loss is due to return loss at the input of the transformer or at the load. To quantify the mismatch $S_{11,2.45GHz} = -1.75\ dB$ and $S_{22,2.45GHz} = -1.95\ dB$. The transformer is tuned for a $25\ \Omega$ environment with parallel mim capacitors at input $C_P = 4.21\ pF$ and output $C_S = 4\ pF$, the obtained S-Parameters can be seen in 3.17, where the loss at $2.45GHz$ is $S_{21} = -1.69\ dB$ that represents an efficiency of $\eta = 67.8\%$.

Figure 3.16: Transformer G_{Max}.

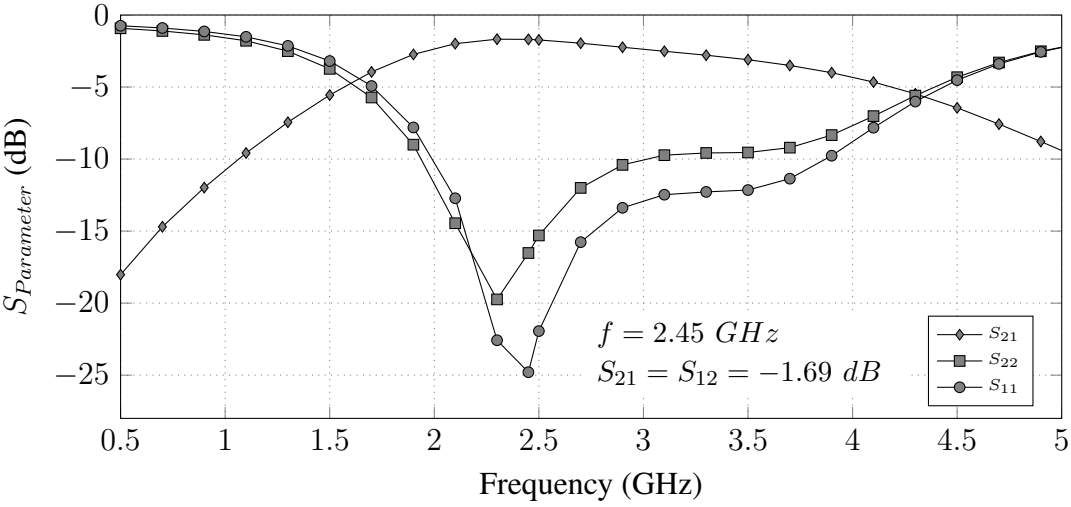


Source: The author.

Table 3.6: Designed Passive Simulation Results at 2.45 GHz

Parameter	Value @ 2.45 GHz
L_P	825 pH
R_P	1.23 Ω
L_S	945.8 pH
R_S	1.69 Ω
k	0.585
G_{max}	-1.57 dB
η_{max}	69.7%

Figure 3.17: Tuned Transformer S-Parameters.

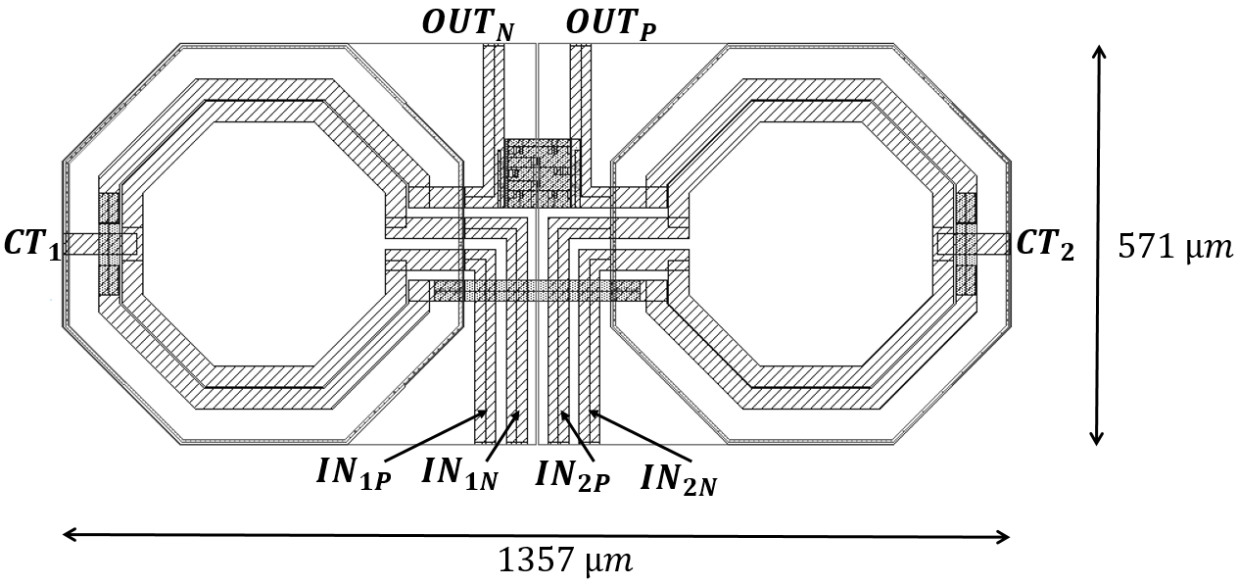


Source: The author.

The transformers performance is severely impacted by the technology high metal loss. There was a series of transformers designed before the tapeout, the presented version is the best one of those. After tapeout, it was seen that by reducing the winding distances to the minimum of 1.5 µm the G_{Max} can be improved around 0.1 dB to $G_{max} = -1.47dB$. On the other hand removing the thin-metal underpass on the secondary and making the primary center-tap on a thin metal layer does not improve the G_{Max} substantially.

The power combiner consists of two of the aforementioned transformers with their primaries independently driven and their secondaries connected in series as shown in the layout of figure 3.18. Because of the high output voltage and the low breakdown voltage of the technology capacitors, a custom-made output tuning capacitor was designed to tune the SCT output. This device is made of parallel metal layers with thick oxide for high dielectric breakdown voltage (on the order of hundreds of volts), it was Em-simulated and presented a value of 743.7 fF and behaves as a lumped component at least until 10GHz. The combiner structure does not have a G_{Max} defined because it is a 3-port network, but by connecting a dependant source in one of the inputs to simulate symmetrical driving it is possible to calculate as if it were a 2-port network by discounting 3dB at the output power. This G_{Max} can be seen in figure 3.19

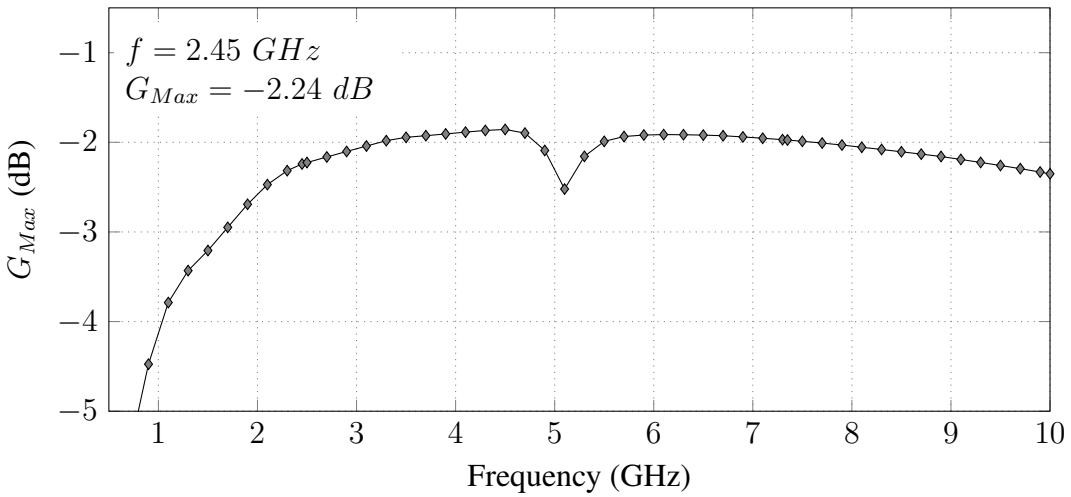
Figure 3.18: Series Combining Transformer



Source: The author.

A simulation was conducted with amplifiers driving the SCT, this simulation excludes the 2nd harmonic effects by using a tuned ideal LC filter at the second harmonic at each drain,

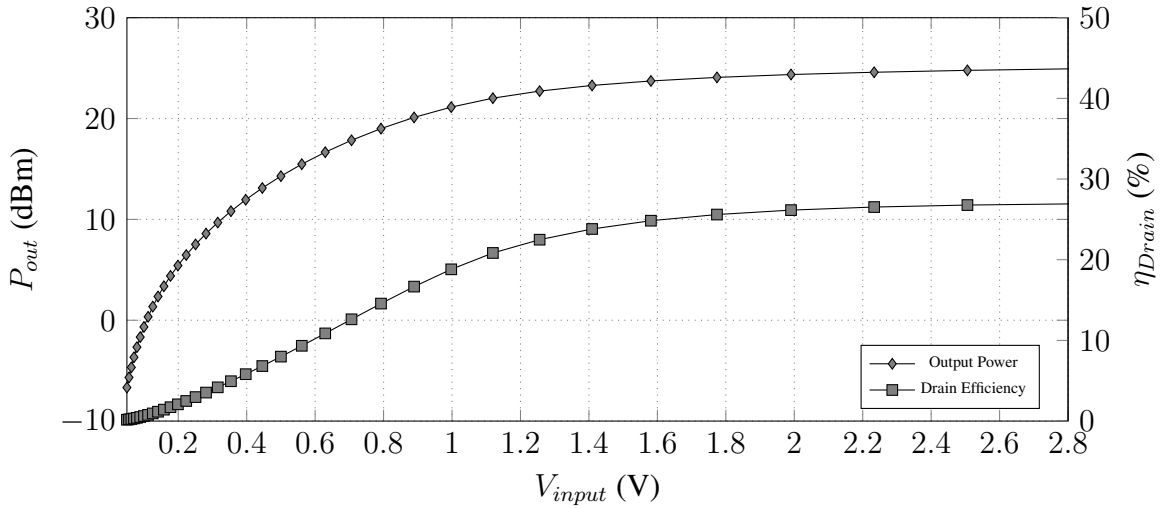
Figure 3.19: Series Combining Transformer G_{Max}.



Source: The author.

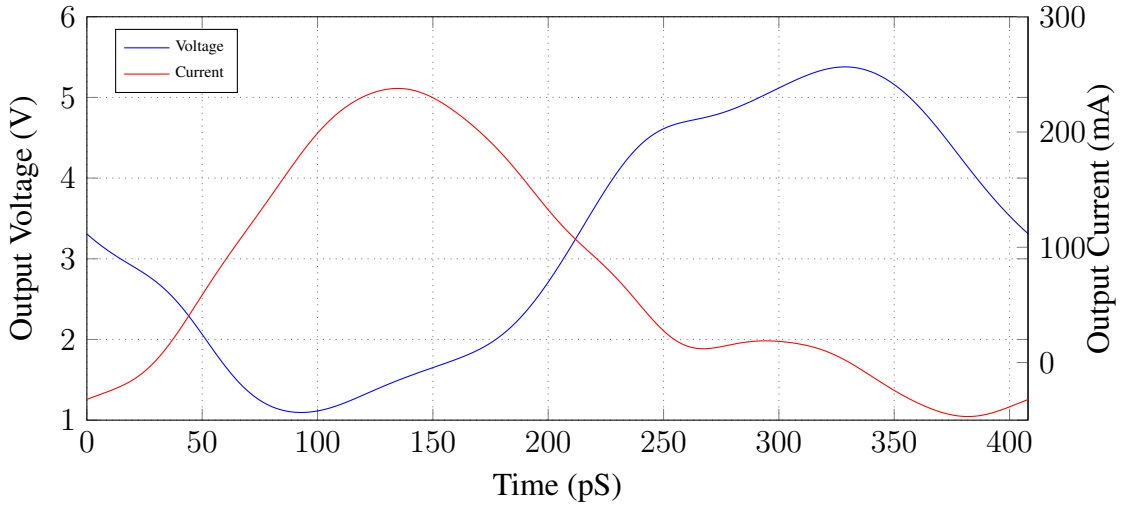
The results can be seen in figure 3.20. It is possible to see current and voltage waveforms for an input level of $V_{in} = 1.6\ V$ in figure 3.21. In this figure we can see that the fourth harmonic problem is smaller than before due to the bandwidth limitation from the transformers and active core layout. The voltage harmonics are: $V_1 = 2.08\ V$, $V_2 = 6.21\ mV$, $V_3 = 5.00\ mV$, $V_4 = 207.7\ mV$. The maximum output power is $24.93\ dBm$ with a drain efficiency of 26.92%. The insertion loss of this device .

Figure 3.20: PA results with extracted layout of active core, EM-simulated power combiner and ideal harmonic filter.



Source: The author.

Figure 3.21: Single-Ended branch current and voltage waveforms with ideal 2nd harmonic tuning.

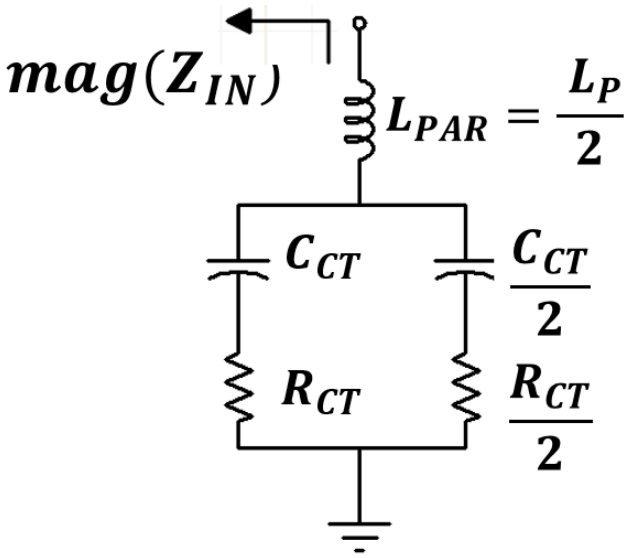


Source: The author.

Finally, The common-mode second harmonic tuning network is added, this network acts as a bypass capacitor that resonates with the leakage inductance of the primary of the transformers to form a low impedance at the second harmonic, connected to the differential AC ground on the active core. A small resistor is added in series with the capacitors to make the tuning more broadband, and to decrease the Q of the network, avoiding the possibilities of high Q resonances that can generate common mode instability, this have the downside of increased second harmonic impedance. This network is shown in figure 3.22 and the common mode impedance magnitude seen by each core amplifier is shown in figure 3.23. In this schematic L_{PAR} is the transformer parasitic inductance and is $L_{PAR} = 412\ pH$, the capacitance $C_{CT} = 4\ pF$ and $R_{CT} = 7.7\ \Omega$.

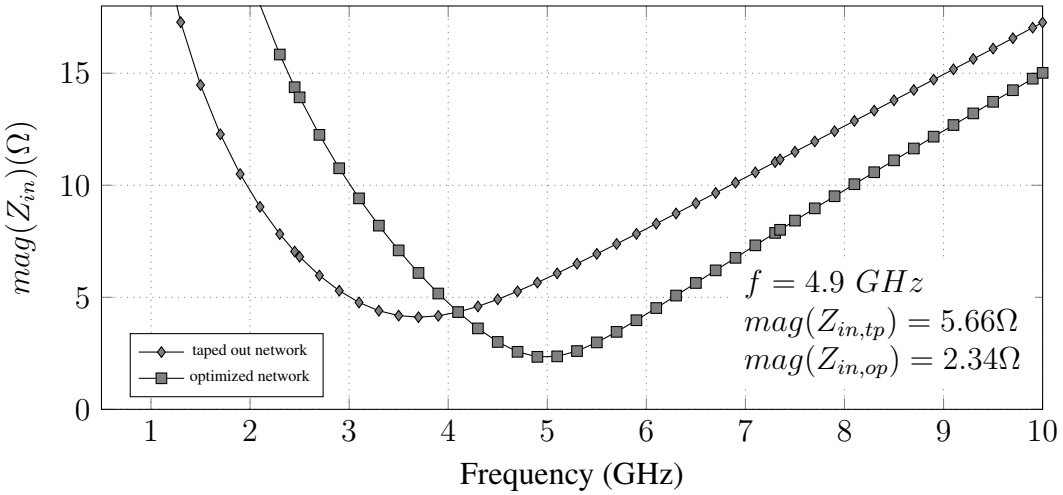
With the use of the real harmonic tuning network on the center tap of the amplifiers the voltage second harmonic content is greatly increased and the resulting waveform for the input voltage of $V_{in} = 1.6\ V$ can be seen in figure 3.25. The voltage second harmonic content rise to $V_2 = 967.1\ mV$ due to a non-ideal network. This poor result was due to a mistake in the electromagnetic (EM) simulation at the time, when the port setup was not calibrated to simulate coupling properly, that predicted an slightly off inductance for the transformer. The network was re-optimized after tapeout and the common mode impedance seen by the amplifier is shown in figure 3.23. The increase in second harmonic voltage causes the compression of the gain and smaller fundamental amplitude, which is $V_1 = 1.85\ V$, degrading output power

Figure 3.22: Common-mode second harmonic tuning network schematic



Source: The author.

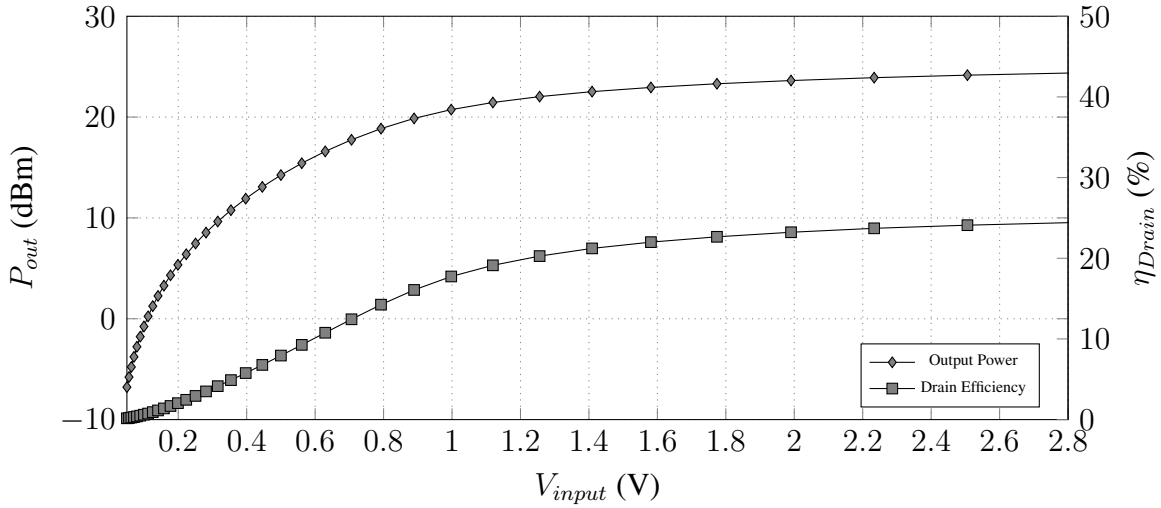
Figure 3.23: Common-mode impedance seen by each core amplifier.



Source: The author.

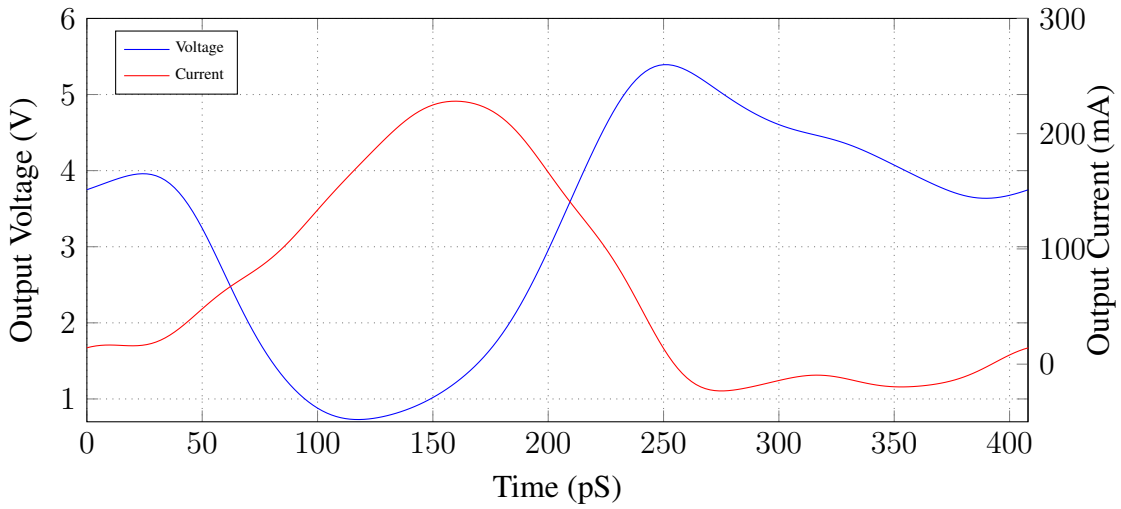
and efficiency as can be seen in 3.24. The third harmonic, responsible for spectral regrowth and EVM, has increased to $V_3 = 25.59\ mV$ but remain relatively low. The fourth harmonic also increases to $V_4 = 280.5\ mV$ due to the compression caused by the second harmonic. The maximum output power of the amplifier with this network is $24.4\ dBm$ and drain efficiency is $24.4\ \%$, which is as expected, worse than the previous results with an ideal network.

Figure 3.24: PA results with layout parasitics and harmonic tuning network.



Source: The author.

Figure 3.25: Single-Ended branch current and voltage waveforms with center-tap harmonic tuning.



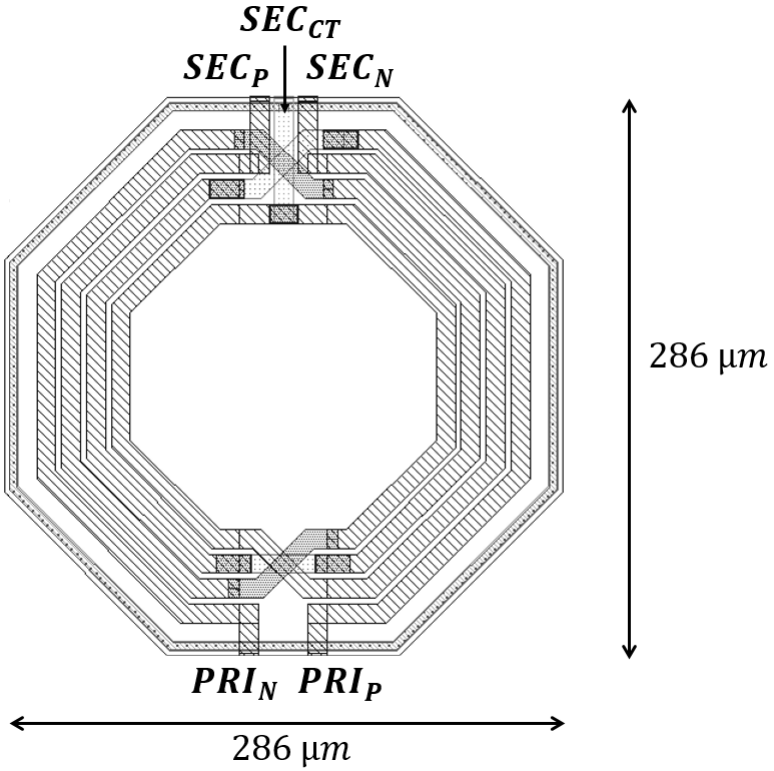
Source: The author.

3.5 Input matching

In order to measure the power gain and stability factor of the amplifier, and to make it easier to test the amplifier without the need to worry about high VSWR due to impedance mismatch, the amplifier input is to be reasonably matched. As this design is a single-stage PA, the transistors at the output stage are large and this makes the circuit have have a very high input capacitance, which makes the input matching dificult. The input matching network can be seen in figure 3.2. The network also acts as balun and signal splitter, supplying a differential signal

from the single-ended signal at the chips input, and guaranteeing that the amplitude voltage at the input of the two amplifiers close to equal by the parallel connection of the transformers. The input capacitance of each of the input transistors of the amplifier is $1.75\ pF$ and the AM-PM nonlinear compensation transistor has an input capacitance of $1.98\ pF$, which makes for an equivalent differential capacitance of $1.865\ pF$ for each amplifier core, and a total of $3.73\ pF$ of differential capacitance at the input of the PA. The topology used is a "inverted PCT", another alternative is an "inverse SCT", this would present a better match by connecting the transformers primaries in series, and thus seeing the low input impedance of the amplifiers in series with each other, but this topology have a downside of dividing the input voltage by two, reducing the gain of the amplifier much further, already low in a single-stage topology.

Figure 3.26: Input matching network transformer layout.

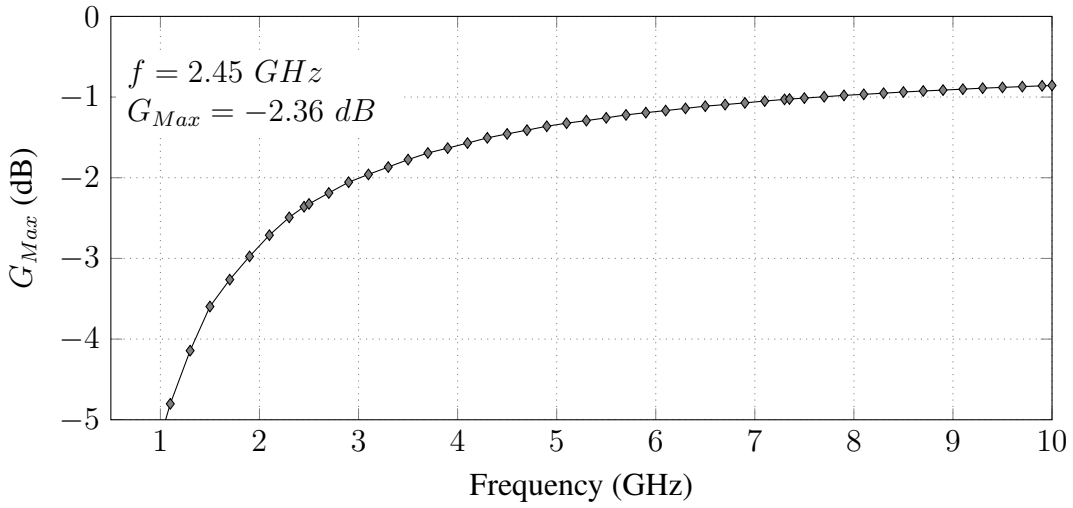


Source: The author.

Because area is much more of concern with these transformers and they are operating under a 100Ω environment, the transformer topology is moved to a two-spire primary and secondary, providing higher inductances for a smaller area at the cost of lower efficiency. The layout of this unity transformer in the input matching network can be seen in 3.26, the extracted narrow-band model parameters are: $L_P = 1.515\ nH$, $R_P = 5.83\ \Omega$, $L_S = 1.289\ nH$, $R_S =$

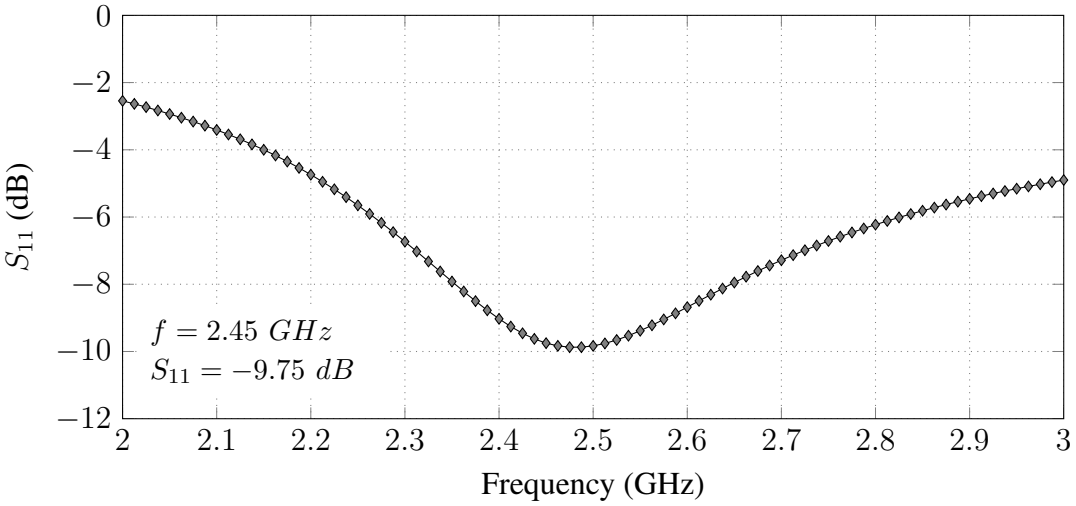
$3.39\,\Omega$ and $k = 0.75$. its Gmax can be seen in figure 3.27 and has a value of $G_{Max} = -2.36\,dB$ at $2.45\,GHz$. This loss is so high because of the low quality factors of the inductances, which are: $Q_P = 4.00$ and $Q_S = 5.89$, and this is because the technology only have one layer of thick metal and the transformer has two spires in both inductors to achieve a high inductance and coupling coefficient. Aditional mim capacitors were added to the amplifiers input for the match with values of $884fF$. The input impedance of the PA at $f = 2.45\,GHz$ is $Z_{in} = 26 + j8.56\,\Omega$. The input reflection coefficient S_{11} can be seen in 3.28.

Figure 3.27: Input transformer G_{Max}.



Source: The author.

Figure 3.28: Power Amplifier S_{11}.

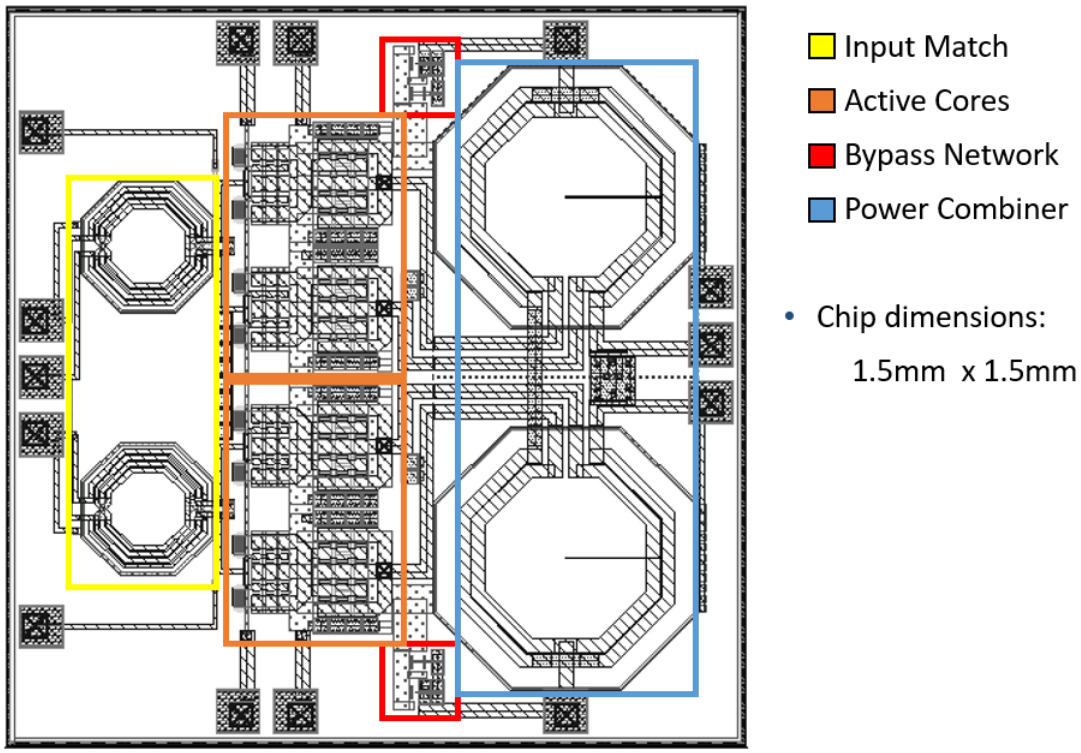


Source: The author.

3.6 Chip top level

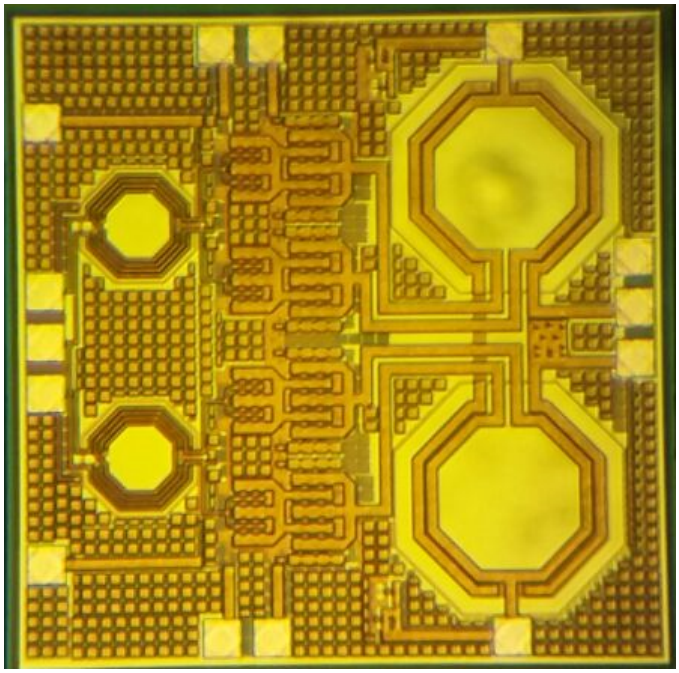
The top level layout without metal fill can be seen in figure 3.29. The pads are composed of a full metal stack with size 90 x 90 μm^2 without ESD protection. The GSG pads have 125 μm pitch. The layout tries to follow the proposed floorplan from 3.3 as much as possible. The bias signals are symmetric and the only pads that changed position from the predicted on the floorplan were the "Bias" pads that are in the left lateral of the chip due to layout issues and simplicity. The whole design process took three months, from February to April 2017. The chip photograph can be seen in 3.30. Metal fill was inserted manually and was kept away from the the internal area of the transformers so as to not degrade their Q. These areas do not comply to local metal density rules, but that is not a problem because no signal is routed or circuit is placed there.

Figure 3.29: Chip top level layout without metal fill.



Source: The author.

Figure 3.30: chip photograph.



Source: The author.

4 TEST SETUP

The PA went for tapeout on March 2017. It was known from the start that it wasn't going to be possible to test most of the performance parameters of the circuit such as Spectral Mask and EVM because the current UFRGS infrastructure lacks power meters, modulated signal sources and modulated signal analyzers in any particular standard. Despite that, it is possible to measure efficiency, S-Parameters and output power, as well as AM-AM and AM-PM nonlinearity with available equipments at lab110 at INF/UFRGS and LCE at Elétrica/UFRGS. The available equipment list on both labs is displayed in table 4.1.

Table 4.1: Available instruments

Location	Function	Manufacturer/ID	Description
LAB110/INF	Spectrum analyzer	Agilent N1996A	BW 100 kHz - 3 GHz
LAB110/INF	RF signal generator	Agilent N9310A	BW 100 kHz - 3 GHz
LAB110/INF	Waveform generator	Agilent 33250A	BW: 80 MHz / 12-bit, 200 MSa/s
LAB110/INF	Osciloscope	Agilent MSO6102A	BW:1 GHz / 4 GSa/s
LCE/Elétrica	Microprobing Station	Cascade EP6 Station	Up to 6 positioners
LCE/Elétrica	2 x GSG RF Probes	Cascade Infinity Probe	BW: DC - 40 GHz
LCE/Elétrica	Spectrum Analyser	Rhode&Schwarts FS300	BW 9kHz - 3 GHz
LCE/Elétrica	RF Signal Generator	Agilent N9310A	BW 100 kHz - 3 GHz
LCE/Elétrica	VNA	Rhode&Schwarts ZVL6	BW 9 kHz - 6 GHz

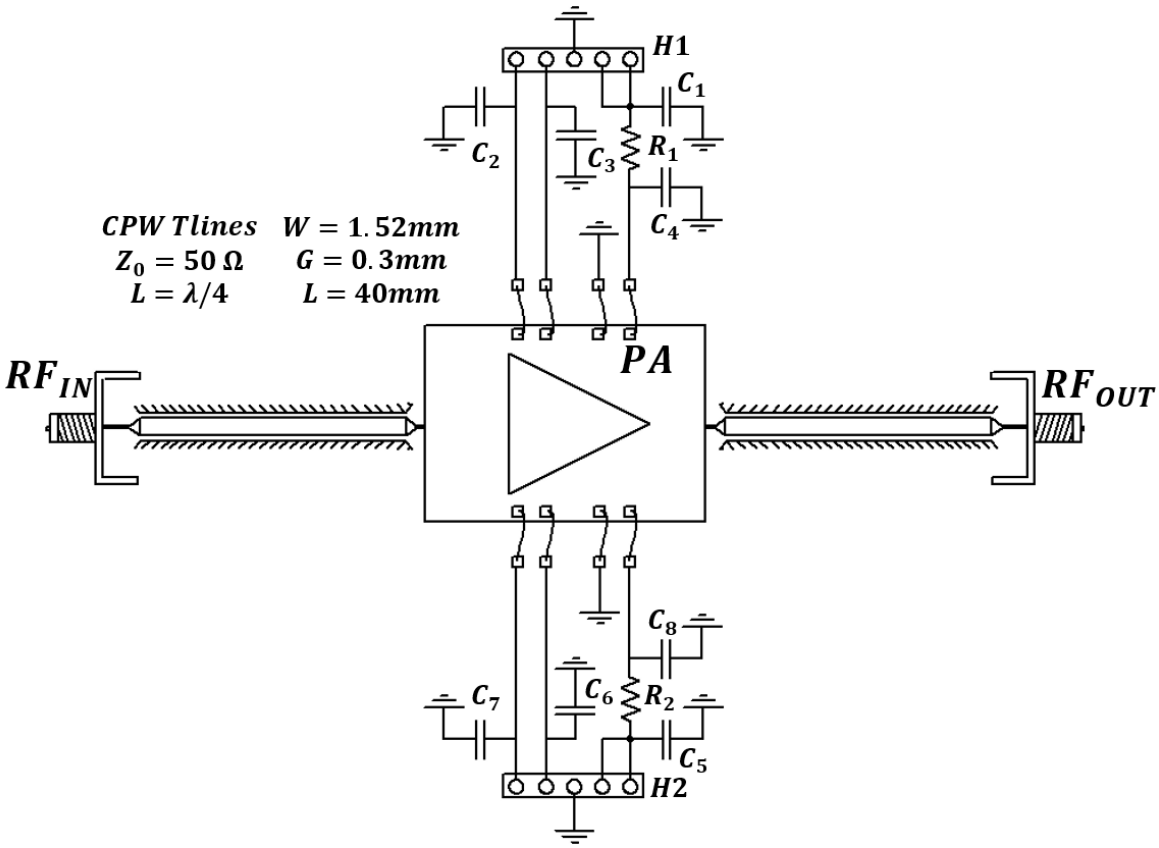
Because of the existence of GSG RF probes and a Cascade microprobing station, the amplifier is supposed to be measured in a hybrid fashion: The bias pads would be connected through bondwires to a PCB while RF signals would be sourced and sinked by these microprobes to eliminate the effect of bondwire parasitics in these paths. There was a total of forty chip samples to be divided in these two configurations. Due to the high cost of low parasitics RF packaging such as Quad-Flat no leads (QFN), all of the samples were ordered bare dies. Because a Fire-Resistant class-4 substrate (FR4) PCB must be designed for the DC signals, a decision was made to include RF transmission lines on the PCB to edge Sub Miniature version A (SMA) Connectors, this allows two different chip-on-boards to be made: One high performance configuration to be measured with microprobes as stated above, and another that connects the RF signals to the board for easy of measurement that does not need microprobes.

4.1 RF PCB design and wirebonding

The proposed board was designed as a double layer FR4 board, where the bottom layer is a ground plane. The design focused on the bypass of the DC signals and is symmetrical as is the chip (these signals are supposed to be connected on the supply). The bypass networks and devices were based off on demonstration boards from power amplifiers of the same frequency and power class from Avago Technologies.

The board schematics is shown in figure 4.1. The components are described in table 4.2.

Figure 4.1: PCB Schematics.



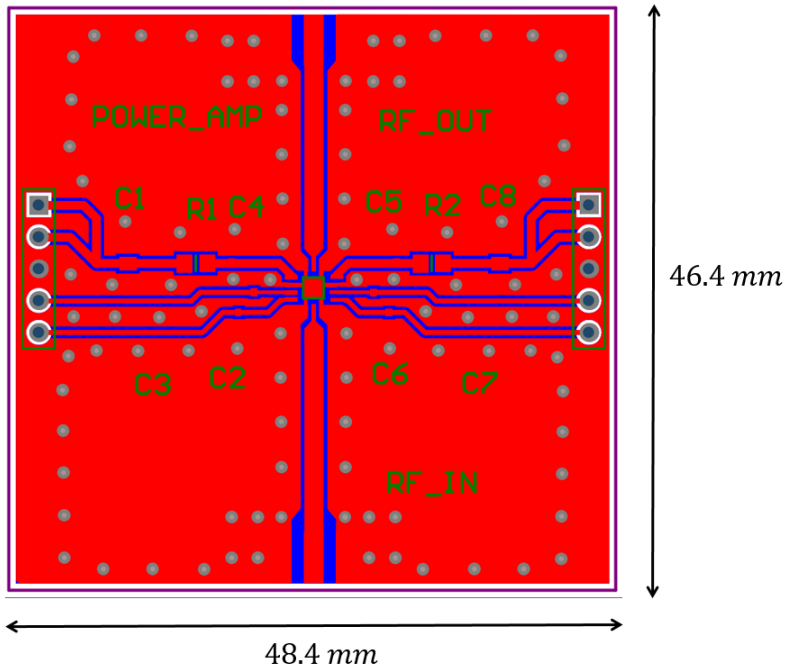
Source: The author.

The board layout can be seen in Figure 4.2. RF layout techniques such as via fencing were utilized. The PCB was fabricated in July 2017.The photo of the fabricated PCB can be seen in 4.3. The PCBs had their surface-mount devices (SMD) components assembled in-house to prepare the boards for the die attach and wirebonding.

Table 4.2: PCB BOM

Label	Description	Package	Suplier	Price (US$)
$C_{1,8}$	2.2µF Ceramic capacitor	0805	Murata	0.1900
$C_{4,5}$	0.1µF Ceramic capacitor	0402	Murata	0.0062
$C_{2,3,6,7}$	82pF Ceramic capacitor	0402	Murata	0.0087
$R_{1,2}$	0.0 Ω thick-film resistor	0805	Yageo	0.0071
$RF_{in,out}$	SMA edge connector	-	Taoglas Limited	3.2200
$H_{1,2}$	5-pin female header	-	Sullins	0.6200

Figure 4.2: PCB Layout.

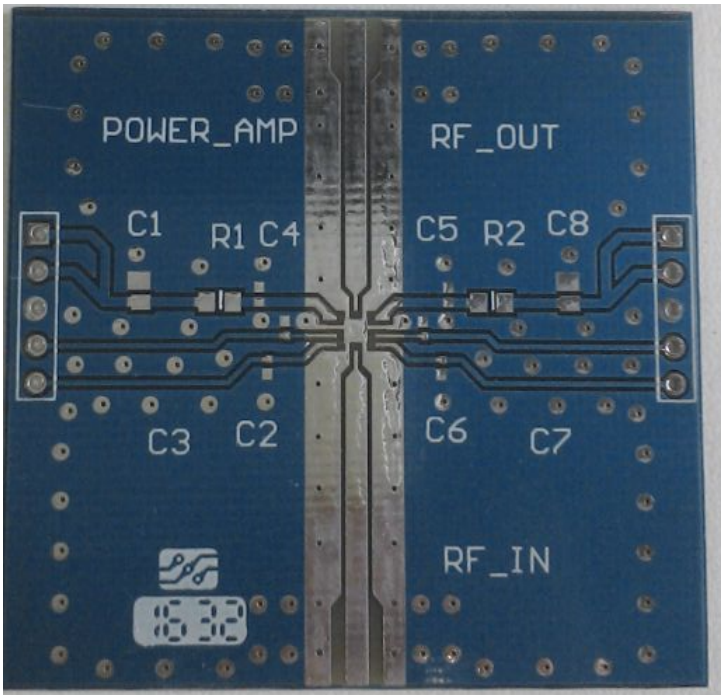


Source: The author.

4.1.1 Wirebonding

There is no working wirebonder at UFRGS and the work suffered from the lack of know-how on Chip-on-board. The physics group at UFSC put a wirebonder (ball-bonder) at the disposal for this work. The Chip-on-board was done with the help of a post-Doctoral researcher. There was no epoxy adhesive for the die attach so the dies were attached to the board using a common cyanoacrylate glue (superglue), which is non-conductive and thus negatively affect the behaviour of the circuits transformers such as increasing their loss. This glue also have different mechanical properties than the ideal adhesive. Nevertheless, the main problem was that the manufactured PCB had a Hot Air Solder Leveling (HASL) finish, which has a common tin solder coating. This makes nearly impossible to bond the gold wires of the machine to the board and makes highly probable that the bond will either have no electrical contact or will be

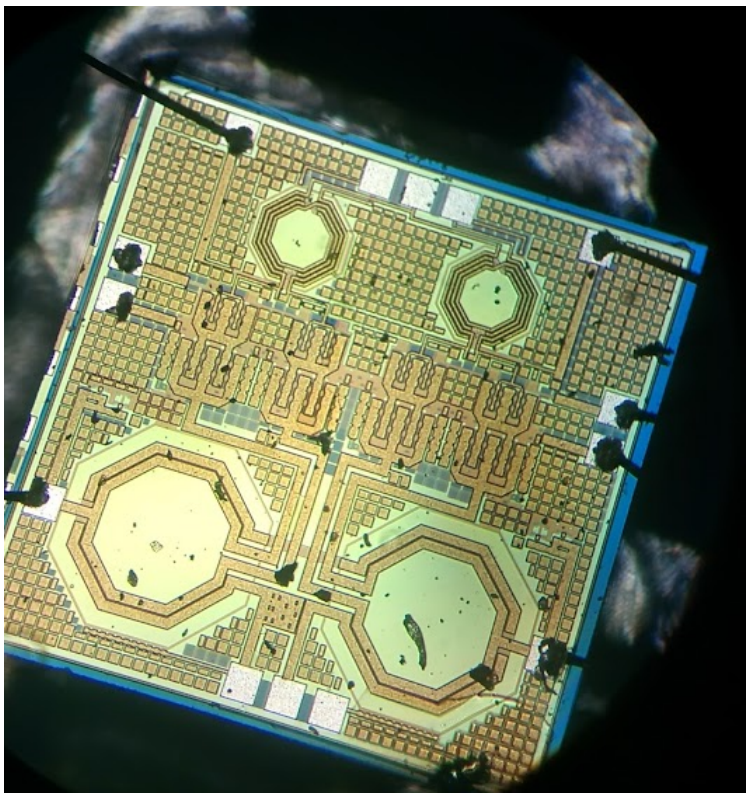
Figure 4.3: PCB photograph.



Source: The author.

a high resistivity contact. For the use of gold wires the PCB should be either gold-platted or has a Electroless Nickel Immersion Gold (ENIG) surface finish. This was not known at the time and only two boards were finished for GSG probing. Both PCBs had some bonds that later disconnected due to some mechanical stress, probably in transport. This fact made the measurement not viable in the available time-span. A photo of one of the chip with bonds that lifted off and damage by transport can be seen in figure 4.4, a large amount of dust also can be seen in the photo.

Figure 4.4: chip with lifted off bonds and damage by transport.



Source: The author.

5 SIMULATION RESULTS

In this chapter the final simulation results of the amplifier are presented, with emphasis on its performance under the 802.11g standard as proposed in section 3.1. The simulation setup had the active core as a RC extracted layout while passives were EM simulated with Keysight momentum 2.5D EM simulator for their S-parameters models up to 10GHz and with fine mesh of 100 cells/wavelength. The setup also predicts the impact of bondwires in the supply and bias pads. The circuit was simulated in Cadence Virtuoso tools suite with the spectre RF engine. For large-signal and non-linear simulations a Harmonic Balance simulation with a large number of harmonics was used. The amplifier bias condition during these simulations is described in table 5.1.

Voltage	Value
V_{DD}	3.3 V
V_{bias}	750 mV
V_{bcap}	1.08 V
$L_{bondwire}$	529 pH
T	27 ^oC

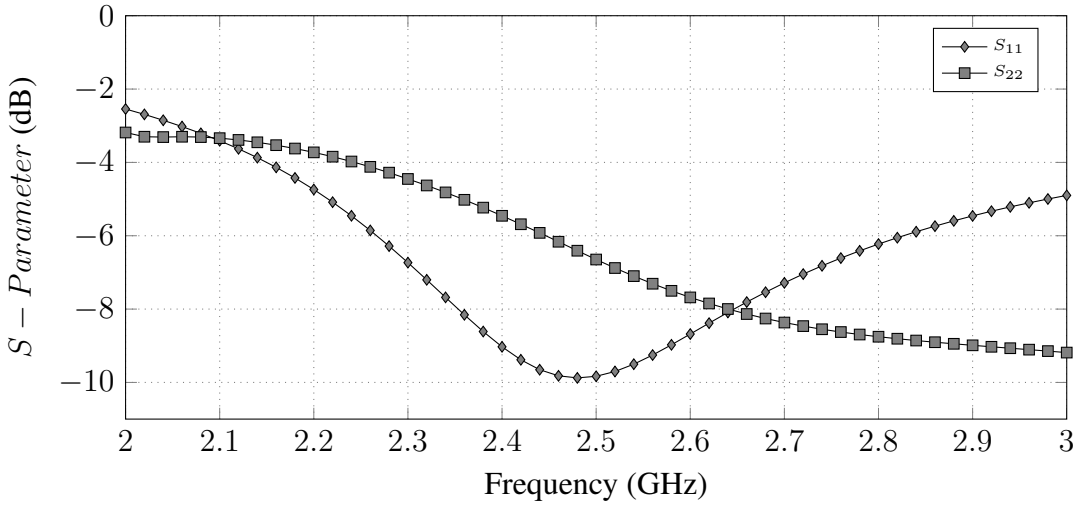
Table 5.1: Amplifier bias condition and bondwire parasitics for final simulations.

The bias voltage is different from the one of the design analysis because this circuit parameter was re-optimized once the design was finished by taking into account efficiency, output power, linearity and gain. The gain of the amplifier was too low after matching - around $6\ dB$ at maximum PAE - and that would make the circuit hard to measure, because it would need a highly linear high power source to fully saturate the amplifier, and these simulations were intended to be confronted with measured data. This is the reason why the bias voltage of the active cores were increased to $V_{bias} = 750\ mV$ as a way of increasing the power gain and being a new optimal point for the operation of the amplifier. The bondwire value is the average inductance of a QFN14 package with 1.5 mm x 1.5 mm cavity (TEXAS INSTRUMENTS, 2004). Temperature effects such as self-heating were not simulated but can be predicted by making a thermal model with package, junction and board thermal resistances.

5.1 Stability and Match

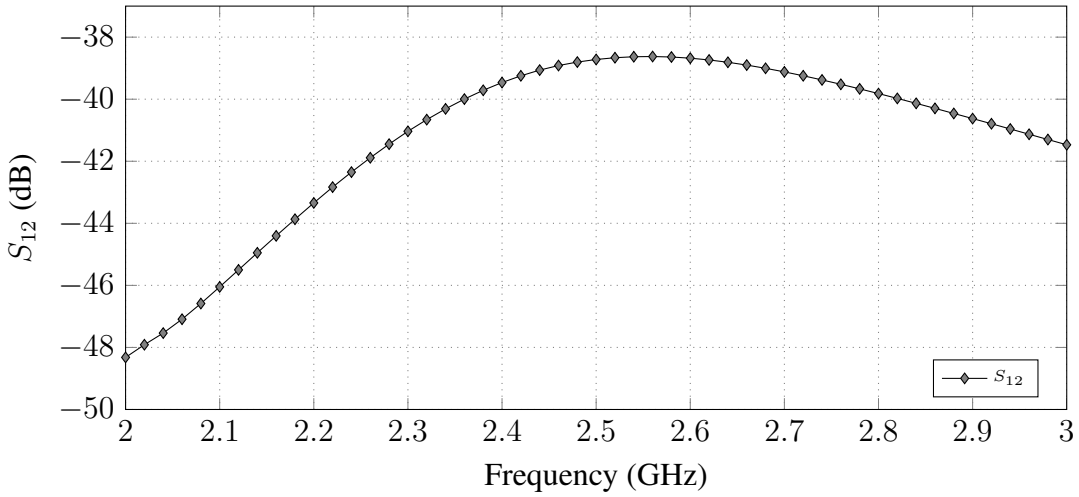
As seen in section 3.5, the PA has its input reasonably matched for a $50\ \Omega$ impedance. The PA S-Parameters can be seen in figures 5.1, 5.2 and 5.3. In the $2.4\ GHz$ ISM frequency range ($f = 2.4\ GHz$ to $f = 2.5\ GHz$) the input match is better than $-9.02\ dB$, the amplifier small-signal gain is higher than $15.8\ dB$ with $0.1\ dB$ variation and the isolation is higher than $38.7\ dB$.

Figure 5.1: Power Amplifier input and output matching.



Source: The author.

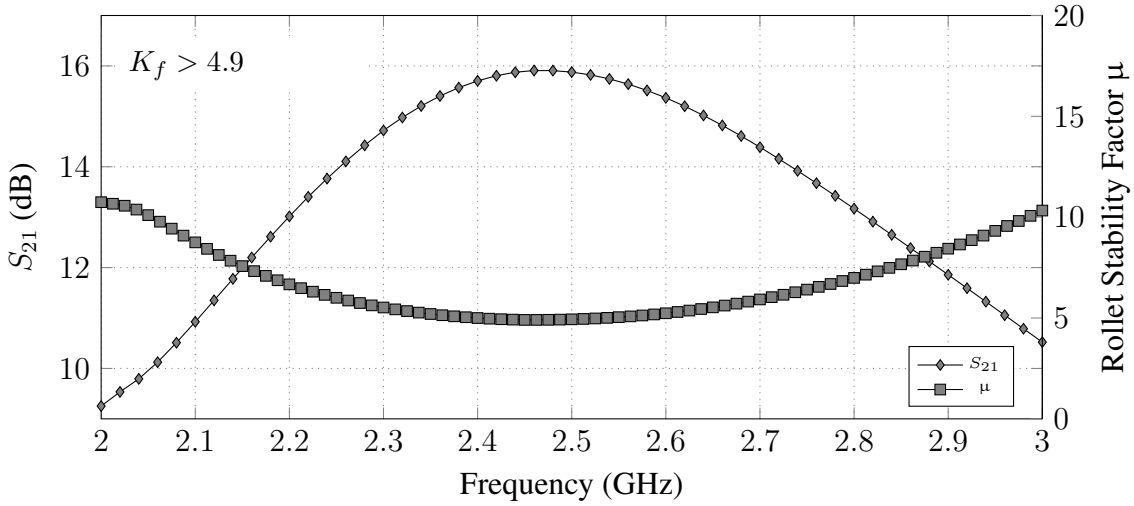
Figure 5.2: Power Amplifier isolation.



Source: The author.

Another important aspect that can be evaluated from the S-parameters is the amplifier stability, the differential gain and differential-mode Rollet stability factor can be seen in 5.3. This figure and gain was simulated for a wideband where the amplifier has considerable gain and it is much larger than 1 outside the shown range of 2-3 GHz. The factor μ minimum value is 4.9 at $f = 2.45\ GHz$.

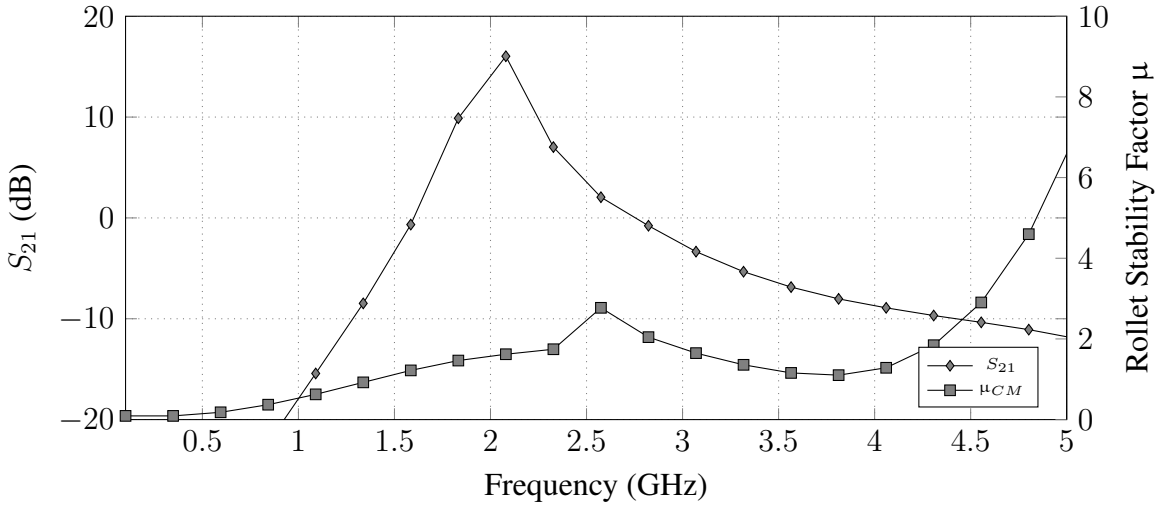
Figure 5.3: Power Amplifier S_{21} and Stability factor.



Source: The author.

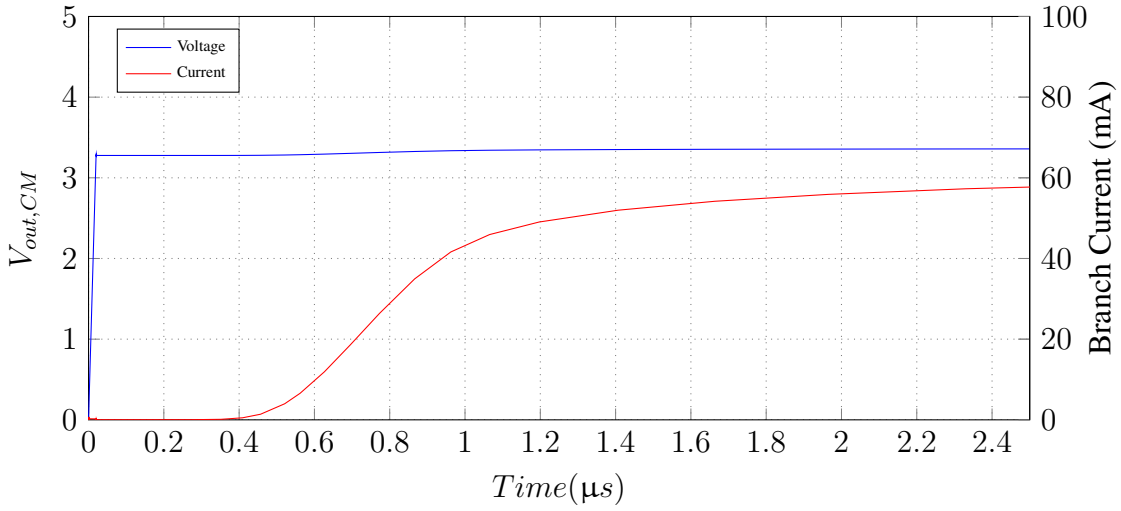
The common-mode stability factor was measured by inserting ports at common-mode bias points internal to the circuit, at transformers center taps. The amplifier is barely unconditionally stable at its internal common-mode as can be seen in 5.4, at the interval that the common mode gain is higher than $0dB$: from $1.6\ GHz$ to $2.75\ GHz$ we have $\mu_{CM} \geq 1.23$ which is very close to 1. Bellow that frequency k_{CM} value dips bellow 1 at $1.4GHz$ where the S_{21} has fallen to $-6.6\ dB$. A issue to point out is the dependence of the S_{21} on the port impedance, as the simulation setup was not made to measure the stability and gain of internal parts of the circuit. Under these conditions a transient simulation was realized to guarantee common-mode stability under the real circuit conditions, a step was introduced in the supply voltage and a long time of $2.5\ \mu s$ with fine time step was simulated to make sure that there are no low-frequency oscillations. The resulting common-mode voltage at the output and amplifier branch current can be seen in 5.5, and one can see that there are no ringings in the current, which indicate good stability.

Figure 5.4: Power Amplifier common-mode gain S_{21} and common-mode stability factor.



Source: The author.

Figure 5.5: PA turn-on to ensure common-mode stability.



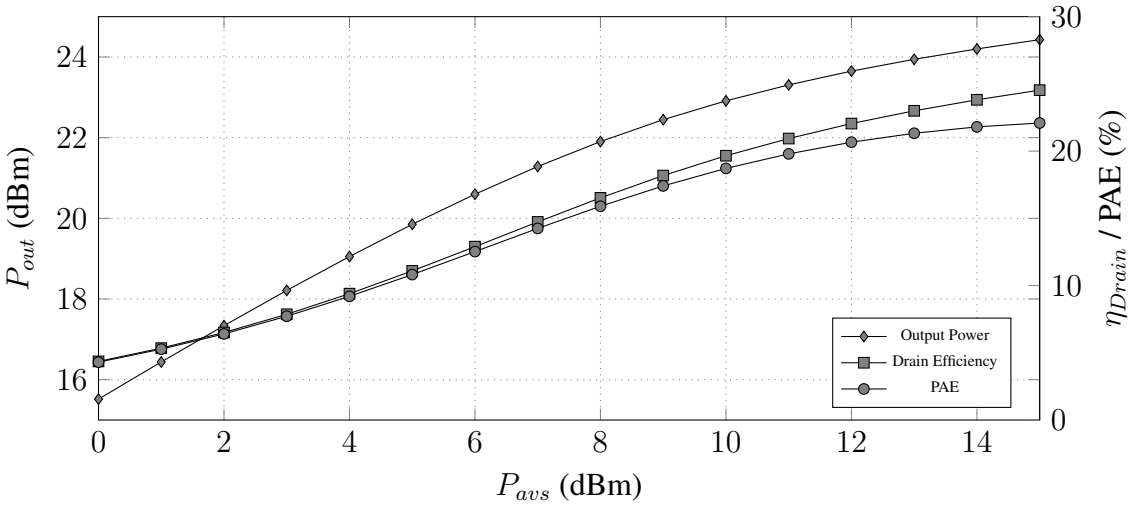
Source: The author.

5.2 Large signal behaviour

The final output power, drain efficiency and PAE as a function of source available power P_{avs} curves are seen in 5.6. The maximum output power is $24.43\ dBm$, the maximum drain efficiency is 24.53% with a PAE of 22% for a available power of $15\ dBm$, which is already high, here it becomes evident why the amplifier bias had to be increased in order to keep the gain around $10\ dB$ when compressed at the saturated output power. This compression behaviour can be seen in the power gain curve in 5.7. the operating power gain ranges from $16.05\ dB$ to $10.23\ dB$, the input referred 1dB compression point is $P1dB = 5.2\ dBm$ while the output

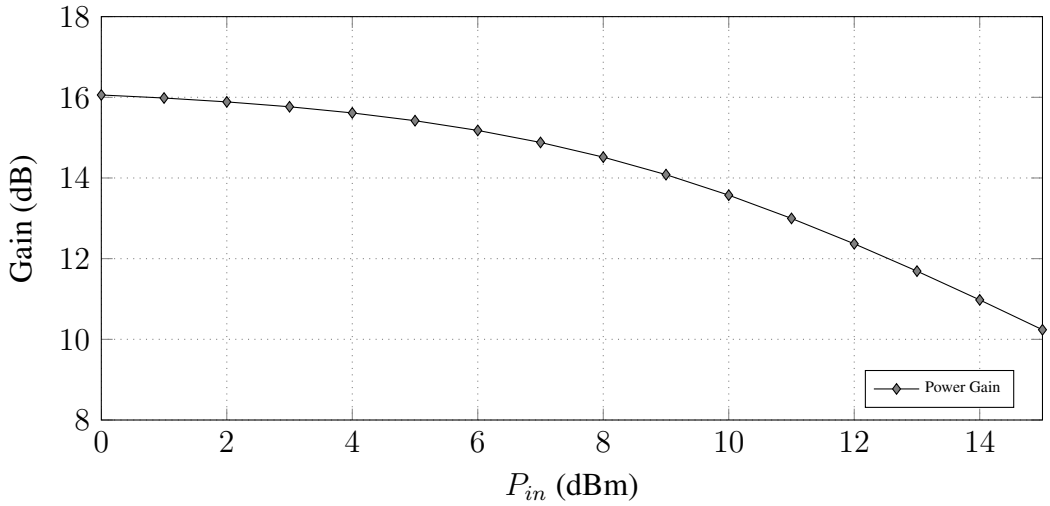
referred is $OP1dB = 20.03\ dBm$. The discrepancy between the calculated gain and the difference of output power and available power is due to two different definitions of power gain: transducer power gain that at the maximum PAE point is $9.53\ dB$ and operating power gain that is $10.23\ dB$.

Figure 5.6: PA simulation results.



Source: The author.

Figure 5.7: PA results with layout parasitics and harmonic tuning network.

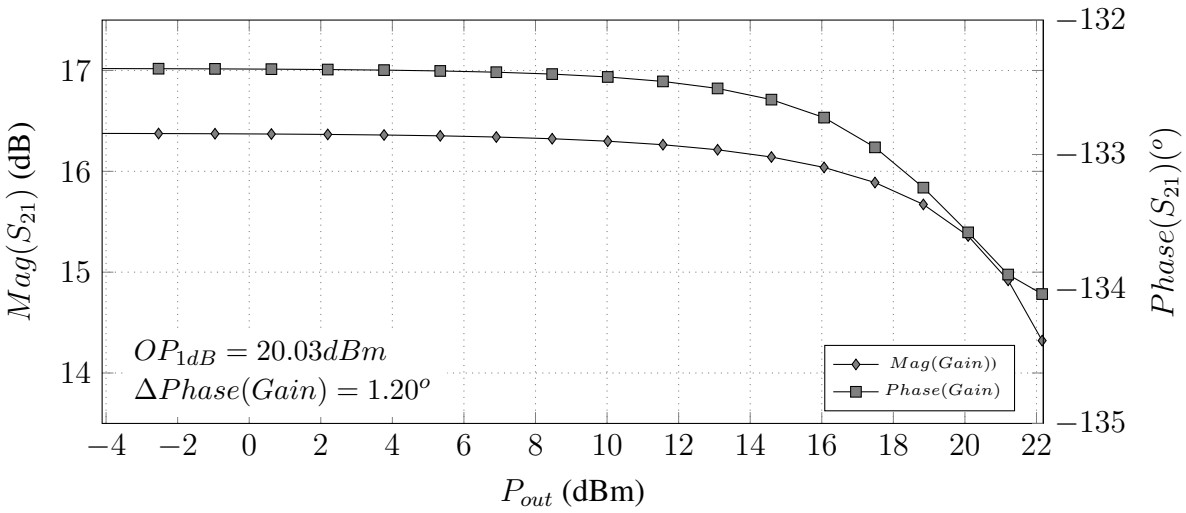


Source: The author.

5.3 General non-linearity measurements

There are many general measures of non-linearity, one of which is based on the approximation of the amplifier as a quasi-static non-linear system where the output signal power and phases are dependant on the input power, this is called "AM-AM" and "AM-PM" non-linearities. The output referred AM-AM and AM-PM curves of the amplifier can be seen in 5.8. The output-referred $1\ dB$ compression point is $OP_{1dB} = 20.03\ dBm$ and the difference in phase shift up to this power is $\Delta Phase(Gain) = 1.2^o$.

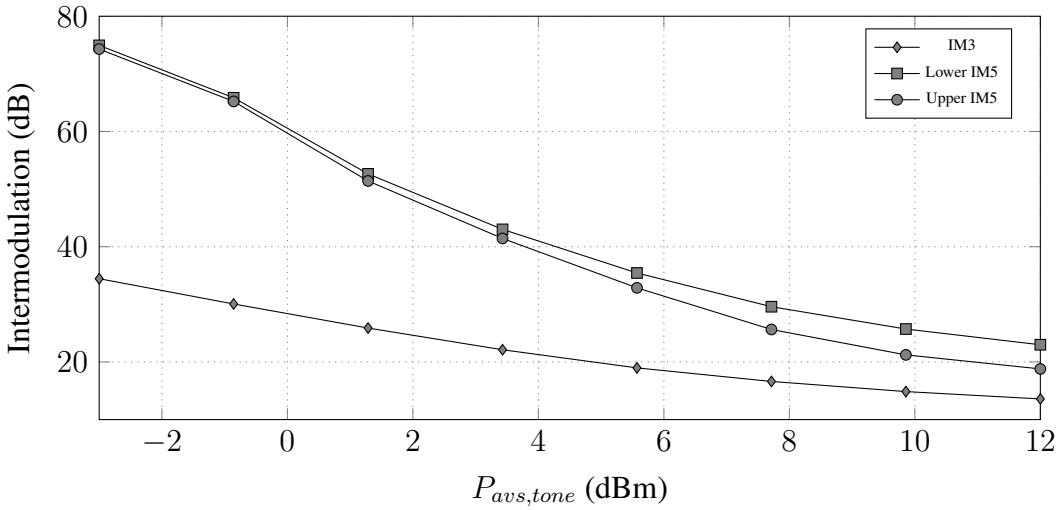
Figure 5.8: PA output referred AM-AM and AM-PM distortion.



Source: The author.

Another type of general measure of non-linearity that is useful in PA design is odd-harmonic intermodulation like IM3 - which is the ratio between the third order intermodulation product and the fundamental at the output of the amplifier - and IM5 - which is similarly defined but for the fifth order intermodulation product - as these are responsible for channel regrowth and self-corruption that causes EVM to rise. Both these tests are two-tones test that measure the amplitude difference between the fundamentals and the intermodulation distortion as a function of output power. For the tests two-tones were used with a $1\ MHz$ spacing between them, their frequencies are $f_{lower} = 2411.5\ MHz$ and $f_{higher} = 2412.5\ MHz$, both inside the frequency range of the first 802.11g channel. IM3 and IM5 curves can be seen in 5.9. The PA IM3 is symmetrical to $0.5\ dB$ so only one of these intermodulation products is shown, while both IM5 products are shown individually. The IM3 at $3\ dB$ back-off from the compression point is $24.22\ dB$, The lower IM5 is $48.16dB$ and the upper IM5 is $49.8\ dB$.

Figure 5.9: PA intermodulation results.



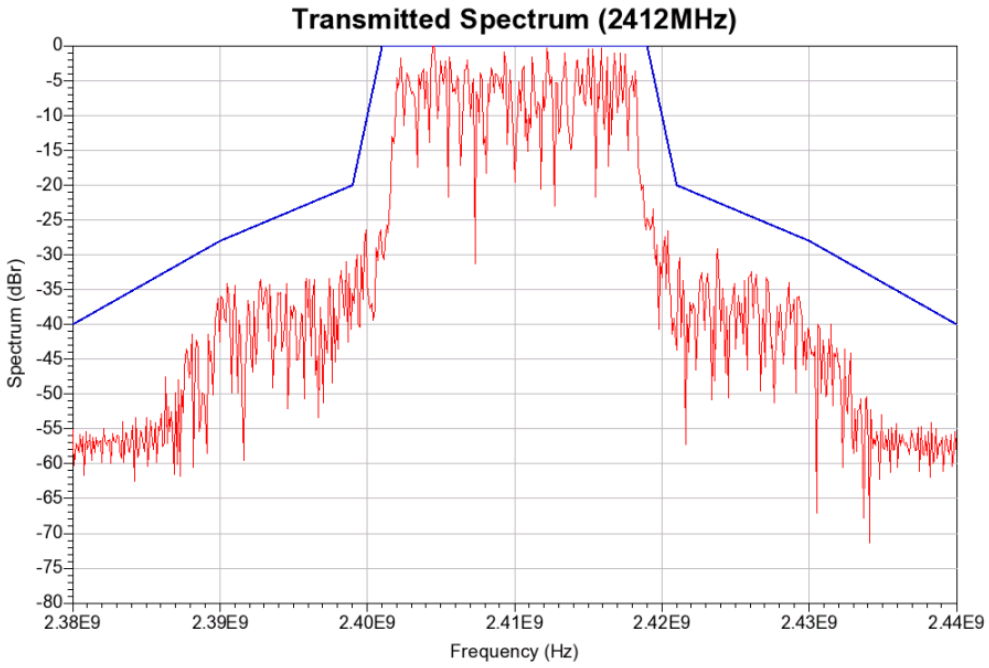
Source: The author.

5.4 Application: WLAN 802.11g signal amplification

Finally the PA is fed with an OFDM 54Mbps 802.11g signal in an envelope simulation to measure its performance under this WLAN standard, for this a standard 802.11a/g signal source in ADS keysight is used in a EVM pre-configured testbench. The reason for choosing the 54Mbps bitrate is because it is the most strict in terms of the PAs performance and thus, if the PA be compliant with the linearity requirements at that rate, it also satisfies them at lower rates, which have simpler modulation schemes and more redundancy on the forward error correction (FEC). No Analog or Digital pre-distortion or post-distortion techniques were used to improve the PA linearity.

The necessary EVM for demodulation of the signal is 5.6% or $-25\ dBm$. The amplifier achieves this EVM value with an average output power of $P_{avg} = 15.4\ dBm$. At the same time the amplifier satisfies the output masks with an output power of up to $P_{avg} = 19.5\ dBm$. This shows that the amplifier output power is limited by the EVM and not the output mask. In figure 5.10 it is possible to see the output spectrum and mask of the first channel of the band with center frequency of $f = 2412\ MHz$ and with a output power of $P_{avg} = 15.4\ dBm$. Another spectrum can be seen in 5.11 for channel number 14 with center frequency of $f = 2484\ MHz$ and an output power of $P_{avg} = 15.4\ dBm$. In figure 5.12 it is possible to see the amplifier output

Figure 5.10: Output spectrum and mask for 802.11g 2412 MHz channel.



Source: The author.

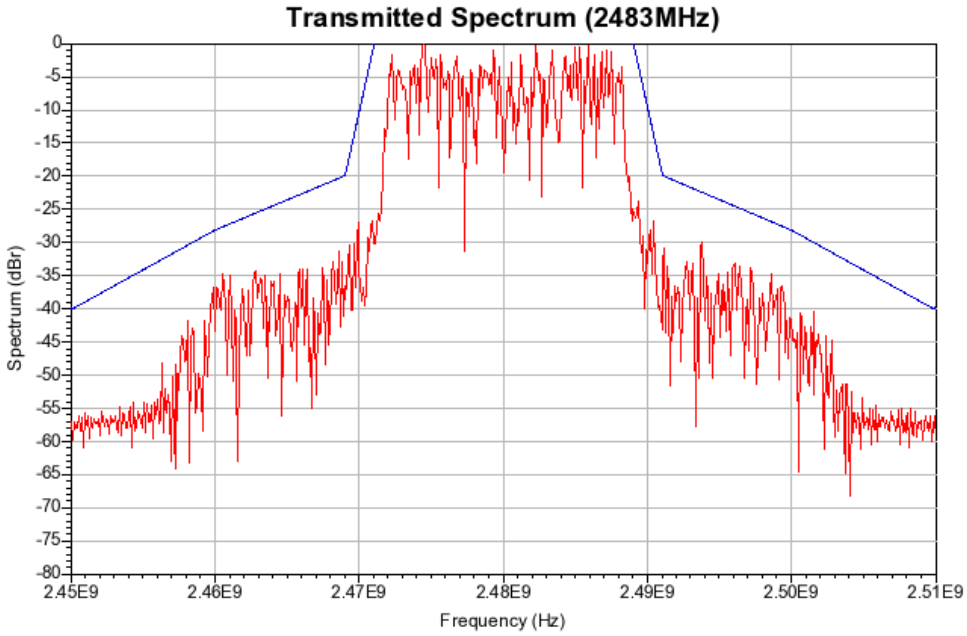
constellation with an output power of $P_{avg} = 15.4\ dBm$ in the channel with center frequency of $f = 2412\ MHz$. This constellation has an EVM of 5.43% or $-25.3\ dB$.

5.5 Comparison with state-of-the-art

Table 5.2 summarizes and compares the PA performance to the state-of-the-art of CMOS PAs. These particular works were chosen to make the table diverse in terms of technology, standard and other performances that are part of PA design trade-offs.

The amplifier in (CHOWDHURY et al., 2009) is the one closest to our own design, it uses the same supply voltage and works in the same frequency band, and this work has the same SCT topology, although that PA was implemented in a 90nm technology and it is a two-stage amplifier with $2.1x2.06\ mm^2$ chip area. The difference in performance is around $5.6\ dB$ in saturated output power and $7.3\ dB$ in average output power for a very similar standard, a 1024 carrier OFDM 64-QAM signal, although with a bandwidth that is $10\ MHz$, half that of 802.11g. The maximum PAE of that work is 33.1% against our 22%.

Figure 5.11: Output spectrum and mask for 802.11g 2483 MHz channel.



Source: The author.

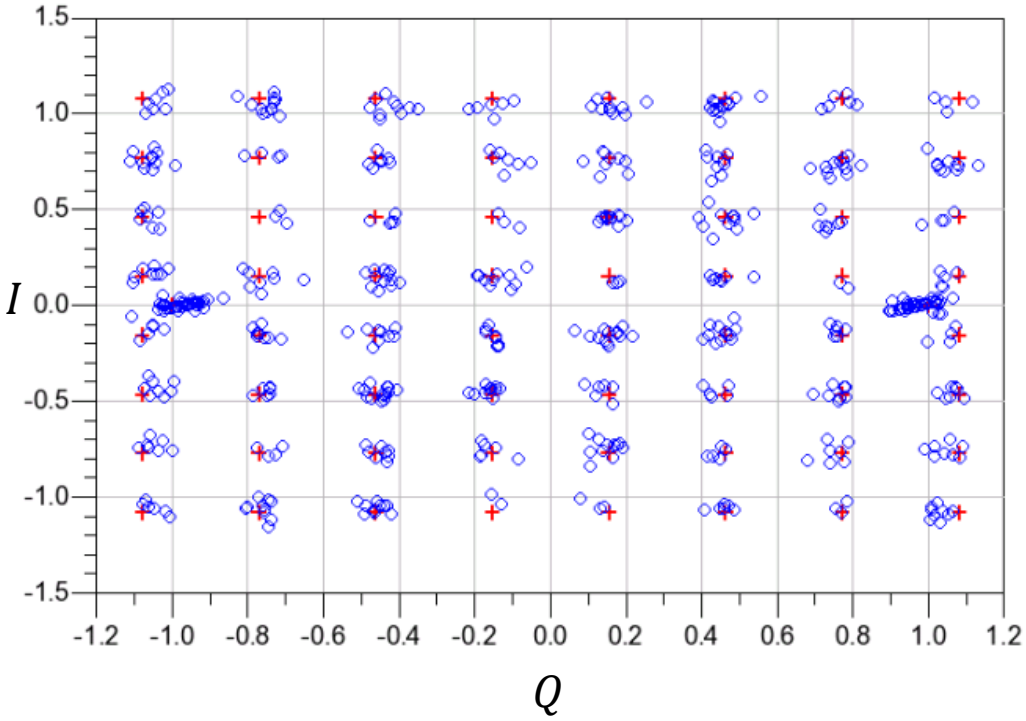
Table 5.2: Comparison between our work and recent linear CMOS power amplifiers.

(+) experimental; (*) simulation	This work*	[1]+	[2]+	[3]	[4]+	Unit
Technology	180	90	40	90	130	nm
Supply Voltage	3.3	3.3	1.5	1	3.3	V
Frequency	2.4	2.4	1.9	5.8	2.4	GHz
P_{SAT}	24.4	30	28	24.3	31.6	dBm
Modulation	802.11g	WiMax	LTE10M 16QAM	-	LTE10M 16QAM	
P_{avg}	15.4	22.7	23.4	-	27	dBm
EVM	-25	-25	-23	-	-32.9	dB
$(*)PAE; (+)\eta$	22* / 24.53+	33.1*	34*	27+	39.6*	%
Chip Area	1.57x1.57	2.1x2.06	2.1x1.4	0.9x0.9	0.8x0.8	mm^2
Load Impedance Transformation	On-Chip	On-Chip	On-Chip	On-Chip	Off-Chip	

[1] - (CHOWDHURY et al., 2009)
[2] - (KAYMAKSUT; REYNAERT, 2014)
[3] - (HALDI et al., 2008)
[4] - (AREF; NEGRA; KHAN, 2015)

The explanation for this great difference in performance is two main factors: The passives in this technology have a much higher insertion loss, in annex A the author showcase $1:1$ transformers designed in a 130nm technology with 2 thick-metal layers with lower resistivity than the 180nm technology used for the PA. The passives present much lower insertion loss

Figure 5.12: Output constellation for 802.11g 2412 MHz channel.



Source: The author.

and thus, higher efficiency. The use of such passives would increase both the output power and the efficiency of the impedance conversion network, having a double impact on the overall PA efficiency. Another factor that impacted both the output power and efficiency is the low power gain of the devices in this technology and single-stage characteristic of the PA. The PA require a large input voltage to generate the necessary output current, increasing the knee voltage of the devices and saturating them with a lower output voltage swing.

The work in (KAYMAKSUT; REYNAERT, 2014) is for a $10\ MHz$ 16-QAM LTE standard in the $1.9\ GHz$ frequency range, it is done in a 40nm technology. It is a two-stage design that achieves $P_{SAT} = 28\ dBm$ and $P_{avg} = 23.4\ dBm$ at $-23dB$ EVM. (AREF; NEGRA; KHAN, 2015) has the highest average output power and lower EVM, as well as highest PAE. But this is achieved with an off-chip impedance transformation networks, this work is in the table just to present the difference in performance of fully-integrated PAs and not fully-integrated, showcasing the dependence of the circuits on high quality factor networks.

Finally the work in (HALDI et al., 2008) was the first amplifier integrated with a spiral-transformer SCT and is a single-stage amplifier like the one presented in this work, it combines

four amplifiers in a $5.8\ GHz$ SCT for a maximum output power of $24.3\ dBm$, which is slightly lower than our own, although it is measured, so it is expected to be a little higher than our output power in the measured circuit. The drain efficiency is 27% against our 24.53%, the reason for using drain efficiency and not PAE is because that design does not have an input matched to $50\ \Omega$ and thus power gain could not be calculated. The PA in that work failed to support a modulated signal and has what the author called a supply-voltage modulation problem which is due to the lack of second-harmonic termination.

So this work would fit right between (HALDI et al., 2008) and (CHOWDHURY et al., 2009), it has input match and can support a highly linear standard, although its efficiency is sub-par, mainly because of the technology but also because of some design issues that were described in 3.

6 CONCLUSIONS

This thesis presented the development of a fully integrated RF Power amplifier for a communication standards that require high linearity in 180nm CMOS technology. The design process involved the analysis of the challenges in integrating a high-frequency, high-power circuit in a technology with low supply voltage and lossy passives. The solution that recent work have converged to is power combining networks. Following this trend a series combining transformer was designed and optimized in the technology with the help of a 2.5D electromagnetic simulator. The PA makes extensive use of AC grounds to make itself robust against supply voltage and ground bondwire parasitics. It also has a 2nd harmonic termination network that takes into account the parasitic inductance of the load impedance transformation network for reduced size and lower impedance termination.

The developed PA has a chip area of 1.57 x 1.57 mm^2 and is a single-stage design with single-ended input and output. In simulation, its input is reasonably matched to a $50\ \Omega$ impedance environment with a return loss of less than $-9\ dB$ throughout the $2.4\ GHz$ ISM frequency band. The PA presents a small-signal power gain of $15.8\ dB$ with a variation of $0.1\ dB$ on the intended band and is unconditionally stable. The PA achieved a $24.4\ dBm$ saturated output power while having a drain efficiency of 24.53% and a PAE of 22%. It was verified through simulation that the design PA satisfies the requirements for linearity of a communication standard in the 2.4GHz ISM frequency band, the 802.11g standard. When compared to other works in the literature, the PA linearity performance is state-of-the art, although when it comes to output power and efficiency the PA is subpar, this is mainly because of the technology node used that presents low power gain and lossier passives than more recent RF CMOS technologies, but it is also due to some design decisions that were taken.

6.1 Future works

It is undeniable that the work feels incomplete without measurements to confirm simulation results. A measurement of the taped-out chip must be done in the future, as well as other measurements to validate the EM simulation test-benches. A PCB with the correct surface finish for wirebonding (ENIG) is being provided for the measurement of the PA. Future designs must think of a simpler way to measure the chip. Encapsulating it makes the design harder and more constrained due to parasitics in the RF path, but makes the testing much easier.

There are certainly points that can be improved in this design, the 2nd harmonic impedance

network can have a lower input impedance without compromising common-mode stability and the self-biasing of the cascode transistors in the active core degraded the amplifier performance for two less pads, which in retrospect was not necessary.

A fundamental necessity for further work on linear PAs is access to new technology nodes, better passives are fundamental for the PA performance and higher device gain and higher isolation eases the design of amplifier. In this line a two-stage amplifier design is also recommended as it decouples the output stage from the input match, making it possible to make output stages with much bigger transistors, a design feature that would have improved the performance of even this PA in 180nm technology.

CMOS PA design is still a hard problem. There are still academic possibilities to be explored, some listed bellow:

- Exploring harmonic termination networks:
  It has been seen through the design in chapter 3 the great impact that harmonic termination has on class-AB PAs. This topic requires further investigation with the design of new, integrable, tuning networks for terminating harmonics. The power combining inductance prevents a simple broad-band design of this network but a multi-resonant design could certainly improve the PA performance if possible to be realized.

- Exploring power combining possibilities:
  The field of power combining and transformer networks has many possibilities to explore, the heavy dependence of these networks on the layout and the many uses that they must have: Impedance transformation, power combining, fundamental and harmonic impedance tuning, makes them a promising field for work. The proposed network performance was degraded by the non-symmetric input traces, a better layout could be devised without increasing the common-mode parasitic inductance. Also, load modulation effects are a very promising new way to use these networks, that is the effect that the load seen by one of the ports is modulated by the input power on the other port. this effect was first explored in (KAYMAKSUT; REYNAERT, 2014) to make a Doherty amplifier with high back-off efficiency.

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LIST OF PUBLICATIONS

This first publication is regarding the thesis subject while the second is regarding a parallel project that the author developed during this masters.

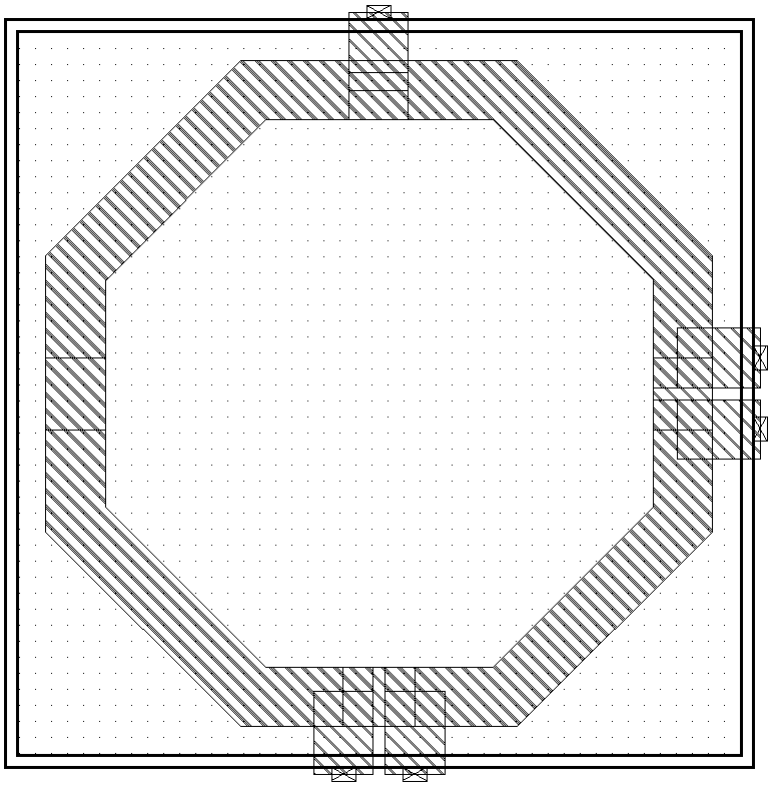
1. **GUIMARAES, G.** ; KLIMACH, H. ; BAMPI, S. ; "A Fully Integrated CMOS 2.4GHz and 24dBm Linear Power Amplifier." in **15th IEEE NEW CIRCUITS AND SYSTEMS CONFERENCE (NEWCAS), 2017**,Strausbourg, France.
2. ANDRADE, N. ; **GUIMARAES, G.** ; DORNELAS, H. ; TOLEDO, P. ; KLIMACH, H. ; FABRIS, E. ; BAMPI, S. ; "Low Power IEEE 802.11ah Receiver System-Level Design Aiming for IoT Applications." in **30th Symposium on Integrated Circuits and Systems Design - SBCCI '17**, Fortaleza, Brazil. (accepted for publication).

APPENDIX A — TRANSFORMERS DESIGN IN GLOBAL FOUNDRIES 130NM TECHNOLOGY

This technology node has a total of seven metal layers with the top two being thick-metal layers, the top metal layer M_7 is an aluminum layer with thickness 4 μm while the layer bellow that M_6 is a copper metal layer with thickness 3 μm. Another advantage is that the thickness of the layers bellow these scale with their level, differently from the 180nm node used in the PA where all layers bellow the top-metal layer have the same thickness.

The first transformer topology is a vertically-coupled $1:1$ transformer, it's layout can be seen in figure A.1 and its geometry parameters are: Inner diameter of 230 μm and trace width of 25 μm, the dielectric thickness between the layers is 4 μm, and the transformer has a total area of 314x 314 μm^2. The resulting narrow-band lumped-circuit parameters can be seen in table A.1 and its G_{max} in figure A.2. The quality factors at 2.45 GHz are $Q_P = 19.3$ and $Q_S = 12.12$. The low inductance seen by the ports is probably because of the high port-to-port capacitance of this configuration.

Figure A.1: Vertically coupled transformer layout.

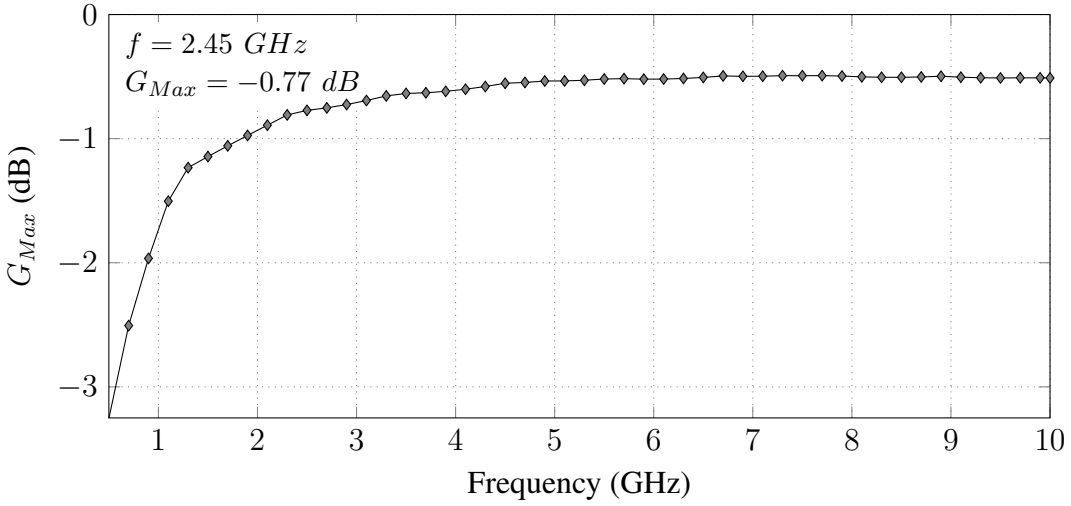


Source: The author.

Table A.1: Designed Transformer Simulation Results at 2.45GHz

Parameter	Value @ 2.45 GHz
L_P	277 pH
R_P	0.221 Ω
L_S	363.8 pH
R_S	0.461 Ω
k	0.731
G_{max}	-0.775 dB
η_{max}	83.65%

Figure A.2: Vertically coupled transformer G_{Max}.

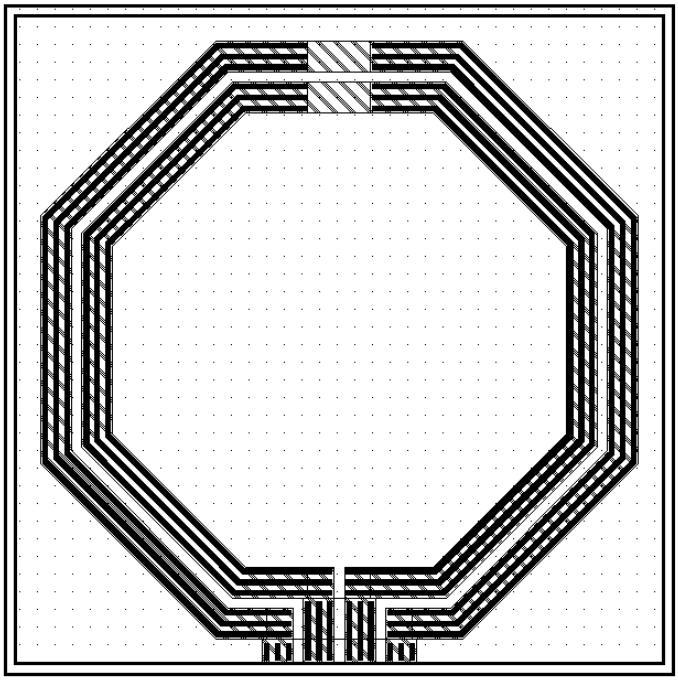


Source: The author.

The second transformer is laterally coupled like the ones developed in the 180nm technology, it has a inner diameter of 220 μm, a trace width of 15 μm with both thick-metal layers connected in parallel. The trace distance is 5 μm which is the minimum allowed by the layout rules. The transformer has a total area of 324 x 324 μm^2, its layout can be seen in figure A.3, its lumped circuit model parameters can be seen in table A.2. The minimum insertion loss is the inverse of the G_{max}, this latter quantity can be seen in figure A.4. The inductances quality factors at $2.45\ GHz$ are $Q_P = 14.1$ and $Q_S = 12.36$.

These two transformers make evident how much the technology parameters can influence the performance of integrated passives, these two transformers were very easily designed and obtained a much better performance than the ones designed in the 180nm node.

Figure A.3: Laterally coupled transformer layout.

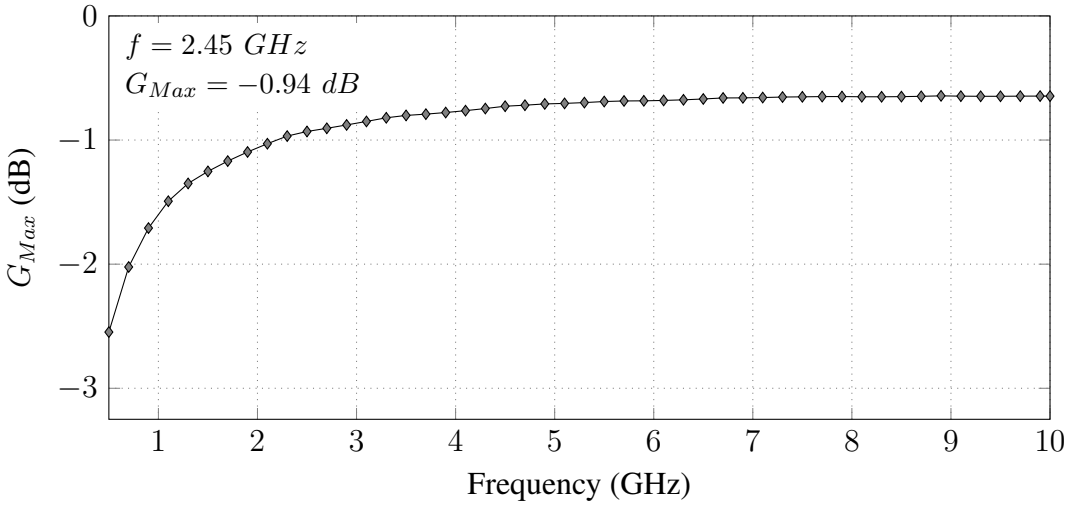


Source: The author.

Table A.2: Designed Transformer Simulation Results at 2.45GHz

Parameter	Value @ 2.45 GHz
L_P	438 pH
R_P	0.478 Ω
L_S	498 pH
R_S	0.620 Ω
k	0.698
G_{max}	-0.94 dB
η_{max}	80.53%

Figure A.4: Laterally coupled transformer G_{Max}.



Source: The author.

APPENDIX B — SUMMARY IN PORTUGUESE

UM AMPLIFICADOR DE POTËNCIA RF CMOS LINEAR COM COMBINADOR DE POTÊNCIA TOTALMENTE INTEGRADO

B.1 INTRODUÇÃO - CAPÍTULO 1

Este capítulo faz um breve histórico do uso de tecnologia CMOS para projeto de circuitos de RF com o objetivo de integrar cada vez mais componentes dos rádios em um único chip. É possível creditar este desenvolvimento como um dos principais fatores que impulsionaram a expansão do mercado de comunicações sem fio nas ultimas décadas. Mostra-se então a importância vital do amplificador de potência, celulares modernos possuem na ordem de dez PAs em umas suas placas para atender os muitos padrões de comunicação com que trabalham, ocupando espaço custoso em placa e sendo parte considerável do custo total dos aparelhos, como exemplo é mostrada na figura 1.2 uma placa de um recente smartphone. Além disso envidencia-se a linha do tempo de PAs CMOS, que chegaram a ser totalmente integrados durante a era 2G e passaram a dominar este mercado, mas perdendo espaço para tecnologias customizadas com o advento de padrões lineares para WLAN, 3G e 4G. Aos poucos PAs CMOS vem recuperando espaço nestes mercados através de soluções inventivas a nível de circuito para solucionar problemas tecnológicos, algumas delas utilizadas neste trabalho como combinação de potência.

Os objetivos do trabalho são então descritos:

- O projeto de um PA na faixa ISM de 2.4GHz, linear o suficiente para uma aplicação em WLAN.
- O PA deve ser totalmente integrado, não requerendo nenhum componente externo em suas redes de casamento.
- O projeto deve ser bem documentado, servindo como guia para futuros projetos desenvolvidos na área.
- O PA deve ser fabricado e ter sua performance medida.

Este ultimo objetivo ficou incompleto devido a falta de acesso a equipamentos de wirebonding e percalços durante o processo de medida como explicado no capítulo de teste.

Então a organização do trabalho é descrita. O capítulo 2 faz uma revisão da teoria de amplificadores de potência RF com foco em amplificadores CMOS e uma revisão do estado-da-arte destes circuitos. O capítulo 3 detalha o projeto do PA, desde especificação à leiaute. O capítulo 4 foca na estrutura de teste preparada, a PCB e o processo de chip-on-board. O capítulo 5 apresenta os resultados obtidos com o PA projetado. Por fim, o capítulo 6 finaliza o trabalho, apresentando as lições aprendidas ao longo deste projeto e propondo novos trabalhos que deem continuidade a este.

B.2 REVISÃO BIBLIOGRÁFICA - CAPÍTULO 2

Neste capítulo aborda-se alguns conceitos básicos necessários para projetos de PAs em tecnologia CMOS. Começando por definir as figuras de mérito que definem o desempenho de um amplificador de potência:

- Potência de saída:
  É a potência que o amplificador consegue entregar à carga, é limitada pela tensão máxima que o amplificador pode ter na sua porta de saída e pela impedância da carga. Para um sinal senoidal, é definida como na equação B.1.

$$P_{saida} = \frac{V_{pico}^2}{2R_{carga}} \tag{B.1}$$

  É possível ver uma característica de grande-sinal de um amplificador típico na figura 2.3, Ela pode ilustrar a definição de métricas como potência saturada, que é a maior potência que um amplificador pode entregar, mesmo com sinal amplamente distorcido e potência média, que é definida como a potência média de saída do amplificador para o qual ele respeita requisitos de linearidade do padrão que se encontra, localizada na região linear da figura.

- Casamento de impedância e ganho de potência:
  Quando um sinal de micro-ondas propagando em uma linha de transmissão ou guia de ondas encontra uma interface com diferença de impedância, parte da sua potência é transmitida pela interface e parte é refletida. Esta ultima pode gerar uma onda estacionária na linha, de onde se define a razão de onda de tensão estacionária (VSWR). Para isto não acontecer é necessário casar a impedância desta interface. No caso do amplificador, é importante que a impedância de entrada esteja casada para baixo VSWR e também para tornar possível o cálculo do ganho de potência do amplificador. Do contrário é impossível fazê-lo porque não é possível saber o quanto de potência é absorvida pela entrada do amplificador e quanto é perdido na linha por causa do alto VSWR.

- Eficiência:
  Existem várias formas de definir eficiência em um amplificador de potência, a mais simples é a chamada eficiência de dreno e é a relação entre a potência entregue à carga e a potência drenada da fonte DC. No entanto esta definição, apesar de simples, não leva

em consideração o quanto de potência o amplificador precisa em sua entrada. Se esta precisa de uma alta potência, a eficiencia do estágio anterior vai ter grande impacto na eficiência do sistema. Por isto uma medida de eficiência utilizada é a eficiência à potência adicionada, ou PAE, definida pela equação B.2. Um fato interessante é que a eficiência de dreno de uma cascata muito grande de amplificadores com o mesmo PAE tende a este valor, comprovando a utilizade desta medida a nivel de sistema.

$$PAE = \frac{P_{saida} - P_{entrada}}{P_{DC}} \tag{B.2}$$

- Linearidade:

  Existem várias métricas de não-linearidade gerais como distorção AM-AM, que é a dependência não-linear da potência de saída em relação à de entrada, e AM-PM, que é a dependência não-constante da fase de saída em relação à potência de entrada. Mas para de fato comprovar que o PA satisfaz os requisitos de linearidade do padrão são necessárias simulações numéricas com o sinal modulado. Este requisitos normalmente são dois: A magnitude média do vetor de erro (EVM), dada em % ou dB tem que ser menor do que um valor definido. Este vetor é definido como a diferença no plano I/Q do sinal transmitido e do sinal ideal da constelação. O segundo requisito é o de máscara, onde o espectro transmitido tem que está contindo dentro de uma máscara de potência, impedindo emissões espúrias que degradariam o sinal de canais adjacentes.

Faz-se então uma introdução as classes lineares de amplificadores: Classe A, AB, B e C. Com o detalhamento de suas formas de onda e relações de compromisso, principalmente entre eficiência e linearidade. A definição de cada uma delas depende da proporção do sinal de entrada que os transistores estão em condução ou corte, definindo ângulo de condução θ_C como o ângulo de fase do sinal de entrar para o qual o transistor conduz, variando de 0 a 360^o. Para a classe A os transistores estão sempre em condução, na classe AB o ângulo de condução está entre $180^o < \theta_C < 360^o$. Para $\theta_C = 180^o$ o amplificador é dito classe B e para ângulos menores que este ele é dito classe C. É identificado um ponto de zero intermodulação de terceira ordem zero na class AB, apresentando alta eficiência teórica. Este é um ponto muito comum para polarização de amplificadores class AB na literatura.

Depois disso analiza-se diferentes estratégias de conversão de impedância para aumento da potência de saída possível em um amplificador CMOS. Mostra-se que redes LC possuem uma relação de compromisso entre eficiência e razão de transformação de impedância extremamente restritiva para os baixos fatores de qualidade encontrados em CMOS. Também analisa-se

redes de transformadores magneticamente acoplados $1 : n$, detalhando as limitações destas. Por fim analisa-se combinadores de potência, em específico transformadores combinadores em série (SCT), que é o tipo de rede utilizada para este trabalho.

B.3 PROJETO DO PA CMOS - CAPÍTULOS 3 e 4

Neste capítulo o processo de projeto é detalhado. Primeiramente define-se os requisitos do PA a ser projetado, podendo ser vistos na table B.1. A tecnologia utilizada é 180nm, e o tapeout que foi um dos 5 dados gratuitamente para projetos de estudantes brasileiros pelo IMEC através do programa mini@sic e a área do chip é de 1660 μm x 1660 μm.

Requisito	Valor
Tecnologia	$180nm$
Tensão de alimentação	$3.3V$
Frequencia	$2.402 - 2.483GHz$
P_{media}*	$16dBm(40mW)$
$P_{saturacao}$*	$24dBm(250mW)$
η_{max}*	30%
Ganho de potência*	$10dB$

Table B.1: Requisitos do PA CMOS.

*Especificação deve ser o maior possível para a área dada.

O projeto começa apresentando a arquitetura de top do PA, vista na figura 3.2. A partir daí começa o projeto do núcleo ativo do amplificador, que consiste em um par diferencial com cascode, sendo o transistor ligado em fonte-comum um de óxido fino e o ligado como porta-comum um transistor de óxido expesso. Os transistores são polarizados no opnto de mínima distorção de terceira ordem, em classe AB, e otimizados para uma carga de 25Ω diferencial. Também é utilizada uma estratégia de linearização da capacitância de entrada dos transistores através da introdução de um capacitor PMOS em paralelo (CHOWDHURY et al., 2009). Após isto, o layout desde bloco é apresentado e analisado. O amplificador com rede ideal, núcleo ativo em layout e filtro de segundo harmônico ideal atinge uma potência máxima de saída de com uma eficiência de dreno de .

O projeto da rede de saída começa com o projeto de amplificadores $1 : 1$ que irão compor o SCT. O layout destes dispositivos é apresentado em 2.23. A perda de inserção mínima alcançada é de $G_{max} = -1.57dB$, os transformadores são sintonizados para operação em $2.45GHz$ e com impedâncias de 25Ω, os parâmetros S resultantes são apresentados em 3.17. O impacto da utilização destes transformadores ao invés de ideais no desempenho do amplificador

é analisado. O amplificador com este tranformador interconectado de forma ideal, núcleo ativo em layout e filtro de segundo harmônico ideal atinge uma potência máxima de saída de com uma eficiência de dreno de .

O leiaute do SCT é apresentado em 3.18. Em sua saída foi projetado um capacitor customizado de placas paralelas com tensão de ruptura em centenas de volts, este capacitor é utilizado para a sintonia de saída do combinador. A perda de inserção mínima atingida é de $G_{mx} = 2.24dB$. O amplificador com este transformador, núcleo ativo em layout e filtro de segundo harmônico ideal atinge uma potência máxima de saída de com uma eficiência de dreno de .

Após isso a rede de terminação de impedância de segundo harmônico é projetada, fazendo uso do tap central do transformador para modificar a impedância de modo-comum vista pelo amplificador sem alterar a impedância de modo-diferencial. Com esta rede real o amplificador atinge uma potência de saída de com uma eficiência de dreno de .

Por fim, a rede de casamento de impedância é projetada usando associações de transformadores. Esta rede atinge casamento melhor que $-9dB$ na faixa de $2.4 - 2.5GHz$.

O Chip foi para tapeout e uma PCB foi projetada pensando em medir o chip em duas configurações, uma com sinais de RF conectados à placa e outra somente com os sinais de baixa frequência conctados pensando em fazer o acesso aos sinais de RF através de microponteiras. A UFRGS não possui uma máquina de wirebonding, a máquina utilizada só possuia fios de ouro e o acabamento utilizado na placa não era o apropriado para este tipo de material. Este acontecimento inviabilizou até o presente momento a medida dos chips fabricados.

B.4 RESULTADOS - CAPÍTULO 5

Neste capítulo são apresentados os resultados de simulação do PA. No test-bench são estimados os efeitos dos bondwires de alimentação, terra e sinais de polarização.

- Estabilidade e casamento:

  Os parâmetros de pequenos sinais do amplificador são analisados, os resultados podem ser vistos em 5.1 e 5.2. O ganho do amplificador é $S_{21} = 15.8 \pm 0.1dB$ na faixa de $2.4 - 2.5GHz$, com isolação melhor do que $38.7dB$ e casamento melhor que $-9dB$. O PA é incondicionamente estável em modo diferencial e uma simulação transiente é feita com resultados podendo ser vistos em 5.5 para garantir que o circuito também é estável em modo comum.

- Comportamento em grandes sinais:
  O amplificador tem como potência máxima de saída $24.4dBm$ com uma eficiência de dreno de 24.53% e uma PAE de 22%. As curvas de comportamento em grandes sinais do amplificador podem ser vistas em 5.6.

- resultados de não linearidade:
  O PA foi avaliando em relação a sua distorção AM-AM e AM-PM, cujas curvas podem ser vistas em 5.8. O ponto de compressão de 1dB referido à saída é de $OP1dB = 20.03dBm$ e o sinal sofre uma distroção não-linear de fase de 1.2^o até essa potência de saída. Outra forma de medir não-linearidade é atravez de um teste de dois tons e medição de distorções de intermodulação. O resultado deste teste pode ser visto em 5.9. A 3dB do ponto de compressão temos $IM3 = 24.22dB$, $IM5_{inferior} = 48.16dB$ e $IM5_{superior} = 49.8dB$.

- Aplicação: Sinal do padrão IEEE 802.11g:
  Um sinal totalmente modulado do padrão IEEE 802.11g foi aplicado na entrada do amplificador, a potência média de saída na qual o amplificador satisfaz os requisitos de linearidade do padrão é $P_{media} = 15.4dBm$. Esta potência é limitada pelo EVM, que atinge o valor de 5.43% or $-25.3dB$. O espectro de saída do sinal no primeiro e último canal do protocolo pode ser visto nas figuras 5.10 e 5.11. Enquanto a constelação pode ser vista em 5.12.

É feita uma breve comparação com outros trabalhos do estado-da-arte. Nesta comparação o nosso amplificador atinge uma potência de saída comparável ao outro amplificador de único estágio apresentado e se destaca em relação a este por ter sua entrada casada e por suportar sinais modulados. Já quando comparado com amplificadores mais recentes nosso amplificador tem um desempenho inferior em relação à potência de saída e eficiência, a razão dada para isto é por causa da antiga tecnologia utilizada e da restrição de área, além de alguns pequenos defeitos que foram evidenciados no capítulo do projeto que poderiam melhorar marginalmente a performance do amplificador, como uma nova rede de terminação do segundo harmônico de sinal.

B.5 CONCLUSÃO - CAPÍTULO 6

Este trabalhou apresentou o desenvolvimento um amplificador CMOS totalmente integrado para padrões de comunicação lineares em tecnologia 180nm CMOS. O fluxo de projeto foi detalhadamente relatado e envolve a análise dos desafios e soluções de integrar um circuito de alta potência e alta frequência em uma tecnologia com baixa tensão de alimentação e passivos de baixa qualidade. A solução que para o qual amplificadores recentes convergiram e que o nosso PA utilizou são redes de combinação de potência. Para isto foi projetado um transformador combinador em série com auxílio de um simulador eletromagnético 2.5D. O faz uso de terras AC para torná-lo mais robusto contra parasitas nos bondwires na alimentação e terra. Ele também possui uma rede de terminação de segundo harmônico.

O PA tem uma área de 1.57 x $1.57mm^2$ e possui um único estágio de amplificação com saída e entradas modo-comum. A entrada é casada para uma impedância de 50Ω com um parâmetro de reflexão de menos de $-9dB$ na banda ISM de 2.4 GHz. O PA apresenta um ganho de pequenos-sinal de $15.8dB$ com uma variação de $0.1dB$ em sua banda e é incondicionalmente estável. O PA atingiu uma potência de saída de $24.4dBm$ com uma eficiência de dreno de 24.53% e uma PAE de 22%. Foi verificado por simulação que o PA satisfaz os requisitos de um padrão de comunicação altamente linear na banda ISM de 2.4GHz como o padrão 802.11g.

B.5.1 Trabalhos futuros:

- Desenvolvimento de novas redes de terminação de harmônicos:
  Foi visto no capítulo 3 o grande impácto que terminação harmonica tem em PAs classe AB. Esse tópico requer mais investigação e o desenvolvimento de novas redes de terminação de harmonicos totalmente integradas compatíveis com topologias de PAs atuais.

- Explorar as novas possibilidades de redes de cominação de potência:
  O campo de redes de combinação de potência ainda é novo e apresenta várias possibilidades de inovação. A grande dependência que estas redes possuem do seu layout e o grande número de características simultâneas que elas devem possuir reforçam este fato. A Rede utilizada neste trabalho, por exemplo, teve seu desempenho piorado pela assimetria de suas conexões de entrada. Efeitos de modulação de carga são uma nova forma de usar estas redes, isto é o efeito que muda a carga vista por uma das portas dependendo

da potência inserida em outra porta de entrada. Este efeito foi explorado em (KAYMAK-SUT; REYNAERT, 2014) para fazer um transformador Doherty totalmente integrado com alta eficiência a uma potência média de saída.