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MAICO CASSEL DOS SANTOS

Adaptive Low Power Receiver combining ADC Resolution and Digital Baseband for Wireless Sensors Networks based in IEEE 802.15.4 Standard

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Advisor: Prof. Dr. Luigi Carro

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ABSTRACT

With the increase of Internet of Things applications and devices, many efforts to reduce power consumption in transceiver has been invested. Most of them targeted in RF frontend, converters, or in the digital baseband architecture individually. As result, there are few margins nowadays for power improvement in these blocks singly that compensates the huge hard work required.

The next optimization step leads to a system level analysis seeking design space and new possibilities expansion. It is in this field that adaptive systems approaches are conquering ground recently. The solutions combines Radio Frequency (RF) and process variation techniques, Low Pass Filters (LPF) and Analog to Digital Converters (ADCs) adjustment for better performance, digital baseband bit width adaptive according to income packet SNR, configurable ADC resolution and topology, and others.

In this scenario the current work proposes an adaptive system level architecture targeting ADC and digital receiver power reduction. It uses a robust algorithm for digital baseband receiver, a Sigma-Delta ADC, and suggests a feedback control block based on packet SNR measure. The system was designed for the IEEE 802.15.4 standard and required system modeling using Matlab tool, hardware description in Verilog language, and logic synthesis using X-FAB XC018 process for validation and power consumption estimation.

Simulations show up to 15% of system power reduction and still meeting the standard requirements. The work results were published in the International Instrumentation and Measurement Technology Conference of 2014 occurred in Montevideo - Uruguay.

Keywords: IEEE 802.15.4. Wireless Sensor Network. ZigBee. Sigma-delta ADC. Digital baseband transceiver.

Receptor adaptativo de baixa potencia combinando resolução de conversor analógico para digital e banda base digital para redes de sensores sem fio baseado no protocolo IEEE 802.15.4

RESUMO

Com o aumento das aplicações e dispositivos para Internet das Coisas, muitos esforços para reduzir potência dissipada nos transceptores foram investidos. A maioria deles, entretanto, focam individualmente no rádio, nos conversores analógicos para digital e vice-versa, e na arquitetura de banda base digital. Como consequência, há pouca margem para melhorias na potência dissipada nestes blocos isolados que compense o enorme esforço. Portanto, este trabalho propõe uma arquitetura adaptativa a nível de sistema focando em reduzir o consumo no conversor analógico para digital e no receptor digital. Ele utiliza um algoritmo robusto para o receptor banda base digital, um conversor analógico para digital topologia Sigma-Delta e um bloco de controle realimentado conforme a relação sinal ruído medida do pacote recebido. O sistema foi projetado para o protocolo IEEE 802.15.4. Para validação do sistema e estimar a potência consumida foi feito um modelo de sistema utilizando a ferramenta Matlab, uma descrição do hardware em linguagem Verilog e uma síntese lógica utilizando o processo da X-FAB XC018. As simulações mostram uma redução na potência consumida pelo sistema de até 13% e ainda atingindo os requisitos do protocolo. Os resultados deste trabalho foram publicados na conferência internacional em tecnologia de instrumentação e medidas de 2014 realizada na cidade de Montevidéu no Uruguai.

Palavras Chave: IEEE 802.15.4. Redes de sensores sem fio. ZigBee. Sigma-delta conversores de analógico para digital. Transceptor banda base digital.

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LIST OF ABBREVIATION AND ACRONYMS

ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPF	Band Pass Filter
BW	Band Width
CCA	Clear Channel Assessment
CIC	Cascade Integrator and Comb
CMOS	Complementary Metal-Oxide Semiconductor
CORDIC	Coordinate Rotation Digital Computer
CS	Carrier Sense
DA	Drive Amplifier
DC	Direct Current
DAC	Digital to Analog Converter
DCR	Direct Conversion Receiver
DCT	Direct Conversion Transceiver
DSSS	Direct Sequence Spread Spectrum
ED	Energy Detection
ENOB	Effective Number Of Bits
EVM	Error Vector Magnitude
FIFO	First-In First-Out
IC	Integrated Circuits
IDSE	Interference Detector and SNR Estimator
IF	Image Filter
IEEE	Institute of Electrical and Electronic Engineers
IEC	International Electrotechnical Commission
IoT	Internet of Things
IRM	Image Reject Mixer
ISO	International Organization for Standardization
FIR	Finite Impulse Response
FSM	Finite State Machine

LO	Local Oscillator
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LQI	Link Quality Indicator
LR	Low Rate
LUT	Look-up Table
MAC	Medium Access Control Layer
MCU	Memory Control Unit
MPDU	MAC Protocol Data Unit
NCO	Numerically Controlled Oscillator
OSI	Open System Interconnect
OSR	Oversampling Rate
O-QPSK	Offset Quadrature Phase Shift Keying
PER	Packet Error Rate
PHR	PHY header
PHY	Physical Layer
PLL	Phase-Locked Loop
PN	Pseudorandom Noise
PPDU	PHY Protocol Data Unit
PSDU	PHY Service Data Unit
POS	Personal Operating Space
RF	Radio Frequency
RSS	Received Signal Strength
RTL	Register Transfer Level
Rx	Receiver
SAR	Successive Approximation Register
SFD	Start-of-Frame Delimiter
SHR	Synchronization Header
SNDR	Signal Noise Ration and Distortion Ratio
SNR	Signal-to-Noise Ratio
TCF	Toggle Count Format
TDMA	Time Division Multiple Access
Tx	Transmitter
VCO	Voltage Controlled Oscillator

VGA	Voltage Gain Control
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network

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1 INTRODUCTION

The Internet of Things (IoT) is increasingly present in our lives and it is bringing a consequence: the world is becoming wireless. The main reasons are clear: low cost, reliability, and mobility. Tech big players companies like Cypress, Qualcomm, Atmel, Samsung, Facebook, Microchip, NXP and Google are moving sharply in this direction spending 13 billions of dollars last year in merge and acquisition.

There are many applications and respective limitations in this field. Most of them have to keep the power consumption under control to guarantee the mobility market requirement. Some have to operate years using a single battery, requiring ultra low power devices over the time (low energy). Home Automation, Smart Energy, Building Automation, Health Care, and Wireless Sensors Network are some examples in which low power devices are mandatory.

IEEE 802.15.4 standard contributes in this field by defining data rate, modulation, signal degradation, minimum distance between devices, and many other parameters targeting low power and low data rate wireless networks. In complement, IC designers have spent uncountable effort in the search for the best algorithms and architectures to push transceivers power consumption to the ground. RF front-end, converters, and digital baseband were already deeply optimized in such way that there is not too much margin to improve in the block level.

The presented work, therefore, explores a bigger picture of the transceiver architecture and, through the study of digital baseband and analog-to-digital converter characteristics, proposes an adaptive system level architecture in which reduces up to 15% the overall power with insignificant overhead. The solution uses the noise robustness of the first, the relationship between resolution and power of the second, and the income signal quality as advantage for an optimum system level relation of signal-to-noise ratio and power.

Chapter 2 presents an overview of IEEE 802.15.4 standard, the transceiver internal blocks, and low power architectures proposed in literature. Chapter 3 details the adaptive architecture including sigma-delta ADC, digital baseband processes, and adaptive control. Also, it describes the system simulation. Chapter 4 details the hardware architecture developed including micro-architecture, RTL simulation, logic synthesis, and the final results. Chapter 5 presents the conclusion and future work.

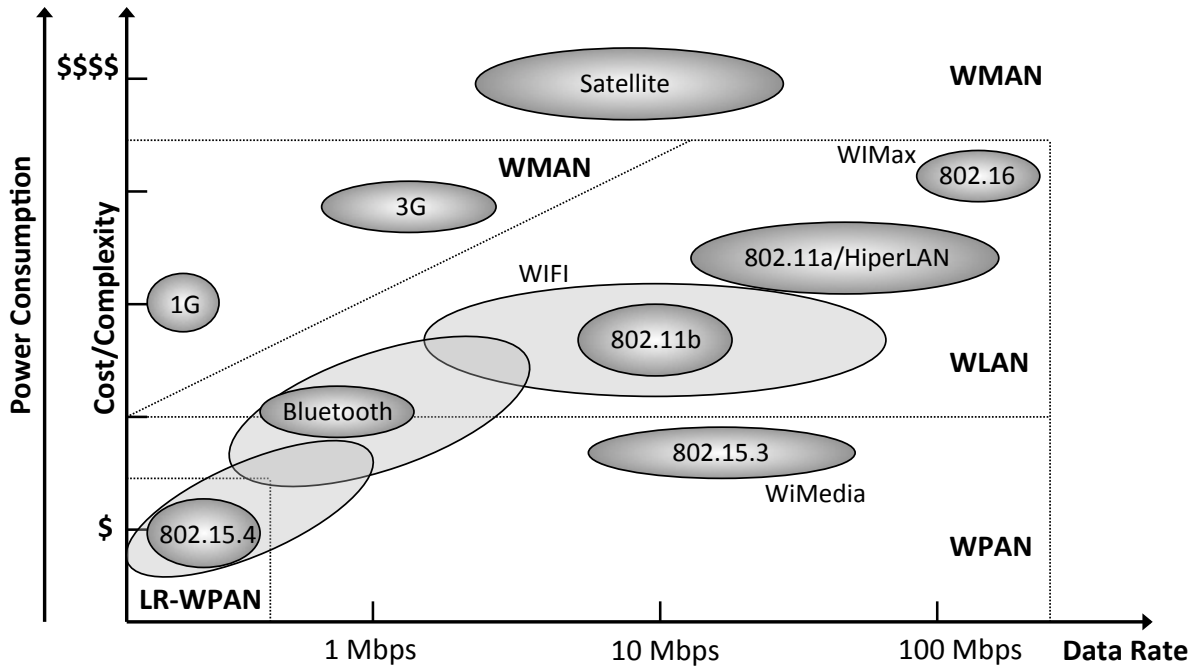
2 WIRELESS SYSTEM

2.1 Why IEEE 802.15.4?

The concept of using wireless communication to gather information or perform certain control tasks inside a house or factory is not new. There are several standards for short-range wireless networking, including IEEE 802.11 and Bluetooth. Each of these standards has its advantages in particular applications.

IEEE 802.11b, for instance, presents high data rate (up to 11 Mbps) and one of its typical applications is providing Internet connections (IEEE 802.11B, 2012). Bluetooth has a medium data rate (1 to 3 Mbps) and its indoor range is typically 2 to 10 meters. The most popular application is wireless headsets, where the Bluetooth is used for communication between a mobile phone and a hands-free headset (IEEE 802.15.3, 2003). IEEE 802.15.4 standard, on the other hand, targets mainly for battery-powered applications, where low data rate, low cost, and long battery life are main requirements. Its data rate of 250k bits per second is commonly adopted in wireless sensors networks (IEEE 802.15.4, 2006). Figure 2.1 summarizes the basic characteristics of the three standards and their fitness with other wireless standards. IEEE 802.11b was used in the comparison because, in the 802.11 standards family, it has the equivalent 2.4GHz band of the two above.

Figure 2.1 - Wireless system standards



Source: The author

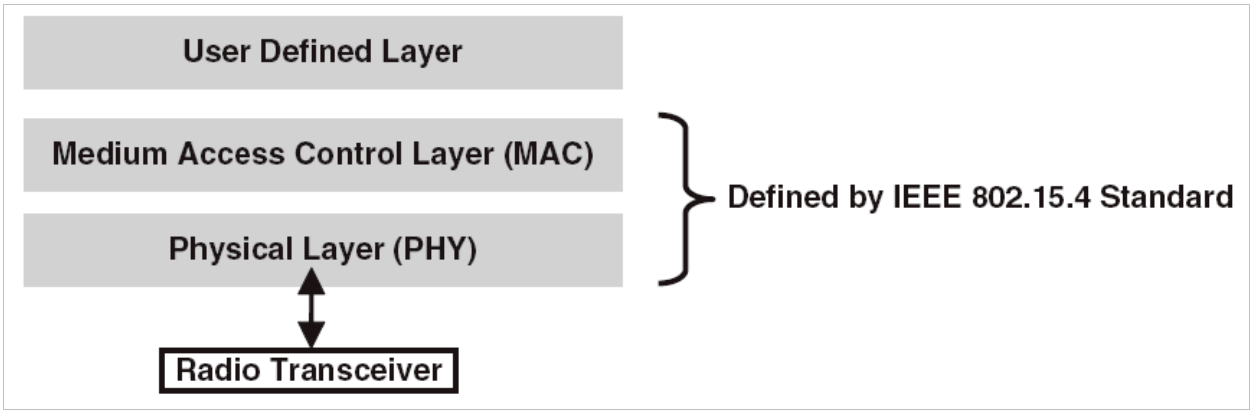
Moreover, while the IEEE 802.11 is Wireless Local Area Network (WLAN) short-range class, the other two are Wireless Personal Network (WPAN). This means that the first is a replacement or extension of a wired Local Area Network (LANs) such as Ethernet (IEEE 802.3) and the goal is to maximize the range of data-rate. WPANs, in contrast, are not developed to replace any existing wired LAN but to provide the means for power efficient wireless communication within the personal operating space (POS) without the need of infrastructure. POS is the spherical region that surrounds a wireless device and has a radius of 10 meters (GUTIERREZ, CALLAWAY and BARRET, 2007).

IEEE 802.15.4 is classified as low rate (LR) WPAN class because of its maximum data rate of 250kbps. As a result it merges the generality, flexibility, and low cost wireless network characteristics of a WPAN with ultra low power specification, becoming a higher potential for large-scale applications.

2.2 Standard Overview

Initially released in 2003, the IEEE 802.15.4 is developed by IEEE 802 standard committee and is divided in two layers based on the Open System Interconnect (ISO/IEC 7498-1, 1994) reference model and illustrated in Figure 2.2

Figure 2.2 - IEEE 802.15.4 layers



Source: IEEE 802.15.4 (2006)

The PHY layer specification determines the physical level characteristics such as frequency of operation, data-rate, and receiver sensitivity requirements. It is responsible for activating the radio that transmits or receives packets, selects the channel frequency and makes sure any other devices on another network do not currently use it.

The MAC layer provides the interface between PHY layer and user-defined layer, usually network layer. It is responsible for generating frames (beacon, data, acknowledge, and MAC command), synchronizing the device to the network if it is configured as a synchronous network (beacon enabled), and providing device network association and disassociation services. For more details about the standard, please refer to IEEE 802.15.4 (2006)

The standard has at least three operation modes: transmitting, receiving, and idle. Therefore, it is not possible to transmit and receive data at same time.

In idle mode, the transceiver is off and waits for a request from MAC or up layers. Transmission and reception requires more detail and are presented in next two subsections.

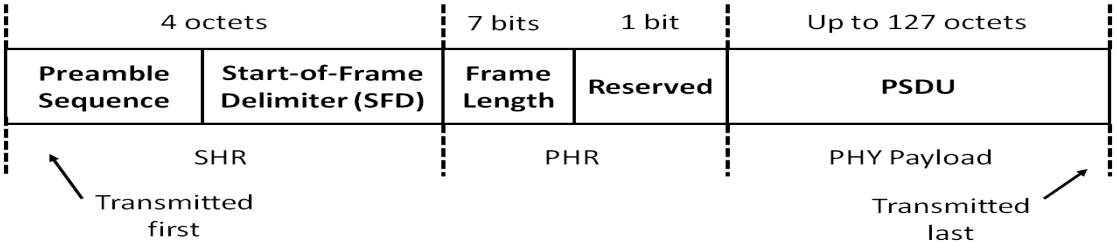
2.2.1 Transmission Mode

In a transmission mode, the transceiver is turned on and the MAC request the PHY to perform a clear channel assessment (CCA) to insure the channel is not in use by any other device. The CCA can be performed through Energy Detection (ED), Carrier Sense (CS) or both. The first estimates the signal energy level in the desired channel while the second demodulates the signal to verify whether the signal modulation and spreading are compliant with the characteristics of the PHY.

Further, if the channel is clear, MAC sends the payload to PHY, which includes the synchronization header (SHR) and the PHY header (PHR) to the packet before transmission. The SHR consists of preamble and start-of-frame delimiter (SFD). They enable the receiver to synchronize and lock into bit stream. Both are binary values of 32 zeros and 0xE5 respectively. The PHR consist of 7 bits, which represent the frame length information in octets.

PHY Service Data Unit (PSDU) is the convention name for the PHY payload sent by MAC and PHY Protocol Data Unit (PPDU) is for final packet transmitted, as it is illustrated on Figure 2.3.

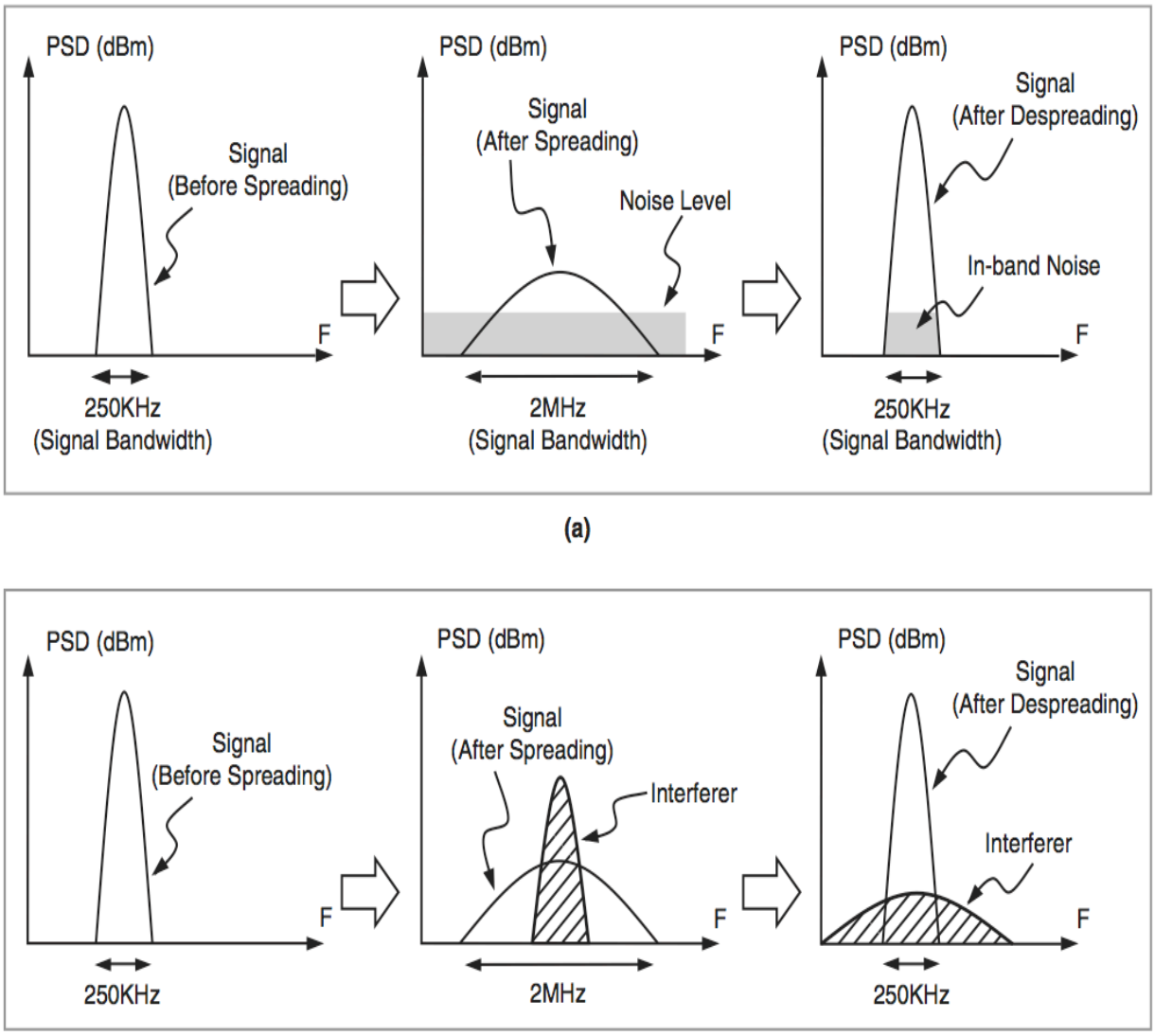
Figure 2.3 – PPDU packet format



Source: IEEE 802.15.4 (2006)

IEEE 802.15.4 uses spread spectrum methods to improve the receiver sensitivity level, increase jamming resistance, and reduce effect of the multipath. The spreading method used is the Direct Sequence Spread Spectrum (DSSS). In this sense, every 4 bits of each octet of PPDU are grouped together and referred to as symbol. Then a lookup table is used to map each symbol in a unique 32-bit sequence. This 32-bit sequence is also known as the chip sequence or the pseudorandom noise (PN) sequence. Figure 2.4 (a) shows the concept of signal spreading, Figure 2.4 (b) shows the reduced effect by interferes and Table 2.1 the lookup spreading table.

Figure 2.4 - Spread spectrum signal effect



Source: Farahani (2008, p. 146)

Table 2.1 - Spread spectrum encode

Data Symbol (b0,b1,b2,b3)	Chip Value (c0, c1,…,c31)
0 0 0 0	1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0
1 0 0 0	1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0
0 1 0 0	0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0
1 1 0 0	0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1
0 0 1 0	0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1
1 0 1 0	0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0
0 1 1 0	1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1
1 1 1 0	1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1
0 0 0 1	1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1
1 0 0 1	1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1
0 1 0 1	0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1
1 1 0 1	0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0
0 0 1 1	0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0
1 0 1 1	0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1
0 1 1 1	1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0
1 1 1 1	1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0

Source: IEEE 802.15.4 (2006)

The use of spread spectrum improves the signal noise ratio according to the following formula (FARAHANI, 2008):

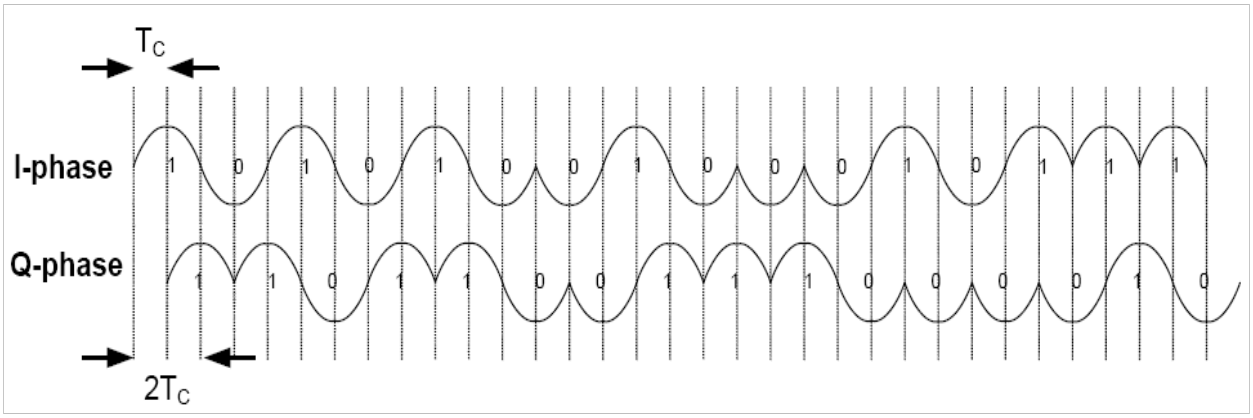
$$Process\ Gain = 10.\log\left(\frac{2Mbps}{250kbps}\right) = 9.03\ dB \tag{2.1}$$

The chip sequences representing each data symbol are modulated onto the 2.4GHz carrier using Offset-Quadrature Phase Shift Key (O-QPSK) with half-sine pulse shaping. Even indexed chips are modulated onto the *in* phase "I" and the odd indexed chips onto the *quadrature* phase "Q" carrier.

To form the offset between *I* phase and *Q* phase the last shall be delayed by T_c with respect to *I* phase, where T_c is the inverse of the chip rate (2 Mchip/s).

Figure 2.5 illustrates the O-QPSK chip modulation.

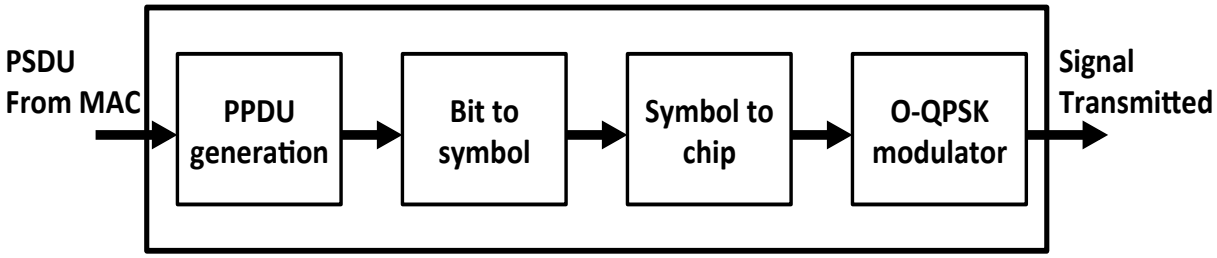
Figure 2.5 - Half-sin O-QPSK modulation



Source: IEEE 802.15.4 (2006)

The functional block diagram in Figure 2.6 illustrates the transmitter processes discussed.

Figure 2.6 - Transmitter internal processes



Source: The author

2.2.2 Reception Mode

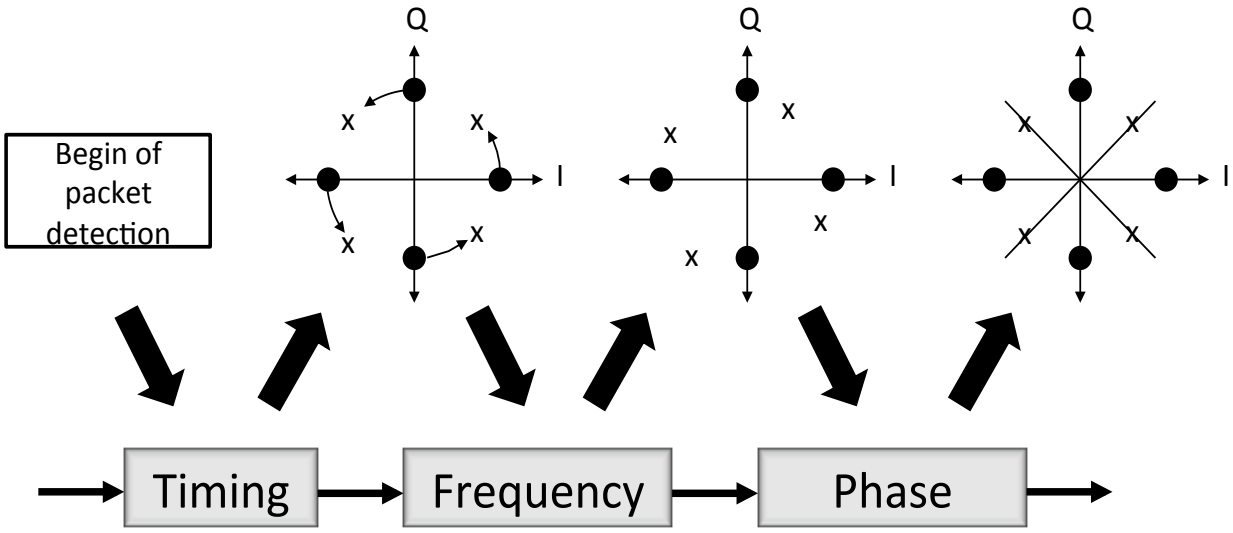
In the reception mode, the transceiver detects the transmitted packet and brings the signal from 2.4GHz frequency carrier back to the 2 MHz baseband. The signal power must be in a range of -85 dBm and -20 dBm for a proper detection and accomplishment of packet error rate (PER) less than 1%.

In addition, the reference clocks in the receiver and transmitter of two different nodes might have a difference of up to ±80 ppm, leading into a maximum rotation speed in O-QPSK constellation of ±200 kHz. The receiver uses the preamble sequence (PHR) and carrier recovery architecture to synchronize its clock and to lock the bit stream.

Carrier Recovery, as shown in Figure 2.7, requires timing, frequency, and phase synchronization. The first detects the beginning of preamble in a sample precision. Frequency

synchronizer estimates the carrier offset and compensates it, resulting in the stop of the constellation rotation. The last adjusts the symbol phase to expected position.

Figure 2.7 - Synchronization processes



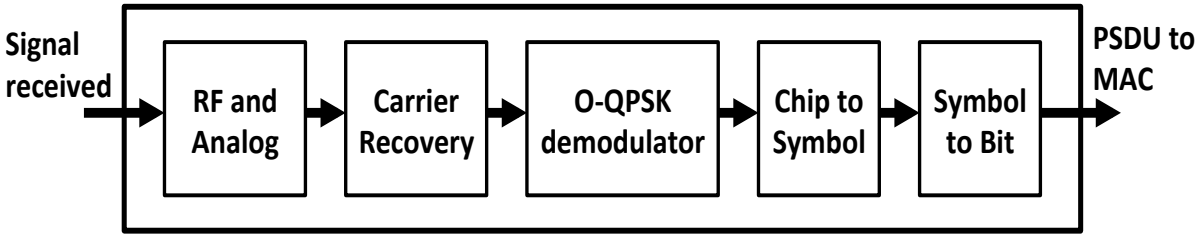
Source: The author

In parallel with the preamble synchronization, the receiver estimates the link quality indicator (LQI) based in received signal strength (RSS), the ratio of the desired signal energy to the total in-band noise energy (SNR), or both. LQI is an indication of the quality of data packets received by the receiver. It is sent to MAC layer and is available to other layers for any type of analysis such as routing path decisions.

Demodulation uses the start of packet detected in the timing synchronizer to sample the signal closest of the peak of half-sin. Positive sample leads to bit “1” and negative, “0”. Further despreading remaps the chip containing 32 bits to symbol and the symbol to set of 4 bits. They are concatenated to form the original octet base packet.

Finally, reception process is represented according to the block diagram of Figure 2.8.

Figure 2.8 - Receiver internal processes



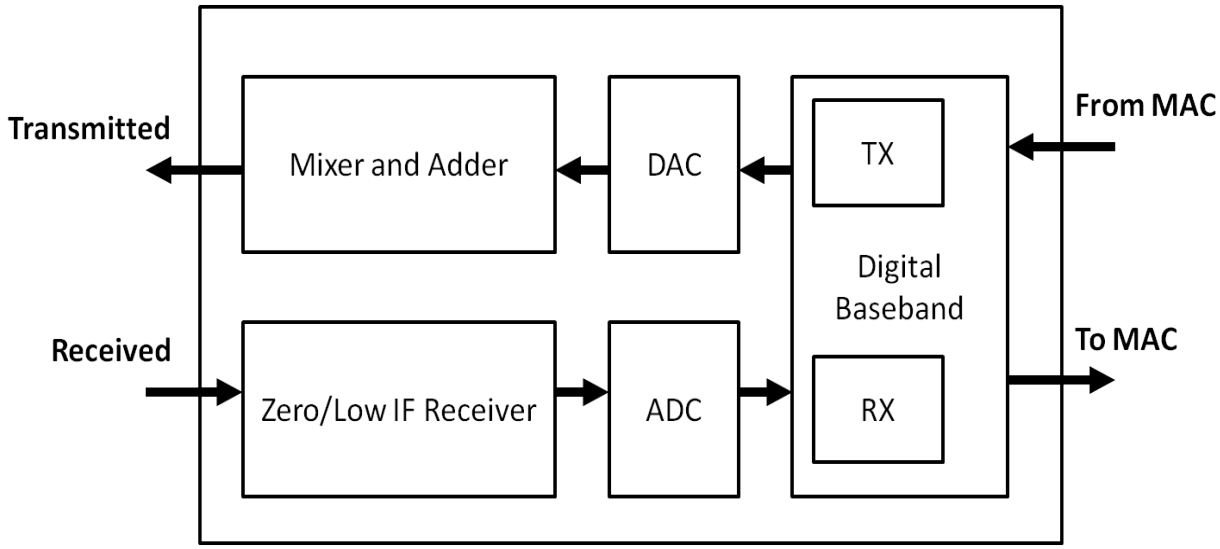
Source: The author

Usually, MAC and up layers are performed by a processor, except for AES cryptographic block which often it is executed by a co-processor. PHY layer, on the other hand, requires a specific hardware according to standard and transmission frequency. Next section discusses some transceiver architectures found in literature and solutions presented for power reduction.

2.3 Low Power Transceivers Architectures

Transceivers architectures, as shown in Figure 2.9, comprise three distinct parts: analog, mixed-signals, and digital. The first is the RF Frontend responsible for modulating and demodulating the signal. The second are the converters, which transform the analog signal to digital and vice-versa (ADC/DAC). The last one is the digital baseband, which synchronizes, encodes and decodes, and controls the PHY operation.

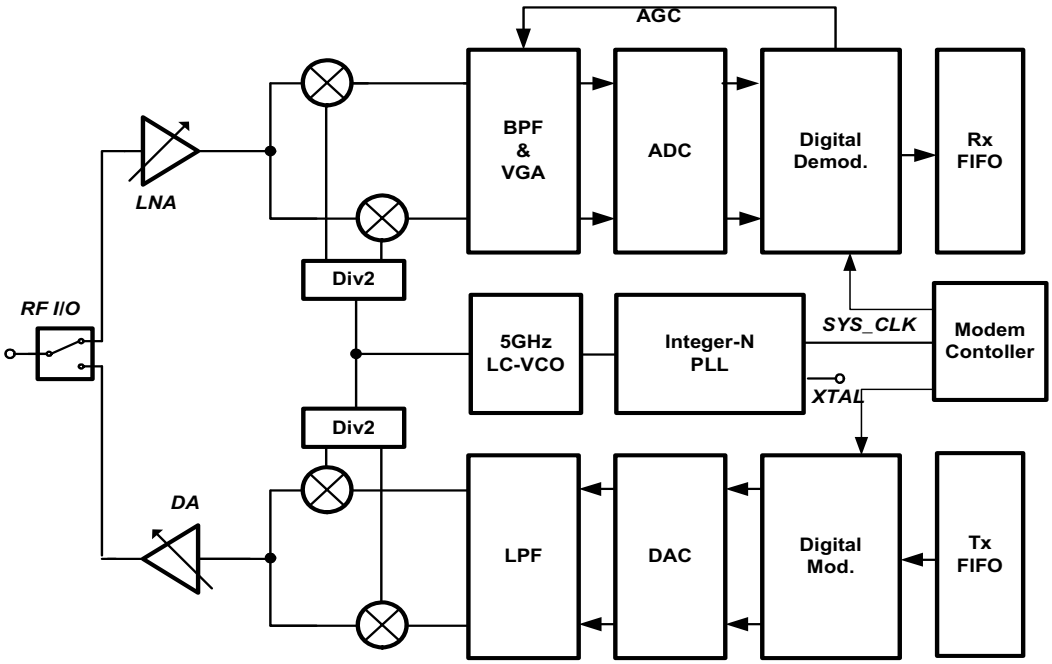
Figure 2.9 - Transceiver basic blocks



Source: The author

Figure 2.10 illustrates an example of a more detailed full transceiver architecture presented by Lim, Cho, *et al.* (2006). From it can be extracted the blocks that comprises the RF Fronted: Low Noise Amplifier (LNA), Mixers, Band Pass Filter (BPF), Variable Gain Amplifier (VGA), Voltage Controlled Oscillator (VCO), Phase-locked Loop (PLL), Low Pass Filter (LPF), and Drive Amplifier (DA). Also, the digital baseband contains the Digital Demodulator, Rx FIFO, Modem Controller, Tx FIFO, and Digital Modulator.

Figure 2.10 - Transceiver architecture example



Source: Lim, Cho, *et al.*(2006)

This architecture consumes the same current in transmission and reception modes, 25mA. It is not unusual, although, that the transmitter spends more power than the receiver. This relation will depend on architecture, design, and signal gain in the Drive Amplifier.

In fact, the gain required to transmit the signal through antenna drives most of the RF Frontend power in transmission mode. DAC and transmitter baseband blocks have low complexity, driving insignificant power.

In the reception, however, digital carrier synchronization requires complex digital processing and ADC has to oversample the signal at least in the Nyquist criteria. The result is a bigger share in power consumption of these blocks in the receiver compared to transmitter.

There are horde topologies and architectures of transceivers and to cover all of them is not the goal of this section, but to discuss some of them that are related to this work.

2.3.1 RF Frontend

Direct conversion transceiver (DCT) architecture is the favorite solution for single-chip radio implementations due to high level of integration and low power consumption. It does not need an image rejection filter and the IF band-pass filter is replaced by the low-pass

filter. In IEEE 802.15.4 compliant devices, in contrast, it is not rare to find Low IF instead of Zero IF (direct conversion) architecture for the receiver.

The main advantage of Low IF receiver is the absence of flicker noise. Also, the limiting IF avoids the need of automatic gain control (AGC) and offer fast response to rapidly change signal levels due to link fading conditions. Also, the discriminator and slicing circuits are straightforward to design (NOTOR, CAVIGLIA e LEVY, 2003).

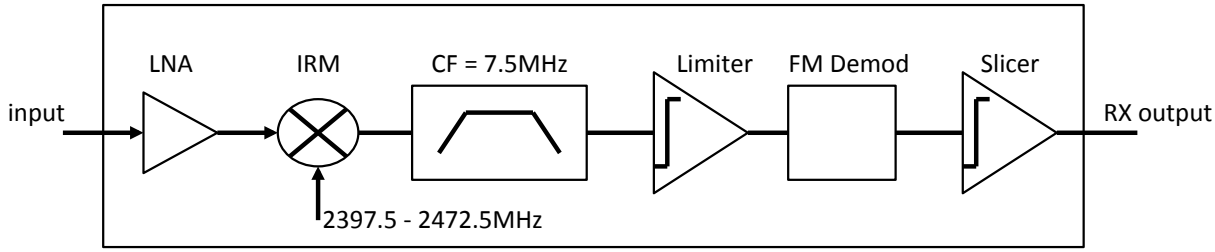
The primary disadvantage of the Low IF architecture is a loss of about 3 dB in sensitivity in comparison to Zero IF receivers. Additionally, a channel filter is required to extract the desired carrier, reject nearby interfering signals, and set the receiver pre-detection noise bandwidth. Finally, an image reject mixer (IRM) is required to reject signals at or near the receiver image frequency.

On the other hand, Zero IF architecture has four advantages compared to Low IF. The first it does not require the transceiver local oscillator (LO) to change frequency when transitioning between transmit and receive modes. Second, it does not require image reject mixer since there is no image frequency. Third, Zero-IF architecture utilizes a pair low pass filters, that are simpler to implement, to reject the high frequency noise and increase the SNR of output signals *I* and *Q*. Finally, the Zero IF architecture supports optimum demodulation with matched filter and synchronous detection techniques.

Unfortunately, Zero IF presents many imperfections like DC-offset, even-order distortion, flicker noise, I/Q mismatch and LO pulling/pushing (RAZAVI, 1997). To compensate them, the architecture include automatic gain control (AGC), post-mixer DC offset cancelation, and additional circuitry to implement synchronous demodulation and optimum baseband filtering. In addition, some care has to be taken to preserve amplitude balance and quadrature phase shift for the channels *I* and *Q* – also known as Error Vector Magnitude (EVM). This leads to a higher receiver currents and greater power dissipation in return to superior performance.

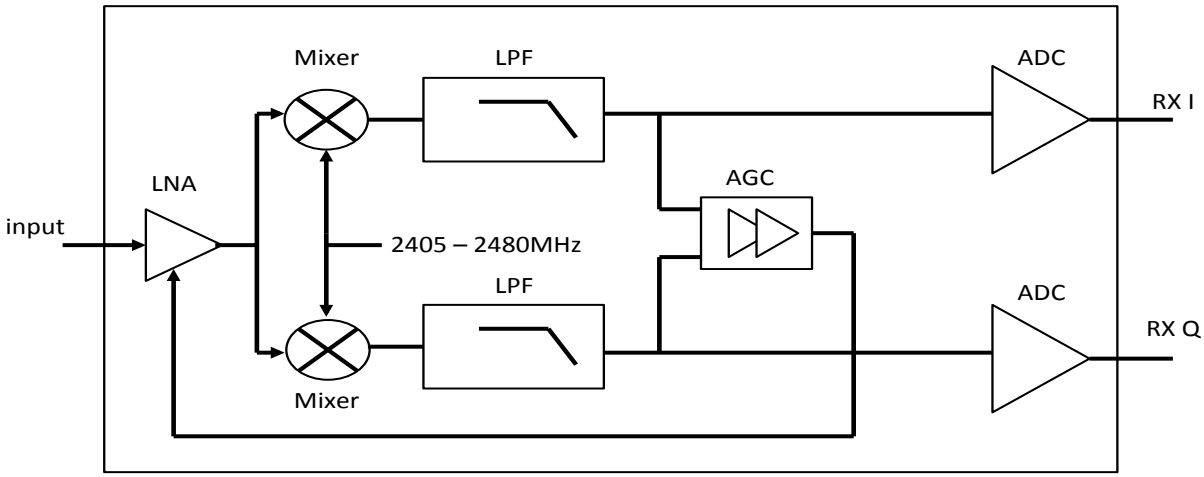
Figure 2.11 and Figure 2.12 illustrates Low IF and Zero IF architectures respectively.

Figure 2.11 - Low IF frontend architecture



Source: Notor, Caviglia and Levy (2003)

Figure 2.12 - Zero IF frontend architecture



Source: Notor, Caviglia and Levy (2003)

Moreover, Notor, Caviglia and Levy (2003) presents a comparison of Low-IF vs. Zero-IF (DCR) for receiver in terms of silicon area and silicon cost for 0.18 um process, presented in Table 2.2. It was used \$ 0.10/mm^2 for production quantities cost estimation.

Table 2.2 - Rx architecture cost

Cost Parameters	Low IF RX	Zero IF RX
RF Front-End Area	0.9 mm^2	1.75 mm^2
IF Chain Area	1.6 mm^2	2.5 mm^2
RX Chip Area	2.5 mm^2	4.25 mm^2
RX Die Cost	\$ 0.25	\$ 0.425

Source: Notor, Caviglia and Levy (2003)

Therefore, although Zero IF presents a better performance, current chip sets are giving more importance to power consumption and die cost, consequently given preference for Low IF receiver architectures.

Kwon, Park, *et al*. (2012) present a more detailed analysis about transceiver RF Frontend. They compare the advantages and disadvantages of different approaches of low-power and low-cost systems seeking reduce the power consumption in the sleep and the active mode. The "References" column list several published works in which the respective approach was used. For instance, in the second line they referenced five works that used Scaling Down CMOS approach that enhance the respective advantages and disadvantages columns. Regulator for sleep block, RC oscillator, current bleeding mixer, stacked VCO, passive wake-up block, quick start oscillator, and LNA with negative "gm" blocks were implemented with focus on low power. As result an ultra low power transceiver was achieved.

The main considerations and techniques taken into account are summarized in Table 2.3.

Table 2.3 - Advantages and disadvantages for low-power and low-cost systems

	References	**Advantages**	**Disadvantages**	**(KWON, PARK, et al., 2012)**
CMOS approaches	Scaling Down: (BAKER, 2005) (LEE, 1998) (MARK, 2010) (PHAN, KIM, *et al.*, 2005) (LEE, JANG, *et al.*, 2007)	• ft increases • VDD decreases • Low Power	Hard to meet the standard specification using the low VDD	0.18 um
	Thick Metal Layer: (ABIDI, POTTIE and KAISER, 2000)	Sheet resistance decreases -> high Q	Cost increases	In use at inductor
Circuit approaches	Weak inversion: (SHAMELI and HEYDARI, 2006) (LIN, SANCHEZ, *et al.*, 1998) (ELMOURABIT, LU and PITTET, 2005)	Low power	Poor frequency response	In use at LNA and RC-OSC
	MTCMOS: (JIAO and KURSUN, 2010)	Low power	Cost increases	Not in use
	Negative Gm: (ALLAM, MANKU and MARSY, 1996)	High Q at inductor -> low power	Complicated tuning	In use in LNA
	Current reuse: (ZHENG, YAO, *et al.*, 2009) (KARANICOLAS, 1996)	Low power	• High noise • Headroom decreases	In use at VCO and DIV2
System approaches	Digitized receiver using SD-ADC: (KWON, PARK, *et al.*, 2008) (PHILIPS and PETER, 2004)	• Multi-standard • Low power	Not good to protect from interferes	Low IF
	Subsampling: (JAKONIS, KALLE, *et al.*, 2005) (DEVRIES and MASON, 2008)	• Multi-standard • Low power	• High noise • High up-conversion of phase noise	Low IF
	Polar transmitter: (ZHUANG, WAHEED and STASZEWSKI, 2010)	• Multi-standard • Low power	Complicated control	Zero IF
	Wake-up: (HAKKINEN and VANHALA, 2008) (DRAGO, SEBASTIANO, *et al.*, 2009) (HUANG, RAMPU, *et al.*, 2010) (PLETCHER, RABAY and GAMBINI, 2009)	Low power	Wake up by the interferers	In use
Operating approaches	Sleep mode: (JURDAK, RUZZELI and O'HARE, 2010)	Low power	• Impossible to quick response • Required additional circuits (RC, OSC, regulators…)	In use

Source: Kwon, Park, *et al.*(2012)

To finish, Kwon, Park, *et al.* (2012) compare their performance with others CMOS transceivers and the results are shown in Table 2.4.

Table 2.4 - Performance comparison of CMOS transceivers

	Arch. (RX/TX)	Power Consumption (RX/TX/sleep)	Sensitivity	RX		TX/DA	Die size (mm2)
				LNA	Mixer		
(KWON, BYUN, *et al.*, 2009)	Low IF / Direct modulation	25.74mW 30.06mW 1.44uW	-95dBm	Cascode with negative gm	Current reuse mixer	Differential common source topology with off chip inductor	7.84[3]
(NAM, CHOI, *et al.*, 2007)	Low IF / Direct modulation	22.3 mW[1] 18 mW[1]	-94dBm	Gm boosted LNA	Gilbert cell current reuse LNA and mixer	-	5.125
(RAJA, CHEN, *et al.*, 2010)	Low IF / Zero IF	10.8mW[2] 16.2mW[2]		Common source with resistive load	Gilbert Cell	External inductor load	3.61
(EO, YU, *et al.*, 2007)	Low IF / Zero IF	32.4mW[1] 30.6mW[1]		Single ended sascode LNA with inductive source degeneration	Gilbert Cell	Class AB power amp. external inductor	6.5
(BALANKUTTY, YU, *et al.*, 2010) [4]	Dual mode / -	32.5mW -		Single ended cascade LNA	Gilbert Cell		2.9
(KLUGE, POEGEL, *et al.*, 2006)	Low IF / Direct modulation	26.46mW 28.26mW 3dBm output	-101dBm	Stacked LNA	Passive switching pairs	Class AB power amp. With on-chip LC	5.77
(RETZ, SHANAN, *et al.*, 2009)	Zero IF / Direct Modulation	30.24mW 32.4mW	-96dBm	Common gate LNA	Passive current mode quadrature mixer	-	5.9
(NGUYEN, KIM, *et al.*, 2007) [5]	Zero IF / -	20.7mW[1] 40.5mW[1]		Single ended cascade	Balanced passive mixer	-	10
(SEO, MOON, *et al.*, 2007) [5]	Zero IF / -	25.2mW[1] 28.8mW[1]	-98dBm	Current reuse complementary technique without inductor	Gilbert cell	Differential common source topology with off chip inductor	3.96
(KWON, PARK, *et al.*, 2012)	Low IF / Zero IF	18.36mW[1] 23.58mW[1] 1.08uW[1] 0dBm output	-101dBm	Cascode with negative gm	Current reuse mixer	Differential common source topology with off chip inductor	7.84[3] 3.96

[1] Not include modem

[2] Not include modem and PLL

[3] Including MCU and flash memory

[4] 90 nm process, 0.6 V

[5] 915 MHz

Source: Kwon, Park, *et al.*(2012)

2.3.2 Converters

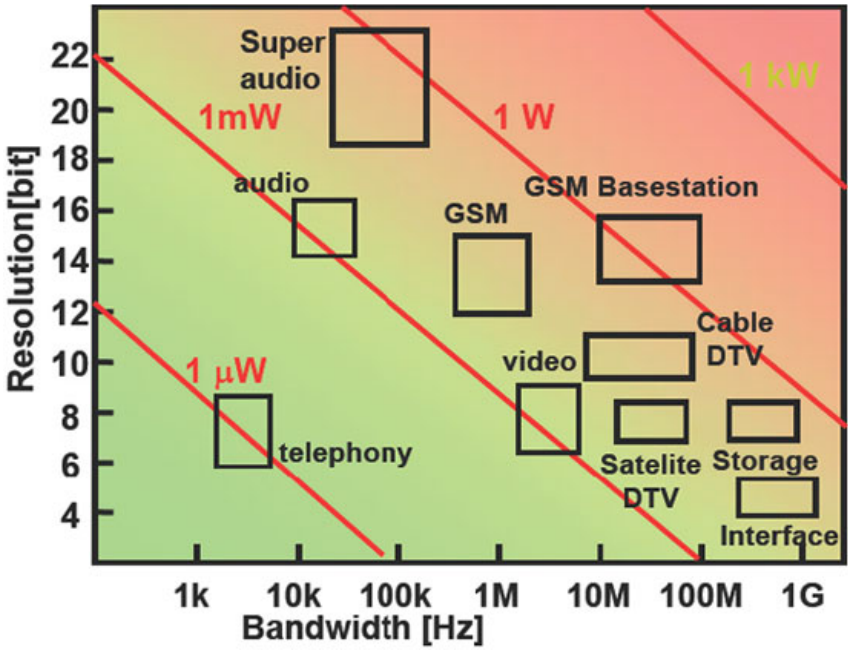
In complex systems and in portable applications the main architectural decisions of converters are often determined based on bandwidth, resolution and power available.

For DAC, Resistors Chain is the commonly chosen architecture for short bandwidth and low-resolution transceivers due to its stability and power consumption. Current Steering is another option when high speed and high resolution is required. Although it has the same advantages of the previous, Capacitor's Switches introduce switching noises to the signal. For this reason it is avoided in RF applications (SHE and ISMAIL, 2002).

Nevertheless, all DAC architectures for transceivers are quite simple and, compared to the RF Frontend, they do not influence in the transmitter power dissipation (most of them consumes in order of "uW").

ADCs, on the opposite, have complex architectures. The power consumption varies sharply according to topology, resolution and bandwidth. Figure 2.13, presented by Pelgrom (2010), illustrates this dependency through the projected power dissipation according to resolution and bandwidth of ADCs.

Figure 2.13 - Projected power dissipation (1pJ/bit)



Source: Pelgrom (2010, p. 427)

Therefore, choosing the correct ADC architecture that meets to the application requirements is mandatory. For IEEE 802.15.4 the main requirements are BW = 2 MHz, low power, and the minimum resolution required by digital baseband for carrier synchronization.

From Table 2.5, extracted from Pelgrom (2010) which summarizes the main ADC topologies and specifications, it is clear that Successive approximations and Sigma-delta are the two topologies that most fit to the standard. It can not be neglected, however, that in the near future multi-standard transceivers will be a reality. This means that a single ADC will operate with different bandwidth and resolutions. Therefore, choose the most versatile ADC topology that still accomplishes the low-power requirements of the standard, results not in a technical but market advantage. For this reason, the Sigma-Delta ADC was chosen instead of SAR.

Table 2.5 - ADC topologies and specifications

Type of analog-to-digital converter	Clock cycles for N bit conversion	Specification
Full-flash converter	1	Very fast BW = 1GHz, N < 6-8, power hungry
Folding converter	1	N < 8, 9
Pipeline	N	N < 12-14, fast BW = 10 – 200 MHz, efficient, latency of > N clock cycles
Successive approximations	N	Compact, BW = 2 – 5 MHz, N <12, low power
Sigma-delta	20 – 50	N up to 24, BW = 100 Hz – 5 MHz
Dual-slope	2^N	N = 14 – 20, BW = 10 kHz

Source: Pelgrom (2010, p. 423)

Scolari and Enz (2004) compare three different architectures of sigma-delta ADC for IEEE 802.15.4 standard in order determine which better fits for the application: Direct conversion, Low IF, and Low IF with quadrature band-pass.

Direct conversion is the simplest because of the absence of IF and, therefore, any image frequency. This results in reduced power consumption and high integration. The disadvantages are a strong DC component caused by self-coupling of the LO signal occurring at the mixer input and flicker noise.

Low IF with Low-Pass sigma delta presents no flicker noise and the intermediate corner frequency (frequency at which the flicker noise is equal to the white noise – fc) of IF can reduce the noise power. The count is that the “fc” can not be chosen too high because the quantization noise of the Sigma-Delta starts to degrade the SNR.

The last one is the Low IF with quadrature band-pass Sigma-Delta. It avoids the quantization noise and flicker noise but it is more sensitive to the mismatch of *I* and *Q* signals.

Therefore, any of the last two could be used if countermeasures for their imperfections

are predicted.

Until now the bandwidth and the best ADC topology for low power is defined. The last parameter is the resolution.

The resolution of an ADC implies in the quantization noise added to the signal that propagates to baseband. Determine the minimum resolution depends on the minimum SNR the baseband supports to succeed in the signal recovery. The SNR consist not only from the noise of an ADC but also from channel and the RF frontend according to the Equation 2.2

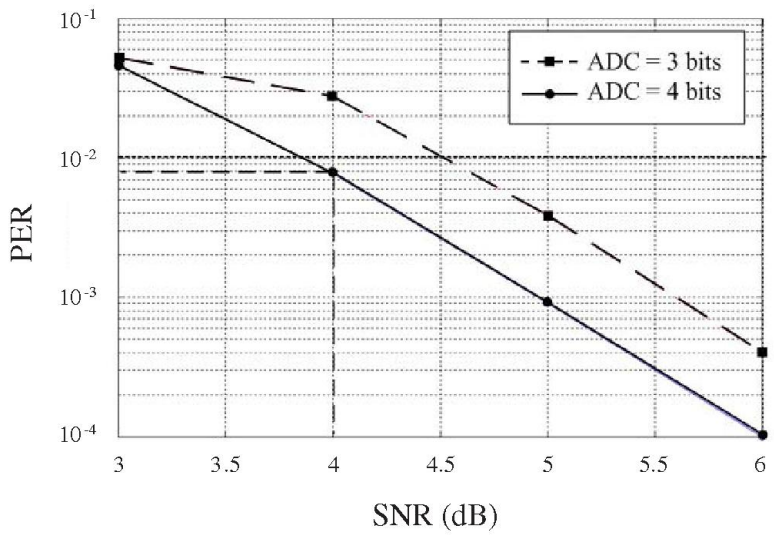
$$SNR = \frac{P_{signal}}{W_{channel+radio} + W_{adc}} \tag{2.2}$$

Where:

- P_{signal} = Signal power
- $W_{channel}$ = Noise power introduced by channel
- W_{adc} = Noise power introduced by ADC

To define the ADC output bit number (N), Wang, Huang, *et al.* (2006) simulate their proposed transceiver architecture varying the N of the ADC and plotting the SNR vs. Packet Error Rate (PER) curves for each N, shown in Figure 2.14. Therefore, for a PER of 1% their digital baseband requires at least 4 bits for a SNR of 4 dB. Since digital baseband SNR robustness is singular to the architecture, a similar simulation is recommended to determine the minimum ADC resolution.

Figure 2.14 - Resolution requirement of the ADC for Digital Baseband



Source: Wang, Huang, *et al* (2006)

2.3.3 Baseband

The baseband is the responsible for the carrier recovery, despreading and transmit the packet information (MPDU) to MAC layer. For IEEE 802.15.4 standard the most complex function is the correct synchronization. Since the frequency error caused by clock variations between transmitter and receiver might vary 10% of the bandwidth, ±200 kHz, and the low power application requires low complexity, a robust and simple algorithm becomes mandatory.

Synchronizers comprise estimation and recovery processes. The first is commonly executed in digital domain. Recovery, on the other hand, can be done on analog, through feedback the estimation to compensate in the VCO, as implemented by Wang, Huang, *et al.* (2006), or in digital, through inner product of income signal and the signal generated with the frequency error.

Although digital correction might lead to a bigger area, it is a trend nowadays to push signal processing to digital. The main reason is to avoid parameters variations in analog circuit components caused by corners, temperature and supply voltage, and process variation in fabrication.

Mengali and D'Andrea (1997) present a collection of estimation algorithms for linear modulator and continuous phase modulation for the three synchronizers: frequency, phase and timing. Table 2.6 presents some algorithms applicable to IEEE 802.15.4 standard and their main advantages and disadvantages.

Table 2.6 - Synchronization algorithms performance

	Algorithm	**Advantages**	**Disadvantages**
Frequency Estimation	Data-Aided	High precision	Low operation range or high SNR required
	Decision-Directed	Simple implementation	Low precision and high SNR required
	Delay-and-multiply	Robust to low SNR and high operation range	Low Precision
Phase Estimation	Data-Aided	High precision, robust to low/intermediate SNR, and low complexity	As SNR increases, precision is degraded which might require long observation length
	Decision-Directed	High precision	Intermediate to high SNR required
	Ad Hoc Feedforward	Robust to low SNR	Medium precision

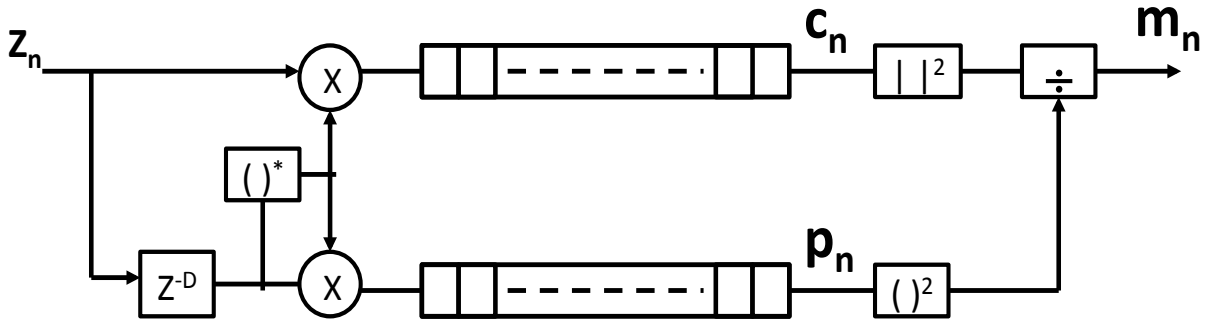
Timing Estimation	Decision-Directed	Low SNR, good tracking and high precision	Long pulses required, have false locks and it is complex implementation
	Feedforward	Short pulses, low SNR and low complexity	Poor tracking and medium precision
	Feedback	Short pulses, no false locks, low SNR and low complexity	Poor tracking and medium precision

Source: Mengali and D'Andrea (1997)

From the Table 2.6, it is clear that there will always be trade-off between any of those algorithms. Moreover, the choice of any of those algorithms, as they are, will not lead to the best solution. As it is described in next paragraphs, the combination of some of those in a practical hardware produces a higher performance.

Targeting OFDM LANs, 802.11 more specifically, Heiskala and Terry (2002) present a simple method for packet detection called "delay and correlate" developed by Schmidl and Cox (1996), which imply the Delay-and-Multiply with extra features. The method is based in two sliding windows *C* and *P*, as shown in Figure 2.15. *C* window is the cross-correlation between received signal and a delayed version of the received signal. The delay z^{-D} is equal to the period of the preamble. The *P* window calculates the received signal energy during cross-correlation window and it is used to normalize the decision statistic.

Figure 2.15 - Delay and correlate architecture



Source: Heiskala and Terry (2002, p. 55)

From Figure 2.15, the Equation 2.3 and Equation 2.4 are extracted to calculate the value of c_n and p_n respectively. Note that the "*" means complex conjugate and Z^{D} means the delay in digital signal processing. In the equations, *L* means the window length.

$$c_n = \sum_{k=0}^{L-1} z_{n+k} z_{n+k+D}^*$$

(2.3)

$$p_n = \sum_{k=0}^{L-1} z_{n+k+D} z_{n+k+D}^* = \sum_{k=0}^{L-1} |z_{n+k+D}|^2$$

(2.4)

The decision statistic m_n is calculated from Equation 2.5.

$$m_n = \frac{|c_n|^2}{(p_n)^2}$$

(2.5)

When the received signal consists of only noise, the output of c_n of the delayed cross-correlation is zero-mean random variable. Once the start of the packet is received, m_n jumps quickly to its maximum value.

In addition, using same structure and adding the expected preamble, t_k, the algorithm becomes a symbol timing estimation, as shown in Equation 2.6.

$$t_s = arg\left\{ \max_n \left| \sum_{k=0}^{L-1} z_{n+k} t_k^* \right|^2 \right\}$$

(2.6)

The value of *n,* which corresponds to maximum absolute value of the cross-correlation, is the symbol-timing estimate.

Also, the length of *L* of the cross-correlation determines the performance of the algorithm. Larger values improve performance, but also increase the amount of computation required.

Based in TDMA applications, Classen, Meyr and Sehier (1993) merged the Delay-and-Multiply with Data-Aided algorithms and proposed a method in which timing estimation from Equation 2.6 and frequency estimation can be performed simultaneously if the preamble exhibits some kind of periodicity. Equation 2.7 and Equation 2.8, resulted from this method, calculates the start of frame and frequency error estimation respectively.

$$\dot{n} = \max_{n} \left\{ \left| \sum_{k=1}^{L-1} [z_{n-k} z_{n-k-D}^{*}] d_n \right| \right\} \tag{2.7}$$

$$\emptyset = \frac{1}{D} \arg \left\{ \left| \sum_{k=1}^{L-1} [z_{n-k} z_{n-k-D}^{*}] d_n \right| \right\} | n = \dot{n} \tag{2.8}$$

Where:

- $\emptyset$ is the frequency error
- D is the delay window
- d_n is the inner product of preamble with the preamble delayed (windowed)
- $\dot{n}$ is the timing estimation
- L is the number of frames in the preamble

Moreover, the probability of an incorrect frame synchronization is less than 10^{-5} for AWGN SNR >= 3 dB and the structure provides a robust synchronization over a Rician fading channel (multipath channel model) if the estimation length is small with respect to the inverse coherence bandwidth of the fading process (CLASSEN, MEYR e SEHIER, 1993).

To conclude this subsection, from structure presented by Heiskala and Terry (2002) and the method proposed by Classen, Meyr and Sehier (1993), Chen and Ma (2008) developed a 1.8 mW baseband processor for IEEE 802.15.4. The biggest advantage of such architecture is to merge packet detection, symbol timing, and frequency estimation in a single block. Equations 2.9-2.12 and Figure 2.16 detail the method. Also, the fix-point implementation by Chen and Ma (2008) is robust to SNR down to 4.5 dB.

$$C_n = \sum_{i=0}^{L-1} | z_{n-i} z_{n-i-D}^{*} | \, d_i \tag{2.9}$$

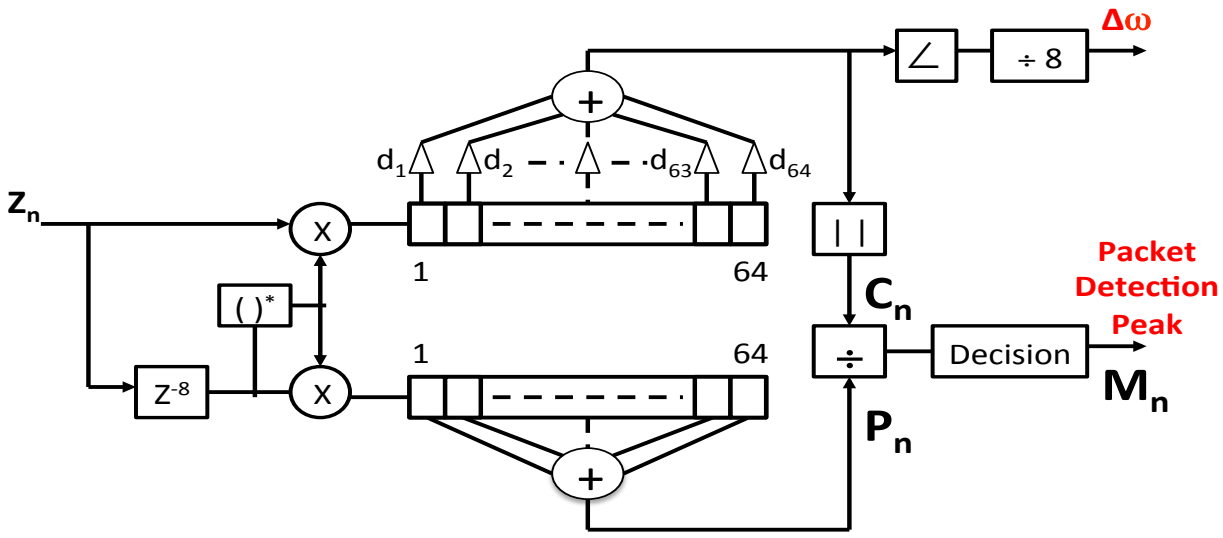
$$P_n = \sum_{i=0}^{L-1} | z_{n-i-D} |^2 \tag{2.10}$$

$$M_n = \left(\frac{|C_n|}{P_n} \right)^2 \tag{2.11}$$

$$d_i = p_i p_{i+D}^*$$

(2.12)

Figure 2.16 - Packet detector, timing and frequency estimation



Source: Chen and Ma (2008)

2.3.4 Adaptive Architectures

From previous subsections it is clear that much effort was spent in the RF Frontend, Converters and Baseband leaving few margin for improvement. Moreover, all transceivers architectures seen until now were designed to the worst condition and become overdesigned for a less constrained environment. Therefore, adaptive system becomes an important player for those who seeks bigger transceiver power reduction. The goal of next paragraphs is to explore a few of adaptive architecture proposed in several baseband fields.

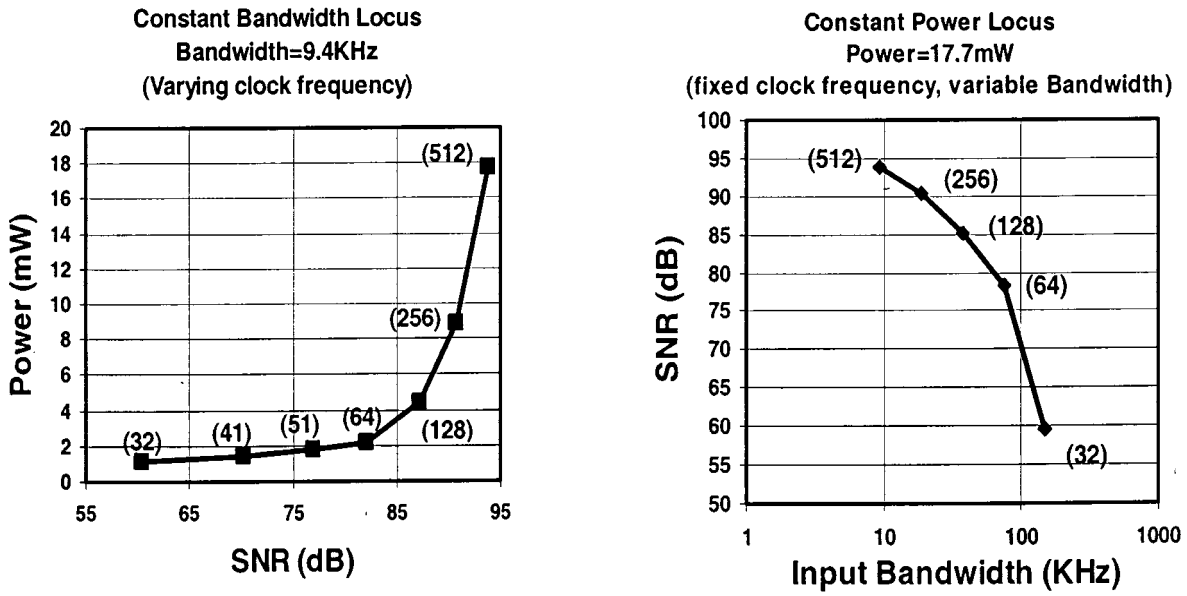
In RF Frontend and ADC field, Oguz, Morch and Dehollain (2011) analyze the reconfiguration strategy and average power dissipation reduction in a direct-conversion IEEE 802.15.4 receiver. High-level power models are built for the Low Pass Filter and a SAR ADC. The trial-and-error solver in Oguz, Morecho, *et al.* (2010) finds the filter Signal Noise and Distortion Radio (SNDR), the filter order, and the ADC SNDR combination that minimizes the total power dissipation for a given operating condition. The optimum is reached with a first-order-filter together with a reconfigurable ADC with SNR between 21 dB and 69.8 dB (ENOB of 3.2 and 11.3 bits).

The necessity for adaptive ADCs for multiple applications, especially in Software Radio, emerges recently. Veldhoven and Roermund (2011) discuss flexible Sigma-Delta ADCs for multiband devices using multiple oversampling rate (OSR). It presents a scalable

modulator and the relationship with the RF Frontend for Wireless and Cellular applications to achieve a scalable bandwidth. To configure the bandwidth it uses defined integrators capacitors for each OSR frequency the converter will operate. This keeps the signal gain without interfering in the converter stability.

Although it was published 10 years earlier, Gulati and Lee (2002) goes further and target in a reconfigurable ADC converter in which topology, resolution, and current bias are the variables. The topology is configured between Pipeline and Sigma-Delta allowing the achievement of a wide operation range. Capacitors size, pipeline length, and OSR are others configurable parameters. Also, bias current of the operational amplifier is adjusted according to the sampling frequency. Such architecture is capable to operate from 0 to 10 MHz of bandwidth and has a resolution range from 6 to 16 bits. For full resolution, a Sigma-Delta topology is used in a 10 MHz frequency, 9.4 kHz of bandwidth, and OSR of 512. The power consumption in this mode is 17.6 mW. In pipeline mode, 24.6 mW is achieved for 2.62 MHz and 11 resolution bits. The core area is 5.5 mm^2 for 0.6 um CMOS process. Figure 2.17 illustrates the power vs. SNR and the SNR vs. Bandwidth according to OSR.

Figure 2.17 - OSR and SNR effects in ADC power consumption

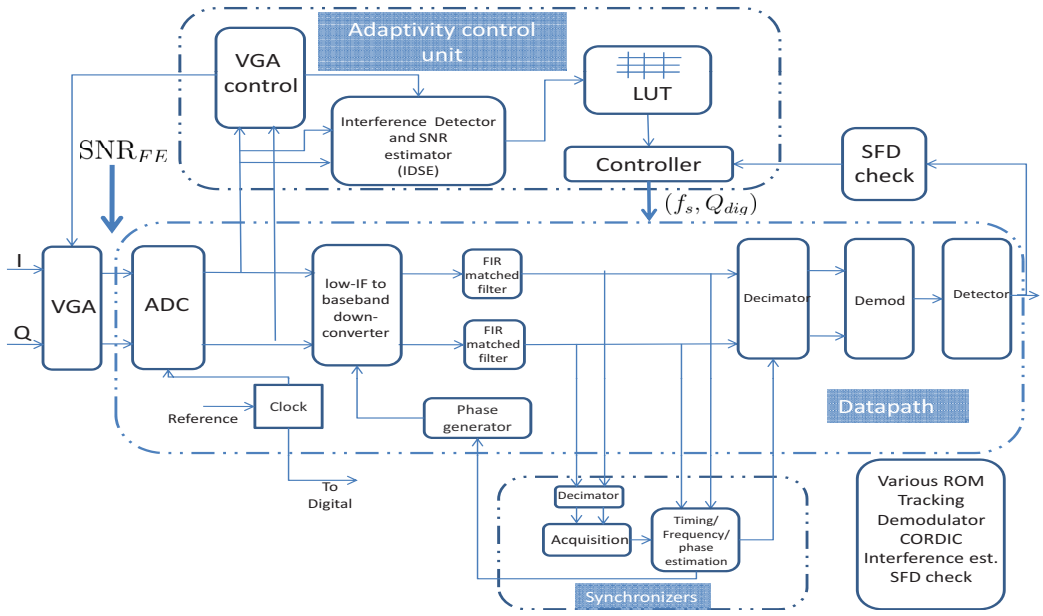


Source: Gulati and Lee (2002)

In the digital baseband, Dwivedi, Amrutur and Bhat (2011) designed power scalable digital baseband for a Low-IF receiver for IEEE 802.15.4 standard. The bit width is used to reduce the power under favorable signal and interference scenarios, thus recovering the design margins introduced to handle the worst-case conditions. The architecture, illustrated in Figure 2.18, uses a SNR estimator and interference detector (IDSE), variable tap and variable

coefficient FIR filter, an adaptive control unit, and an adaptation procedure to achieve up to 85% of power reduction.

Figure 2.18 - Adaptive receiver based in signal SNR



Source: Dwivedi, Amrutur and Bhat (2011)

The cost of adaptive architecture is 16% of the design area. It consumes 10 mW in synchronization and 2.49 down to 0.49 mW in the average for 256-packet size, according to the environment condition. Also, the process used was 0.13um, which gives scaling advantage in dynamic consumption compared to other references. The counter side of this architecture is the lower probability of synchronization acquisition at poor SNR caused by absent of buffered data on synchronization unit.

In summary, this chapter described the specifications of IEEE 802.15.4 standard, the transceiver main parts and architectures proposed by academy to reduce power consumption. In the high-end research are the adaptive architectures based in the LPF, ADC operation range and resolution, digital baseband data width, and income packet's SNR. None of them, however, combines the adaptive ADC resolution with a SNR robust digital baseband to decrease the converter power in a lower constraint environment. This blank research space leads to the current work proposal discussed in chapter 3.

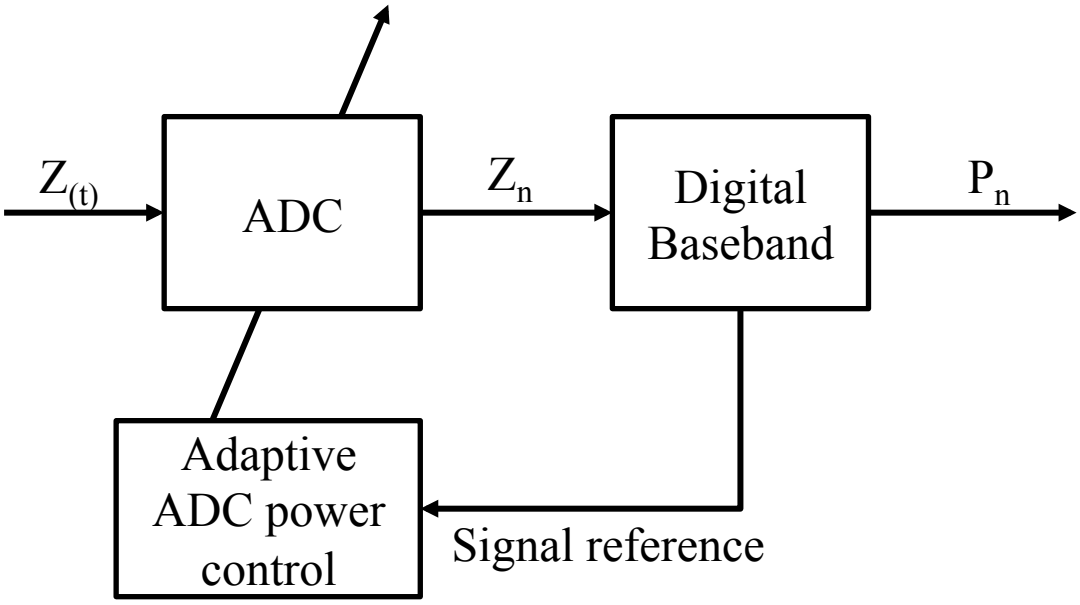
3 ADAPTIVE RECEIVER ARCHITECTURE

Chapter 2 described the specifications of IEEE 802.15.4 standard and the three parts of transceiver exploring topologies and architectures proposed in published articles and books. As it was mentioned, the most used transmitter architecture is direct-conversion. Also, its main power dissipation is driven by the Driver Amplifier to increase the signal power to antenna. Therefore, most of proposals to reduce transmission power are targeted to receiver.

In addition, RF Frontend, ADC, and digital baseband architectures for WPAN applications were deeply investigated in the past 10 years, requiring huge effort nowadays to achieve significant improvements. As alternative, adaptive architectures according to system characteristics and environment become the preferred research spot.

The current work joined the relationship of SNR and power of ADC explored in Dwivedi, Amrutur and Bhat (2011) with the baseband introduced in Chen and Ma (2008) to present a simple, power efficient low SNR robust system adaptive receiver architecture. ADC converters, O-QPSK baseband architecture, adaptive ADC power control block and a reference feedback signal compose it. Figure 3.1 illustrates the top-level block diagram. As can be observed, the architecture does not cover the RF Frontend part, being restricted to converters and baseband.

Figure 3.1 - Adaptive ADC resolution architecture



Source: The author

In the figure, $Z_{(t)}$ is the continuous time output of Frontend RF signal that is converted

to digital domain, Z_n. Digital Baseband calculates the LQI, recover the carrier and despread the signal to send the PSDU, P_n, to MAC layer. The Adaptive ADC power control sets the ADC resolution according to SNR value of *signal reference*.

In receiver wake-up, the ADC starts operation with full resolution and digital baseband search for a valid packet. If the preamble is detected, digital baseband estimates the input signal SNR, during LQI calculation, and feedback the value to Adaptive ADC power control. According to a pre-defined LUT that relates the quantization noise added to signal by ADC resolution, and the SNR of Z_n, the control block acts in the ADC to adjust the output resolution to achieve the minimum signal SNR supported by digital baseband.

Next sections detail the three blocks covering topology: architecture, system modeling and simulation in Matlab tool (MATHWORKS, 2011).

3.1 Analog-to-Digital Converter

Subsection 2.3.2 exposed some ADC topologies and their specifications. Two of them fit better to the IEEE 802.15.4 standard requirements: Sigma-Delta and SAR.

Although SAR could lead to less ADC power consumption, its operation range in terms of bandwidth and resolution would limit the proposed solution application for other standards. Sigma-Delta ADC, on the other hand, is more versatile due to a wider bandwidth and resolution, mandatory characteristics to be used in multi-standards transceivers. Next paragraphs present an architecture overview of the last including the ADC parameters used.

3.1.1 Sigma-Delta ADC Architecture Overview

Sigma-Delta contains a comparator, voltage reference, a switch, one or more integrators and summing circuits, and a digital low pass filter.

A perfect classical N-bit sampling ADC has an *rms* quantization noise of $q/\sqrt{12}$ uniformly distributed within the Nyquist band of *dc* to $f_s/2$, where q is the value of LSB and f_s is the sampling rate (BAJDECHI e HUIJSING, 2003).

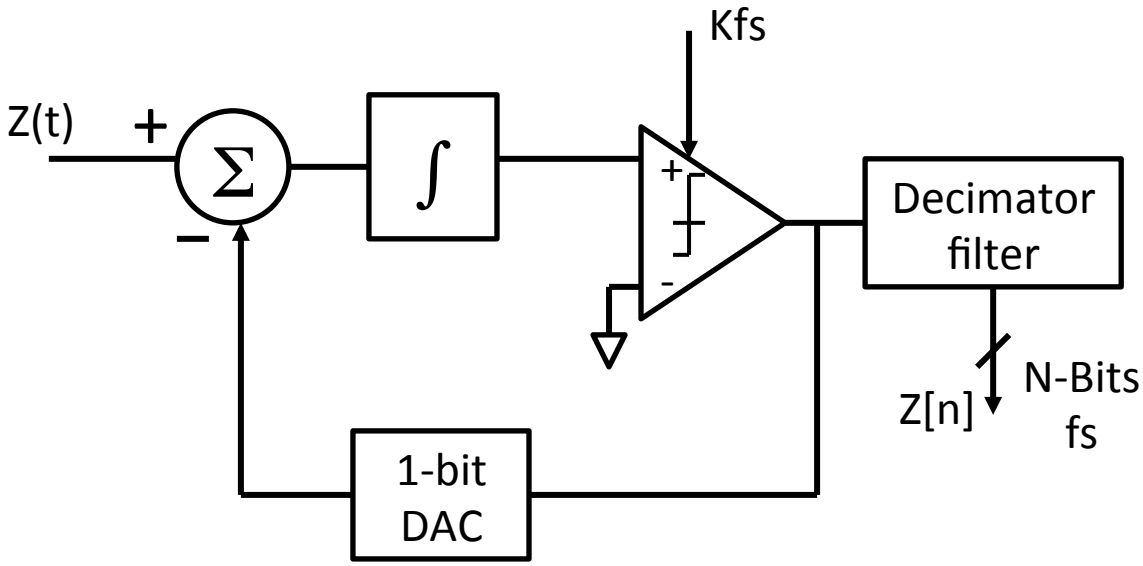
Therefore, its SNR with full-scale sine wave input will be *(6.02N + 1.76dB)*. Also, the ADC imperfections make its noise greater than theoretical minimum quantization noise, resulting in effective resolution lower than N-bits. Equation 3.1 defines the Effective Number of Bits (ENOB):

$$ENOB = \frac{SNR - 1.76dB}{6.02dB} \tag{3.1}$$

For a much higher sampling rate, Kf_s, the *rms* quantization noise remains $q/\sqrt{12}$, but the noise is distributed over a wider bandwidth *dc* to $Kf_s/2$. If a digital low pass filter is applied to the output, much of quantization noise is removed without affecting the desired signal, improving the ENOB. The factor *K* is referred as Oversampling Ratio (OSR). Another advantage of oversampling is the requirements relax of analog antialiasing filter.

Since the digital output filter reduces the bandwidth, the output data rate may be lower than the original sampling rate and still satisfy the Nyquist criterion. This may be achieved by passing every Mth result to the output and discarding the remainder. The process is known as "decimation" by a factor *M*. *M* can have any integer value, provided that the output data rate is more then twice the signal bandwidth.

Figure 3.2 - First order Sigma-Delta ADC modulator



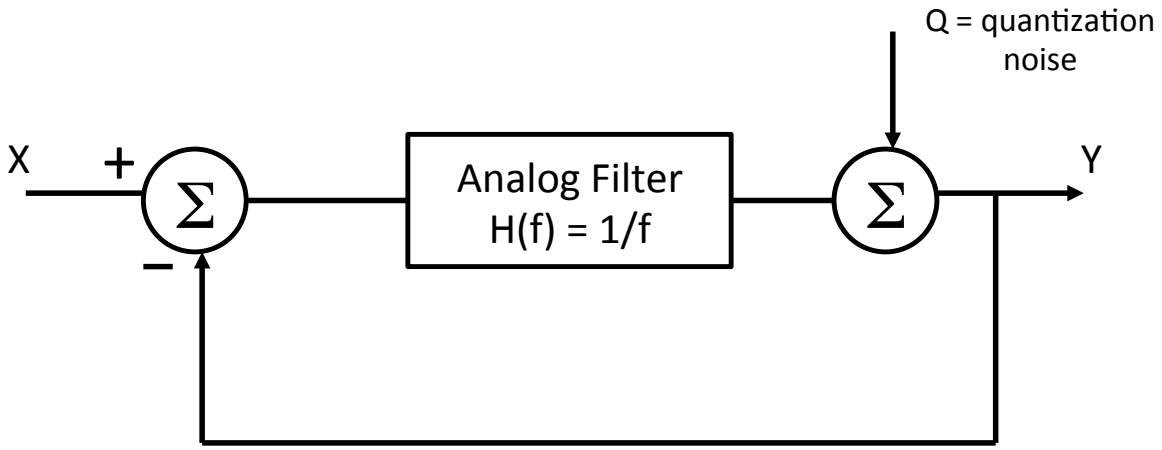
Source: Kester (2008, p. 6)

To enlighten the Sigma-Delta operation, assume a dc input $Z_{(t)}$, illustrated in Figure 3.2. The integrator is constantly ramping up or down the input of comparator. The output of the comparator is fed back through a 1-bit DAC to the summing input. The negative feedback loop from the comparator output through the 1-bit DAC back to the summing point will force the average *dc* voltage in the DAC output to be equal to $Z_{(t)}$. The average DAC output voltage

is controlled by the *ones-density* in the 1-bit data stream from the comparator output. As the input signal increases towards the supply voltage, the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. The behavior is similar but opposite if the signal goes negative. Therefore, the average value of the input voltage is contained in the serial bit stream out of the comparator. This circuit is called "first-order modulator" because only one integrator composes it. The Decimation Filter processes the serial bit-stream and produces the final output data.

The concept of noise shaping is best explained in the frequency domain by considering the simple Sigma-Delta modulator model of Figure 3.3.

Figure 3.3 - First order modulator model in frequency domain



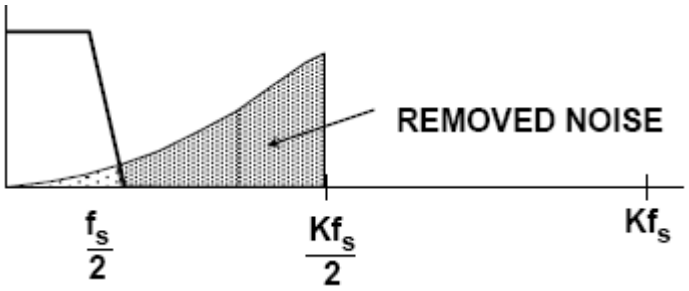
Source: Kester (2008, p. 8)

The integrator in the modulator is represented as an analog low-pass filter with transfer function of $H(f) = 1/f$. This transfer function has an amplitude response that is inversely proportional to the input frequency. The 1-bit quantizer generates quantization noise, Q, which is injected into the output-summing block. Equation 3.2 expresses the output model:

$$Y = \frac{X}{f+1} + \frac{Qf}{f+1} \tag{3.2}$$

Note that as the frequency f approaches zero, the output voltage Y approaches X with no noise component. At higher frequencies, the amplitude of the signal component approaches zero, and the noise components approaches Q. Figure 3.4 shows noise shaping effect and also includes the decimation filter cutting off the higher noise-frequencies.

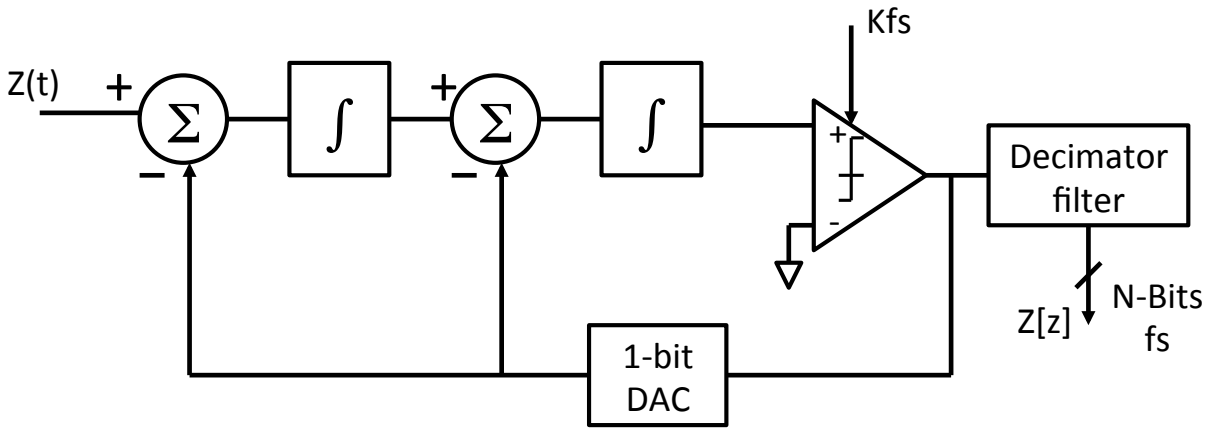
Figure 3.4 - Noise shaping and low pass decimator filter



Source: Kester (2008, p. 5)

By using more than one integration and summing stage in the modulator, higher orders of quantization noise shaping can be achieved and even better ENOB for a given oversampling ratio. Figure 3.5 illustrates a second order modulator.

Figure 3.5 - Second order Sigma-Delta architecture



Source: Kester (2008, p. 9)

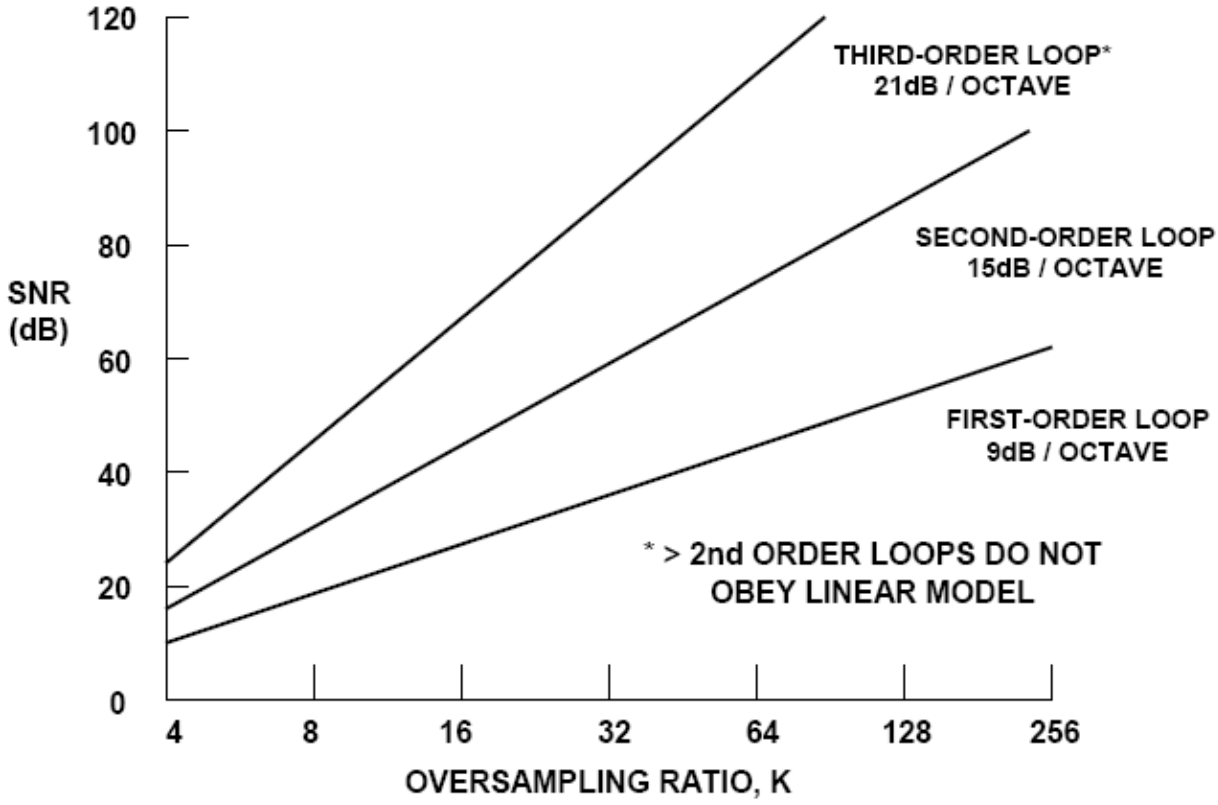
In addition, Figure 3.6 shows the relationship between the order of the modulator and the amount of oversampling necessary to achieve a particular SNR. For instance, if the OSR is 64, an ideal second-order system is capable of providing an SNR of about 80dB. This implies, according to Equation 3.1, approximately 13 ENOB.

Therefore, in sigma-delta analog to digital converters, the order of the modulator, the oversampling ratio, and the window of signal averaged in decimation filters deeply impact the converter SNR. This gives two alternatives to adjust the resolution according to SNR: dynamically increase and decrease the modulator order; change the OSR.

The dynamically adjustment of modulator order requires to set many parameters to avoid the block instability, which might be complex to implement. Changing the OSR, as

suggested by Veldhoven and Roermund (2011), is easier to implement and requires only adjust the capacitors values (the switch frequency in case of switched capacitors) in the modulator integrators to adjust the output gain.

Figure 3.6 - SNR, OSR, and modulator order relationship



Source: Kester (2008, p. 10)

Finally, the specification of ADC used is presented in Table 3.1.

Table 3.1 - Sigma-Delta ADC specification

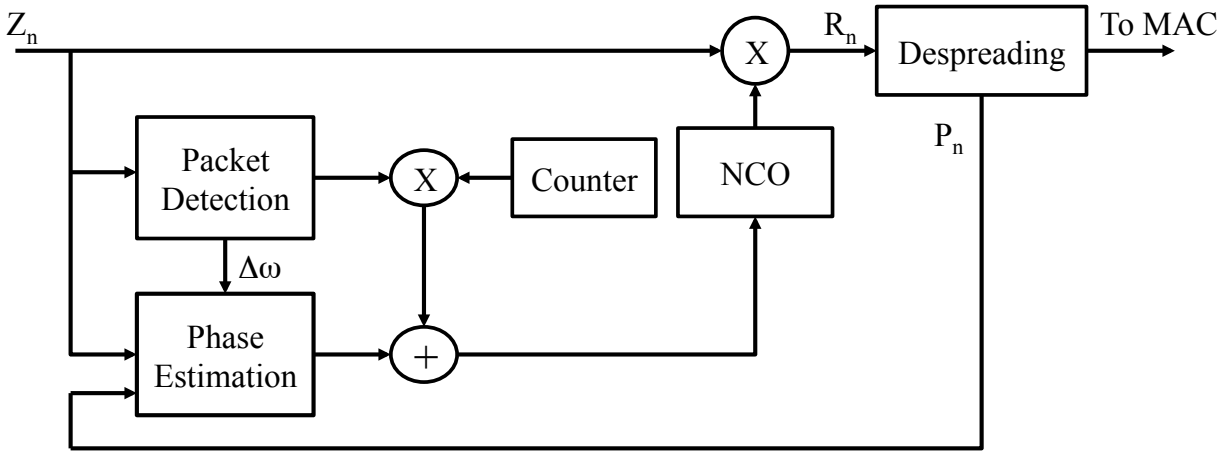
Modulator order	Second order
Maximum OSR	128
Decimation Filter topology	Third order sinc
Maximum Decimation Filter Ratio	16
Input bandwidth	1 MHz
Output sampling/rate	8 M samples
Maximum Output Resolution	7 bits
Modulator Power Consumption	1.8 mW
Decimator Power Consumption	1.55 mW

Source: The author

3.2 Digital Baseband

The digital baseband architecture, as already mentioned in the beginning of the chapter, is based in Chen and Ma (2008) proposal. Its advantages compared to others are the SNR robustness down to 3 dB, frequency operation of 4 MHz, and consumption of 1.8 mW, consequence of its simple and optimized algorithms. In subsection 2.3.3, only one part of the architecture was explained. In this section a top-level representation, illustrated in Figure 3.7, and remaining blocks functionality and architecture are detailed.

Figure 3.7 - Digital baseband processor architecture

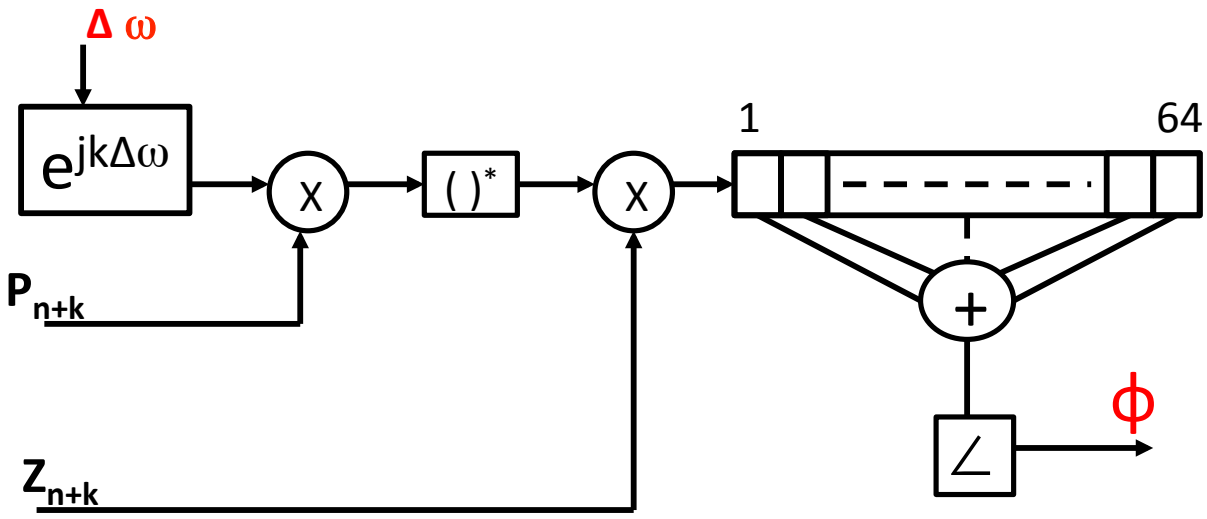


Source: Chen and Ma (2008)

After the receiver wake-up, only the Packet Detection block is active. Its function is to detect the preamble, to estimate the carrier frequency offset (Δω), and to determine the exact sample in which the symbol started – timing estimation. The start of preamble sample is found through a peak caused by a cross-correlation of input signal and preamble. Since there are 8 equals and successive symbols, the block produces up to 8 valid peaks, depending on the packet frame position in the instant the receiver wakes-up. The block considers a valid packet after three consecutive peaks, when it enables the remaining blocks and disables itself. For more detail of the algorithm and architecture of this block, please refer to subsection 2.3.3.

Phase Estimation block, illustrated in Figure 3.8, uses a preamble look-up table (P_{n+k}), a wave signal generator, multipliers, conjugate block, an average of 64 samples, and arctan function to track the phase of the input signal.

Figure 3.8 - Phase estimator block



Source: The author

After the Packet Detector enables the block, it generates a discrete wave with frequency of the carrier-offset estimation and calculates the inner product with the expected preamble value stored in the LUT. This multiplication adds in the expected preamble, P_{n+k}, the frequency error in opposite direction. Further it is multiplied by the input signal Z_{n+k} resulting in the residual frequency error that might be left in the previous block, usually no more than 2 kHz, and the phase error. The phase error estimation, Φ, is obtained from the argument of the average of 64 successive samples – frame number of a unique symbol.

Equation 3.3 presents the algorithm of phase carrier estimation.

$$\Phi = \arg\left\{\sum_{k=0}^{63} Z_{n+k}\left(P_{n+k}e^{j(k\Delta\omega)}\right)^*\right\} \tag{3.3}$$

At the same time, the frequency estimation is integrated through the counter block and added to the phase estimation. A signal with the frequency and phase errors is generated by NCO block and it is multiplied by the input signal Z_n. The signal produced, R_n, is the original signal modulated by transmitter.

The last block correlates and despreads R_n. The P_n feedback signal is generated by spreading the packet again and using a 4 row table to generate the half sin samples.

By the time the preamble has finished, P_{n+k} becomes the feedback of system output. Therefore, the packet contents, Z_{n+k}, need to be stored to computes with the same values that

have passed through the system and were spread again. In the switch time (preamble to packet) a discontinuity of the phase happens, but since the samples are calculated again, there is no impact in the synchronization.

3.3 Adaptive ADC power control

Previous section showed that decreasing the converter OSR, decreases the SNR and consequently the effective bit number. The advantage is the linear power reduction in the decimation filter and a non-linear in the modulator due to non-linear behavior of capacitance variation and power reduction.

The Adaptive ADC Power Control works as a feedback from digital baseband to selects the OSR and capacitances in ADC according to the digital reference, which can be BER or LQI. The first tracks the BER of each chip after preamble synchronization. Since the minimum hamming distance from one chip to another is 12, the maximum BER per chip tolerated to avoid PER is 6. The second reference, and suggested in current work, is the signal SNR extracted from LQI.

As already mentioned, the ADC starts using all output bits. If the SNR is higher than a pre-defined threshold, the OSR is reduced, saving power in the reception.

This architecture can be implemented using simple comparators to generate the command that configures the Sigma-Delta ADC.

Next section describes the model of the transmitter, the channel, the ADC, and the digital baseband. The goal, besides the certainty of the proper functionality of the system designed, is to extract the threshold values for the comparators.

3.4 System Model

Commonly used in IC design flow, system modeling is the easier and faster approach to validate any system architecture before spending much more effort in hardware architecture. Also, as complexity of systems increase, simulation time ramp up to skies and modeling might become the only feasible way to validate the proposed system before tape-out of IC.

This section, therefore, aims to validate the digital baseband architecture, the system with a sigma-delta ADC model, and extract the minimum ADC resolution for a given channel SNR supported by the digital baseband for a correct carrier recovery.

The transmitter, channel, and receiver models constitute the system model implemented. The subsequent subsections detail each model and the signal processing through the system. Further, simulations methods to validate the system are described. The last subsection analyzes the simulation results and concludes System Modeling section.

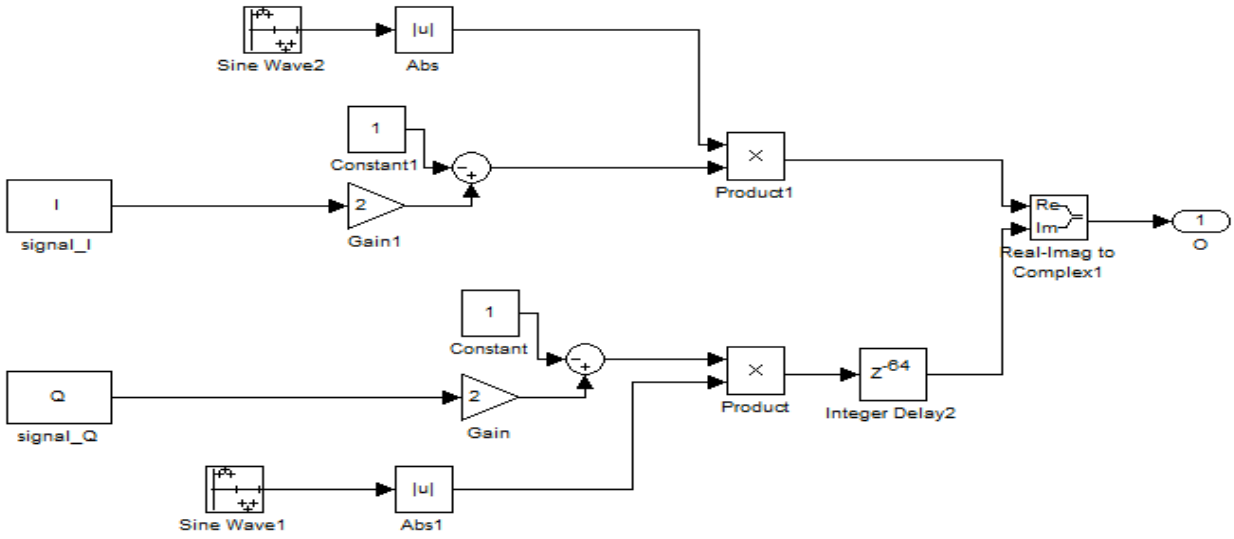
3.4.1 Transmitter Model

The transmitter model comprises a packet generator in Matlab files format and O-QPSK half-sin modulator in Simulink tool.

The packet generator creates the PPDU, which contains 4 preamble octets, 1 octet of SFD indicating end of preamble, 1 octet of PHR indicating frame length, and the payload PSDU – up to 127 octets. Further, it spreads each 4 bits into 32 bits according to the standard and saves in two Matlab variables, “I” and “Q”, depending if the bit index is even or odd.

The modulator uses the packet variables to generate half-sins and delayed the samples to become orthogonal signals, as it is shown in Figure 3.9.

Figure 3.9 - Transmitter model



Source: The author

Since “signal_I” and “signal_Q” are binary (zero or one), they are multiplied by two and subtracted by one to create the +1 and -1 of QPSK symbols. Further, the symbols are multiplied by absolute value of sine wave to generate the half-sin shape. Therefore, if the variable bit is zero, it becomes a negative half-sin, otherwise, positive half-sin.

The modeling of 2.4GHz modulator would lead to higher and unnecessary simulation time. Therefore, in order to emulate an analog signal for downstream analog converter

reception, 128 samples per half-sin were used. Finally, "Q" samples are delayed 64 time steps to create the quadrature signal of O-QPSK. Both signals form complex numbers, real and imaginary, and are transmitted to channel model.

3.4.2 Channel Model

AWGN channel, Phase/Frequency Offset, and Fractional Delay blocks comprise the channel model. All of them are built-in in Matlab Simulink tool.

The AWGN Channel block adds complex white Gaussian noise to the complex input signal producing a complex output signal. The block models the white noise as random numbers generated using the Ziggurat method (MARSAGLIA e TSANG, 2000). This block inherits its sample time from the input signal (15.625 ns).

There are 5 modes to define the amount of noise power added to the signal:

- Eb/No – the ratio of bit energy to noise power spectral density;
- Es/No – the ratio of signal energy to noise power spectral density;
- SNR – the ratio of signal power to noise power;
- Variance from mask – where a positive variance is specified;
- Variance from port – where a positive variance is provided as input port of the block.

Since it is the power signal ratio in the input of digital baseband that is being analyzed, SNR mode is the most appropriate method.

Phase/Frequency Offset block applies frequency and phase mismatches caused by channel or difference in oscillators frequency between transmitter and receiver. Therefore, if the channel input signal is *u(k)*, the output signal is:

$$y(k) = u(k)e^{j(2\pi f(k)+\varphi(k))} \tag{3.4}$$

Where,

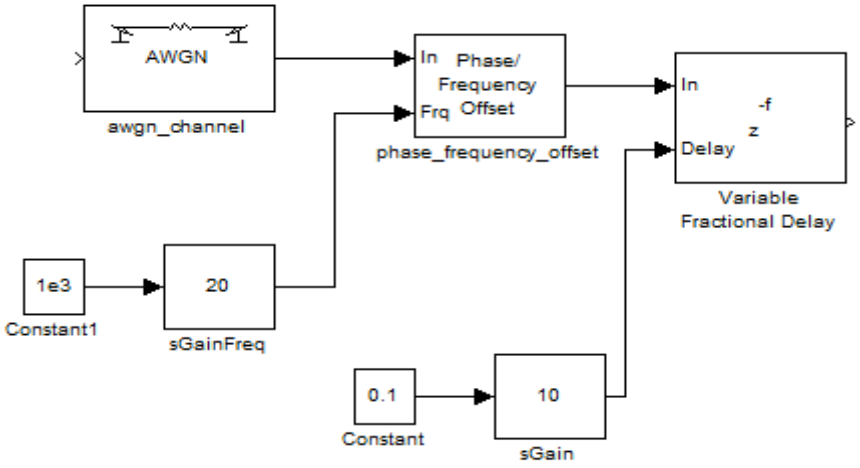
- $f(k)$ = Frequency offset
- $\varphi(k)$ = Phase offset

The Variable Fractional Delay block delays each element of the discrete-time N-D input array, *u*, by a variable number of sample intervals. In Farrow interpolation mode (FARROW, 1988), used in the channel model, the block stores the *Dmax+N/2+1* most recent

samples received at the input port for each channel, where N is the farrow filter length parameter. In the model, the value of 100 is set to Dmax and 4 for the filter length. The block is used to interpolate intermediate sample values according to delay Dmax used.

Figure 3.10 illustrates the Matlab channel model used.

Figure 3.10 - Channel model



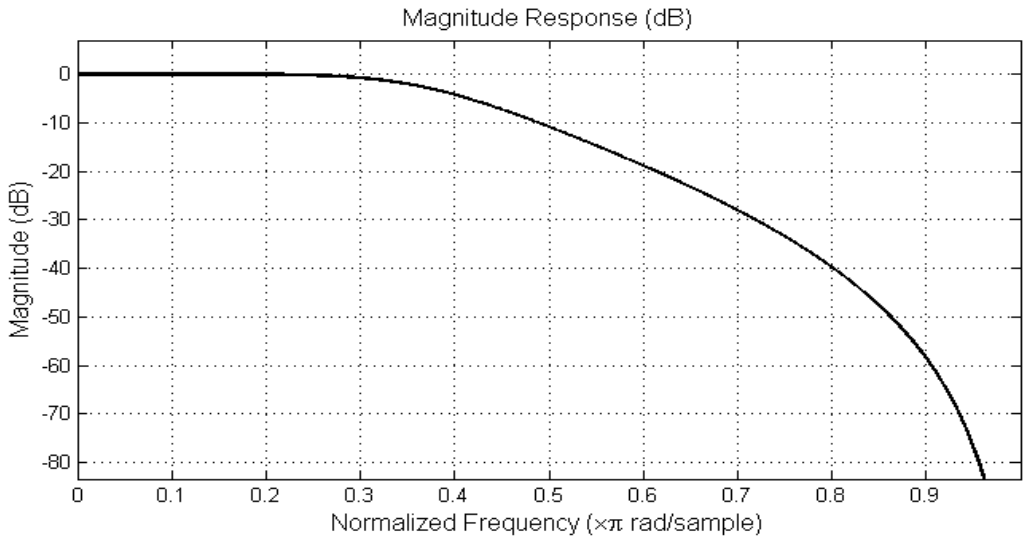
Source: The author

3.4.3 Receiver Model

Three models comprise the receiver: analog filter, sigma-delta ADC, and baseband model.

A biquadratic IIR filter that models the low pass filter used before ADC to reject part of the high frequencies remained after the signal passed to baseband. Figure 3.11 illustrates the filter amplitude response.

Figure 3.11 - Low-pass filter

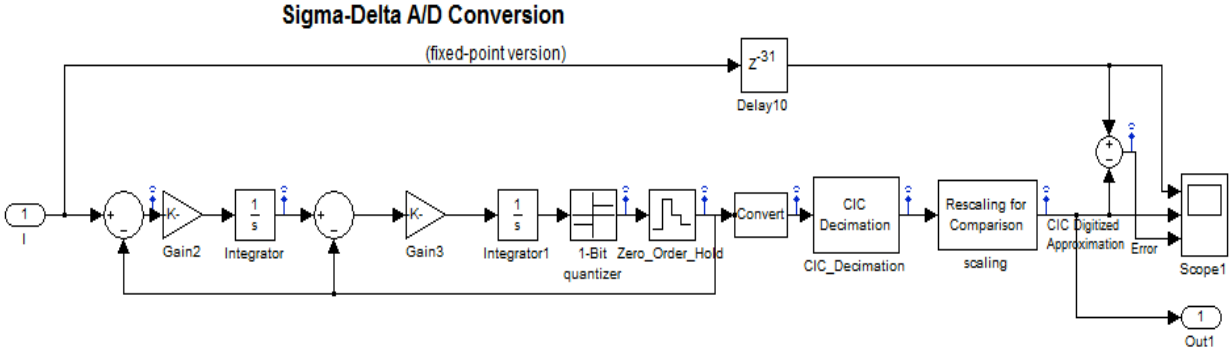


Source: The author

It can be seen from filter magnitude response that the -3 dB is located at 0.3π rad/sample, i.e. 19.2 MHz since the sample rate is 1 Msample/s leading to 64 MHz.

The ADC model is a second order converter and it is based in the one order Matlab Sigma-Delta model version. The gain values of converter modulator are set in the limit of its stability and saturation. The third order decimation filter uses a decimation factor of 16 and its section and output word length vary according to frequency of "Zero_Order_Hold" block, dictating the digital baseband input bus size. Figure 3.12 illustrates the ADC model.

Figure 3.12 - Sigma-delta ADC model

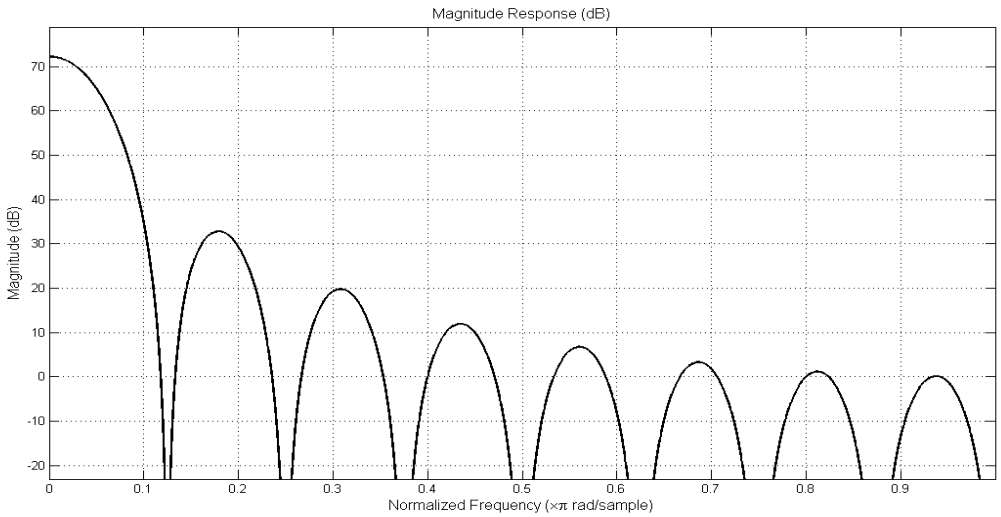


Source: The author

The "Rescaling for Comparison" block adjusts the output amplitude and "Scope1" plots the quantization error.

Figure 3.13 shows the CIC Decimation filter response for a decimation factor of 16.

Figure 3.13 - Decimator filter frequency response

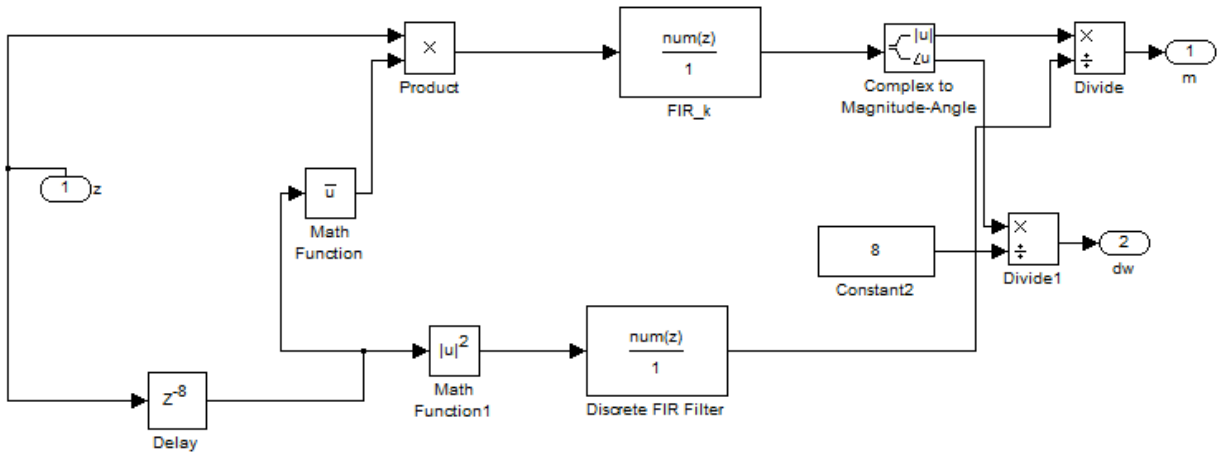


Source: The author

The baseband model comprises three blocks: Packet Detector, Phase Estimator, and Correlator.

Packet detector uses time delay, autocorrelation and cross-correlation with the preamble to estimate timing and frequency errors as described in subsection 2.3.3. The model uses 8 delay steps, a conjugated block, two multipliers, one FIR filter with unitary coefficients, one FIR filter with preamble auto-correlated values, two dividers and one complex to angle and magnitude block. Figure 3.14 illustrates the block diagram.

Figure 3.14 - Packet detector model



Source: The author

The input “z” is driven by ADC model and outputs “dw” and “m” represent frequency error and correlation peak respectively.

The second baseband block is phase detector. As described in section 3.2, this block has two operation modes. The first uses a preamble storage vector to estimate initial phase. The second uses a feedback from dispreading block for phase tracking.

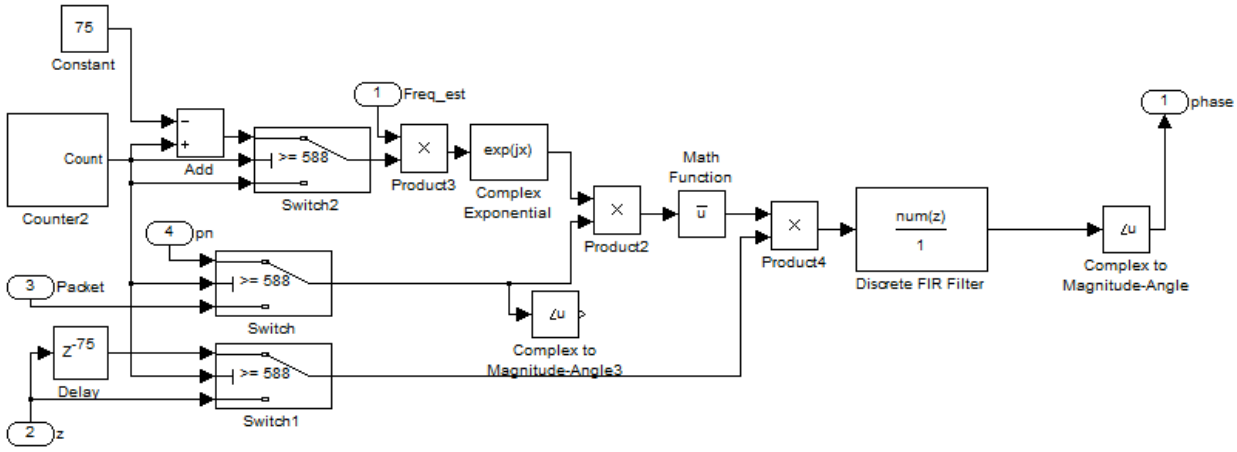
In initial phase mode, a counter multiplies the frequency error estimation and a new signal with the error frequency is generated. The signal is multiplied by preamble values, conjugated and multiplied again by ADC input signal. The average is taken using a FIR with unitary coefficients. Finally, the angle of the complex signal is calculated.

In the tracking mode, the conjugate multiplication is made with the feedback signal from despreading block. To match the phase of feedback and ADC signal, the last has to be delayed by 75 samples as well as the signal with error estimation frequency. Figure 3.15 illustrates the phase modeling.

Both, phase estimation and frequency estimation are added in the top-level model. A new signal containing phase and frequency error is reconstructed and the conjugate is multiplied by the ADC input signal, recovering the *I* and *Q* carrier.

The last block is the Correlator. It uses the sign of *I* and *Q* to decide if it is one or zero and stores the result in a Matlab variable. Also, for model simplification, a new half-sin is created to drive the Phase Estimator from Correlator output. In original model (CHEN e MA, 2008), it should be despread and spread again.

Figure 3.15 - Phase estimator model



Source: The author

3.4.4 Simulation Parameters

The model validation and desired results are obtained through digital baseband simulation, ADC simulation, and system level simulation. All of them use a packet containing 67 octets – 4 for preamble, 1 SFR, 1 PHR, and 61 payloads.

The first set of simulation seeks to validate the digital baseband system and test the minimum SNR required to recover the signal. Therefore, it uses the following configuration:

- No ADC model in the input of baseband was used;
- All frequency errors in a range of ±200 kHz, according to standard were simulated;
- AWGN was set from 10 dB to 0 dB;

The simulation result converges with the theory. For a channel SNR bellow 3 dB the error in frequency estimator increases in order to the digital baseband could no longer recover the signal.

The second set of simulations seeks to extract the gains values of the sigma-delta ADC converters for output numbers of 7 bits, 5 bits, 4 bits, and 3 bits. To perform this task, the output of each integrator in the modulator and the output of "Rescaling for Comparison" block are observed with Matlab scope blocks. The purpose of the first is to adjust the gains (Gain1 and Gain2) to avoid saturation and instability of the converter. The second is to rescale the signal to the maximum amplitude expected by digital baseband.

The ADC parameters extracted from simulation are shown in the Table 3.2. It is important to emphasize that the gains presented is related to the simple ADC model only and it is not a suggestion for a real design.

Table 3.2 - ADC model parameters

# Output bits	Gain1	Gain2	Rescale	Decim. Factor	OSR
7	10,000,000	40,000,000	0.0002441406	16	128
5	8,000,000	40,000,000	0.0006011447	12	96
4	6,000,000	25,000,000	0.001953125	8	64
3	6,000,000	25,000,000	0.00390625	6	48

Source: The author

The OSR required to improve the SNR to produce ENOB of 7, 5, 4, and 3 are shown from Table 3.2. In addition, for the output throughput continues unaltered, the decimation window factor must be 16, 12, 8, and 6 for 7, 5, 4, and 3 bits respectively.

The third set of simulation seeks to extract the lowest required ADC's output bit number to digital baseband recover the carrier according to the noise added by AWGN channel. To accomplish this task, many simulations are required, since for each ADC output bit number, the ranges of frequency error and white noise have to be set.

A Matlab file automates the simulation and sets for each ADC output bit number the following parameters:

- SNR added by the AWGN channel – 10 dB, 5dB, 4dB, and 3 dB;
- Frequency error – 200 kHz, 160 kHz, 120 kHz, 80 kHz, 40 kHz, 20 kHz, and 0 kHz;

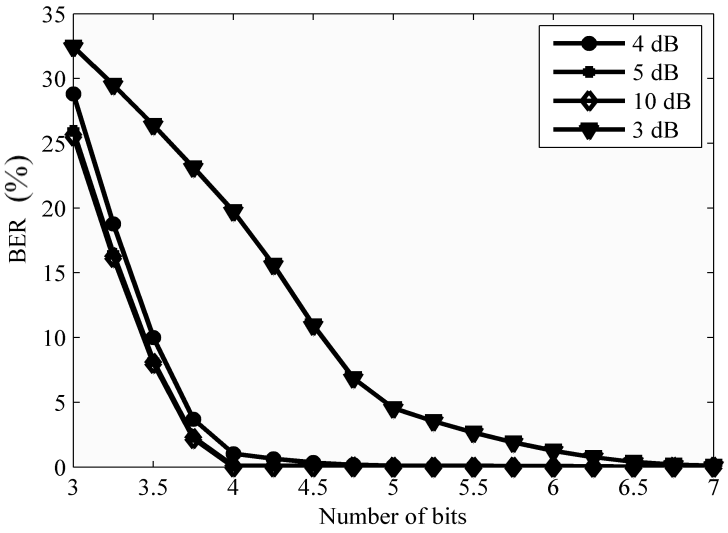
To exemplify, assume the ADC configuration is set to 7 output bits (according to Table 3.2), the Matlab file sets the SNR to 10 dB and the frequency error to 0 kHz. Then it calls Simulink tool and begins the simulation. When simulation is complete, BER, PER, and channel configuration are saved in a text file. Next, the Matlab file changes the frequency

error to 20 kHz and restarts the process. The loop stops when all frequency errors for every SNR value are simulated and saved in the text file.

3.4.5 Modeling Results

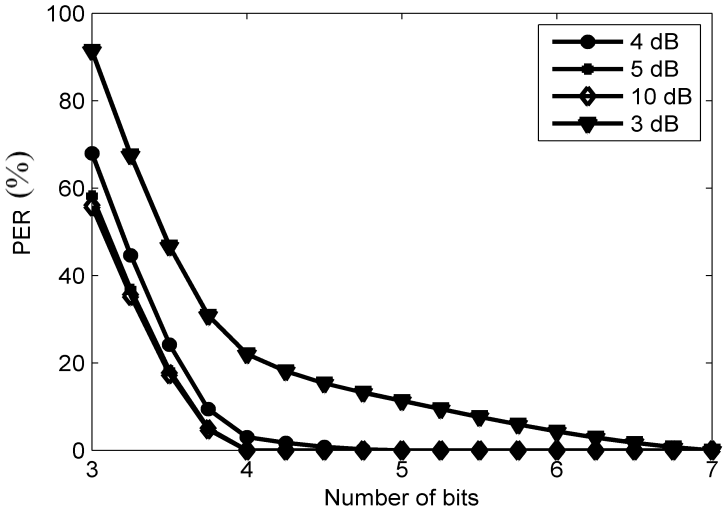
Simulation results are compiled in an Excel table with columns representing SNR and lines BER and PER for every ADC output bit number. Figure 3.16 illustrates the relationship between BER, SNR, and bit length. Figure 3.17 illustrates the relationship using PER instead of BER.

Figure 3.16 - Minimum ADC resolution related to BER for a given SNR



Source: The author

Figure 3.17 - Minimum ADC resolution related to PER for a given SNR



Source: The author

Since the IEEE 802.15.4 standard defines PER of 1%, important conclusions can be made from both figures. The first is that no matter the channel SNR, if the ADC resolution is 3 bits it already adds to much quantization noise into the signal, making the carrier recovery unavailable for the digital baseband architecture presented in this work. The second is that the baseband architecture requires 7 input bits if the channel adds a SNR of 3 dB. For a SNR of 4 dB added by the channel, 5 bits are required. Finally, for 5 dB and above, 4 ADC output bits are enough for a successful carrier recovery.

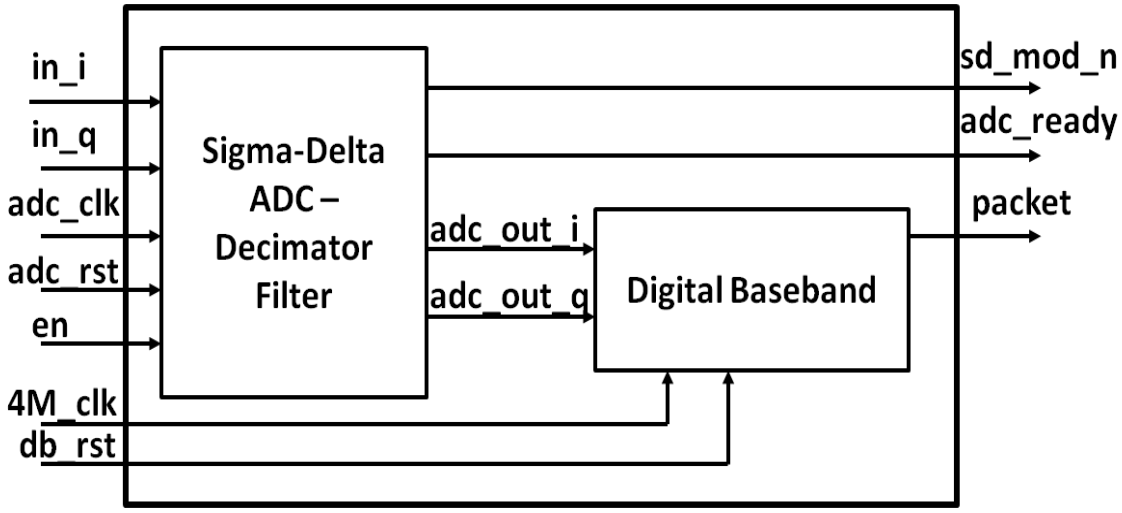
To conclude, this chapter presented the system model and all parameters used. Also, the simulations used were detailed and graphs with the results were illustrated indicating that it is possible to vary the ADC resolution according to the SNR in the receivers input and still recover the carrier. The question that still needs to be answered is if the power saved by decreasing the ADC OSR does pays off the increase of ADC quantization noise. This leads to the next chapter, which will detail the hardware design and the early power analysis results.

4 HARDWARE ARCHITECTURE

Last chapter demonstrated the feasibility of decrease the ADC resolution to save power without compromise the signal recovery. In order to the modification in ADC pays off, the converter must be responsible for considerable amount of the receiver power consumption. It means high ratio between ADC and Digital Baseband power. Therefore the digital baseband must consume as low as possible to increase the ratio and take the maximum advantage of the system noise by power trade.

To estimate the receiver power consumption the digital baseband was carefully designed and the ADC decimation filter in Verilog hardware description language was used. Figure 4.1 presents the ADC and digital baseband top-level architecture.

Figure 4.1 - Top-level architecture



Source: The author

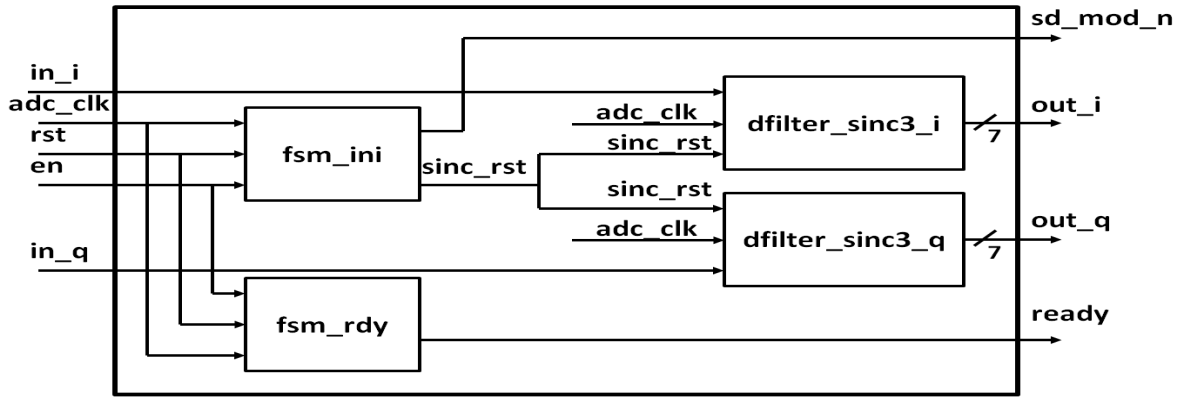
The inputs “in_i”, “in_q”, “adc_clk”, “adc_rst” and “en” are the *I* and *Q* signals from O-QPSK modulation, clock, reset and enable of Sigma-Delta ADC respectively. The inputs “4M_clk” and db_rst are the clock and reset of digital baseband respectively. The “packet” output is the signal synchronized and decoded. The outputs “sd_mod_n” and “adc_ready are detailed in the next section.

The following sections detail both architectures and present the logic synthesis results.

4.1 Sigma-Delta ADC Decimator Filter Architecture

NSCAD Microelectronics team designed the Sigma-Delta ADC and their digital RTL description was licensed to use in this work. The top-level architecture uses two decimation filter (“I” and “Q”) and two finite state machines (FSM) illustrated in Figure 4.2.

Figure 4.2 - Sigma-delta ADC decimator filter architecture



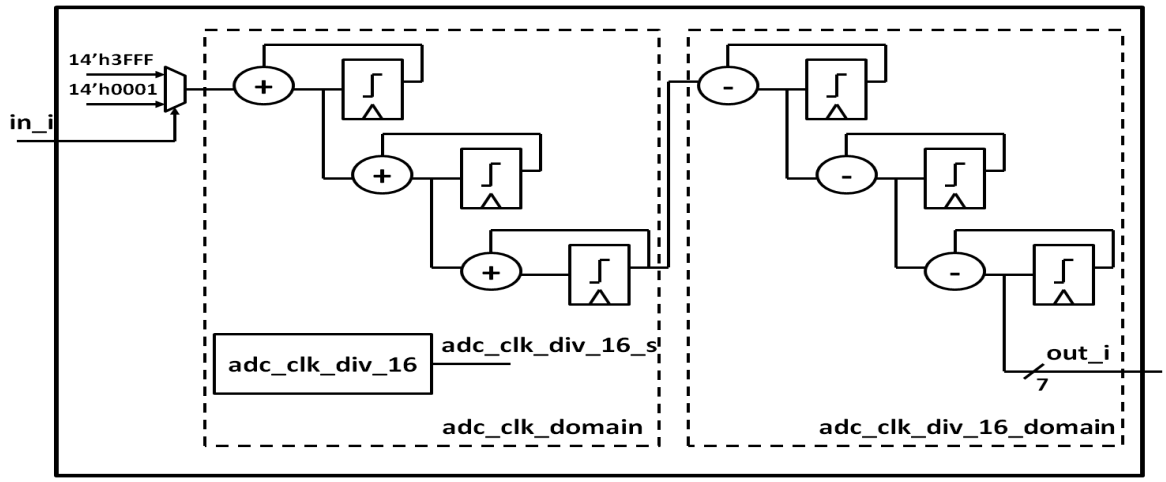
Source: The author

The FSM “fsm_ini” has three states and its function is to generate the initial reset for decimation filters (sinc_rst signal), and the start of operation to modulator through “sd_mod_n” signal. The last triggers high in one “adc_clk” clock cycle after the enable “en” signal and “sinc_rst” in two clock cycles. Further, it remains steady until system reset (rst).

The second FSM function, “fsm_rdy”, is to inform the control system that there are valid values in its outputs. It also has three states and the “ready” signal triggers to high in two cycles after “en” signal.

Finally, the third order decimation filters uses two stages: the first containing additions and the second subtractions cascades. As result of these operations, higher frequencies of Sigma-Delta ADC second order modulator are filtered. To avoid overflow in mathematical operations, 14 internal bits are required. Figure 4.3 presents the block micro-architecture using decimation factor of 16.

Figure 4.3 - Decimator sinc filter micro-architecture



Source: The author

Since "in_i" signal is digital, the input is converted to two-complement logic: zero turning minus one, one turning plus one.

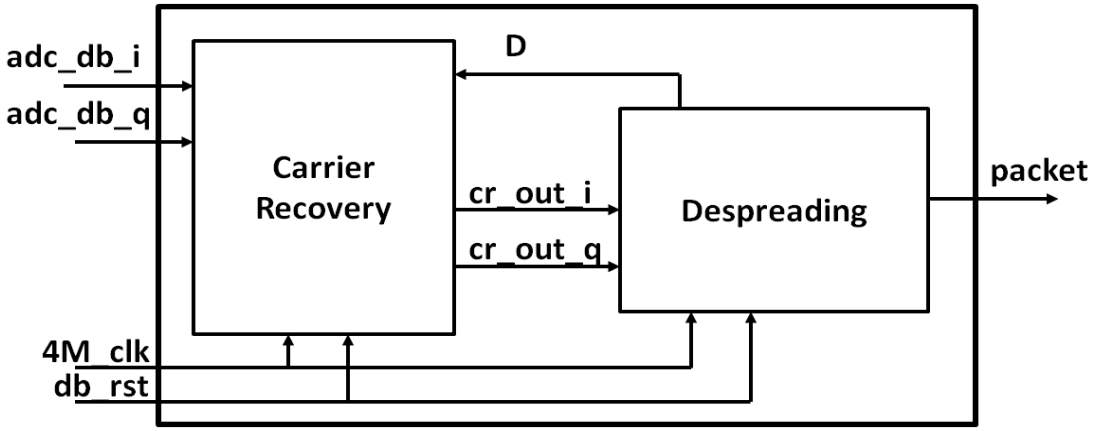
Note that the ADC oversampling frequency will vary according to output bit number required. Therefore, for 7 output bits, it requires clocks of 128 MHz and 16 MHz for first and second stages respectively. Also, as modeling simulations in previous chapter shows, the digital baseband might recover the signal using 4 bits, resulting the minimum first stage frequency of 64 MHz. To keep the throughput constant, the second stage clock frequency must be fixed in 8 MHz. Therefore the decimation factor adapts to 16, 12, and 8 for 7, 5, and 4 bits respectively.

4.2 Baseband Architecture

In Chapter 3 it was presented the baseband architecture chosen as case of study. The micro-architecture, however, might be designed differently from the reference, since details of implementation were not published. Both, on the other hand, have to use similar operators to execute the digital signal processing required for signal reconstruction. Therefore, the micro-architecture presented in current work should obtain close results to the reference.

The top level comprises two processes: Carrier Recovery and Despreading. The first recover the original signal modulated by transmitter and the second despread the packet to its original format. Figure 4.4 illustrates the baseband top-level representation.

Figure 4.4 - Digital baseband architecture



Source: The author

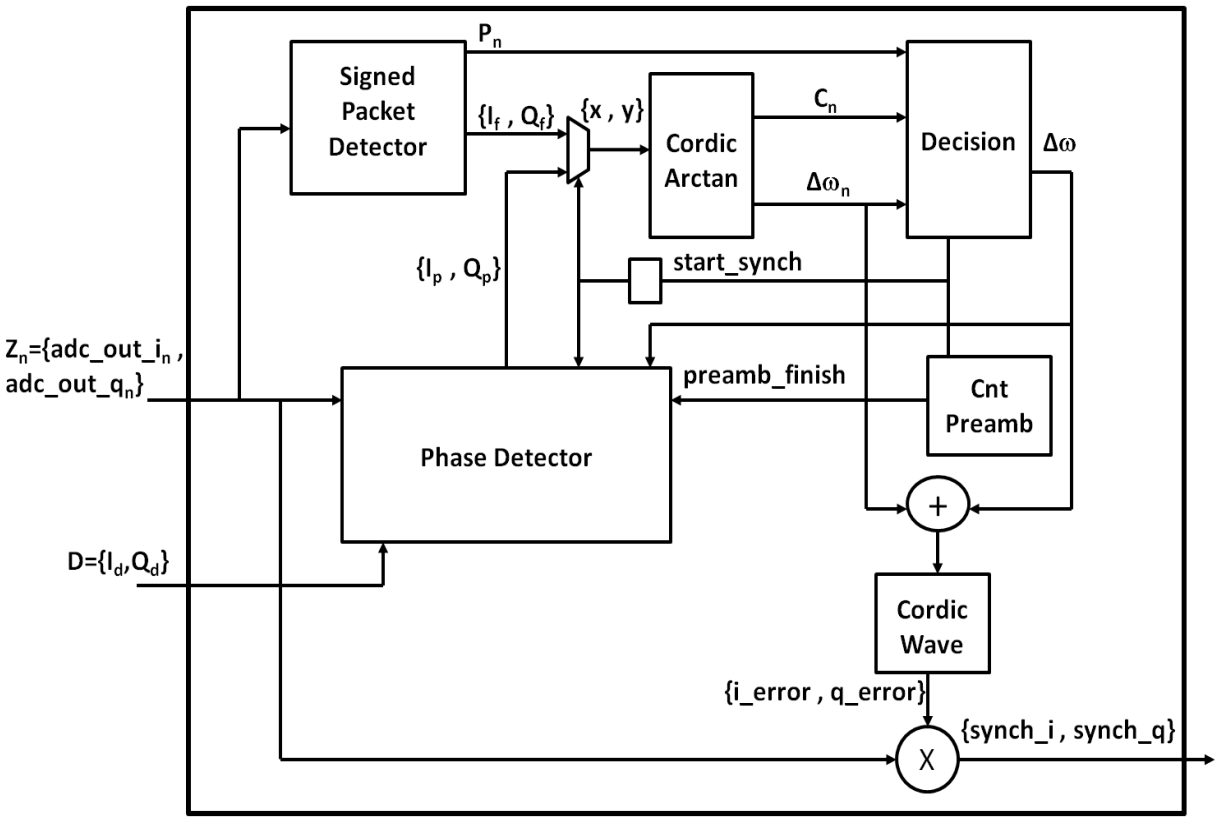
To perform carrier recovery the timing, frequency and phase of the signal need to be estimated and then compensated. Although they might seem to be separated processes, they have dependencies with each other. The frequency algorithm, for instance, selects the sample value based on the timing estimation. Phase estimation uses the frequency estimation in the calculation. Also, compensation uses all estimations to align the signals in a sample precision to properly reconstruct the signal. Therefore, an optimum power efficient digital baseband is a challenging design and requires deep architecture and micro-architecture study.

The carrier recovery designed comprises the following blocks:

- Signed Packet Detector – responsible for packet detection in a sample precision and frequency error estimation.
- Cordic Vectoring – responsible for complex signal's absolute and angle values calculation.
- Decision – responsible for packet incoming validation, Packet Detector block disable, and Phase Detector enable
- Phase Detector – responsible for phase error estimation
- Cordic Rotation – responsible for sin and cosine waves generation.

Figure 4.5 shows the carrier recovery diagram containing the blocks used.

Figure 4.5 - Carrier recovery architecture



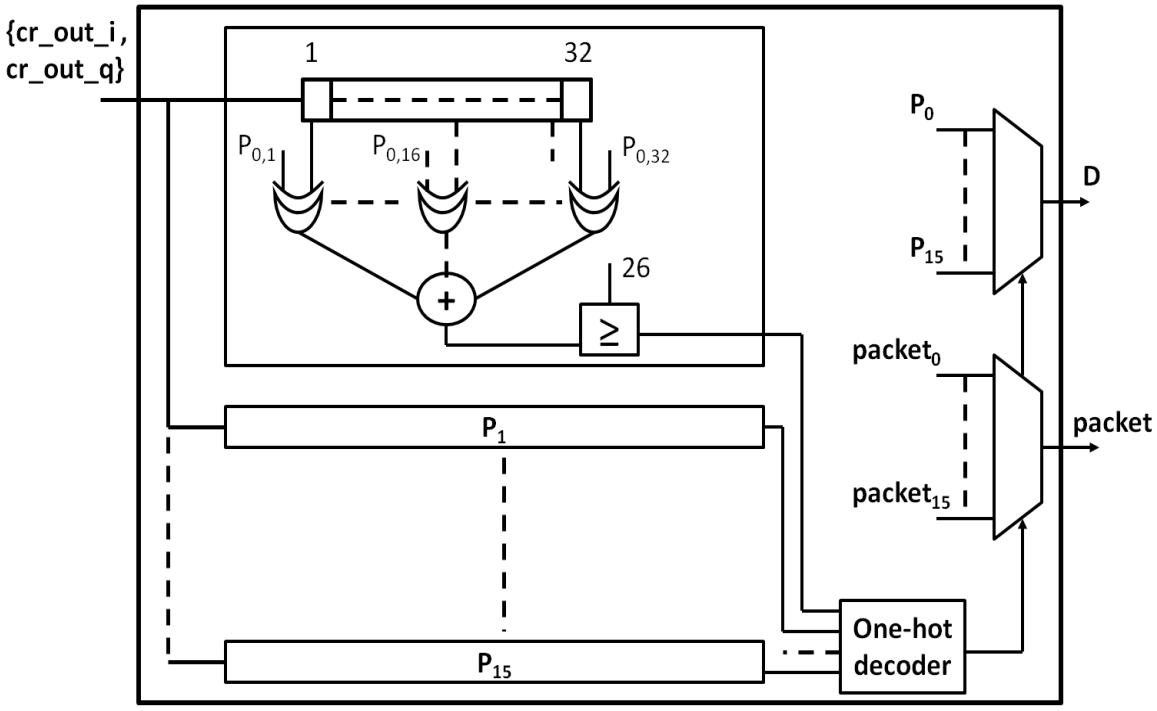
Source: The author

Although it is not represented in the baseband diagram, “start_synch” signal also disables the Signed Packet Detector and enables Phase Detector clocks through clock gating technique.

In addition, signal “preamb_finish” indicates the end of preamble and turns high 128 clock cycles after a packet is detected, which it is enough time for Despreading block to have a valid and synchronized output, “D”, to feedback to Phase Detector block.

The downstream process, Despreading, requires comparison of the incoming bits with 16 vectors of the protocol table. The vector that has higher correlation selects the corresponding 4-bit packet and the feedback vector signal to carrier recovery. Since the minimum hamming distance between vectors is 12, the minimum correlation value is 26 (32 bits minus 6) and it is the threshold that selects the block outputs. Figure 4.6 shows a simplified version of Despreading micro-architecture.

Figure 4.6 - Despreading architecture



Source: The author

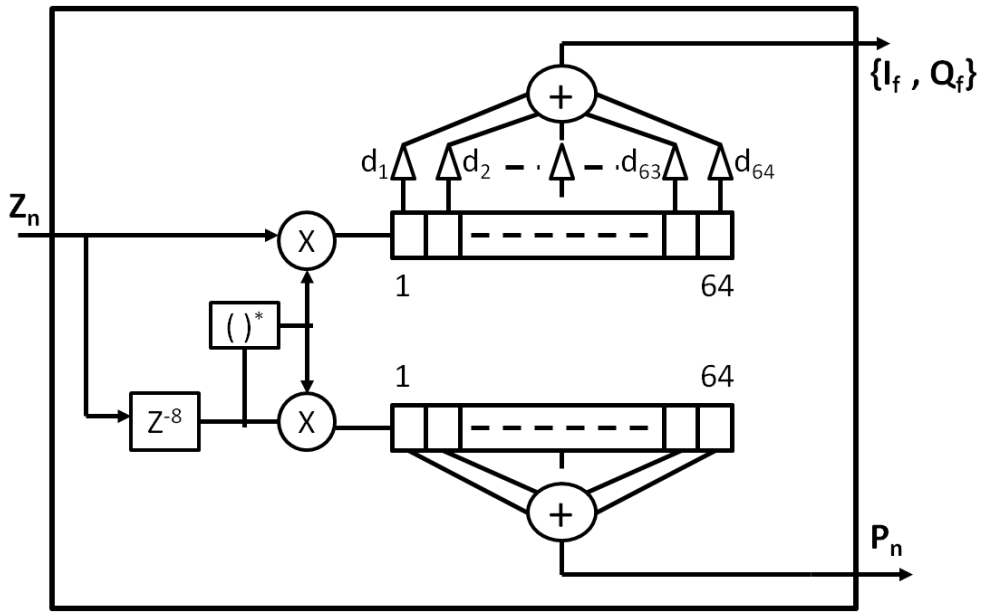
The “Ds” represent the vectors of Despreading lookup table and, because of the hamming distance, only one of the vectors will have correlation equal or above 26.

4.2.1 Signed Packet Detector

Signed Packet Detection micro-architecture uses a smaller version of the original algorithm detailed in Subsection 2.3.3. Targeting register number reduction, and consequently the block power consumption, only the sign of the signals are taken into account.

To validate the signed packet detector, the HDL was exhaustive simulated and compared to Matlab block model. The results matched precisely, ensuring the signed micro-architecture design shown in Figure 4.7.

Figure 4.7 - Signed packet detector



Source: The author

Since the cross-correlation coefficients are unitary real or imaginary values, the multipliers could be strongly optimized, decreasing area and switching activity of combinational datapath logic. Also, to reduce design effort, multipliers and dividers from Cadence Chipware library are instantiated in the hardware description.

4.2.2 Cordic Rotation and Vectoring modes

Coordinate rotation digital computer is a simple and efficient algorithm to calculate hyperbolic and trigonometric functions. It requires only addition, subtraction, bit shift, and table lookup calculations. It has been utilized for applications in many areas such as signal and image processing, communication systems, robotics and 3-D graphics apart from general scientific and technical computation. Also, it is faster than other approaches when the number of gates to implement the functions should be minimized.

To calculate sine and cosine of an angle, assuming the desired angle is given in radians and represented in a fixed point format, it must find the “y” or “x” coordinate of a point on the unit circle corresponding to the desired angle “z”. Successive iterations, starting with x=1, y=0 and rotation of 45 degrees, rotate the vector in one or the other direction by size-decreasing steps, until the desired angle has been achieved. Step “i” size is $\arctan(1/(2^{i-1}))$ for i = 1, 2, 3, …

Equations 4.1 – 4.3 show the Cordic rotation algorithm.

$$x' = \cos(\theta)\,(x - y\tan(\theta)) \tag{4.1}$$

$$y' = \cos(\theta)\,(y + x\tan(\theta)) \tag{4.2}$$

$$\tan(\theta) = \pm 2^{-i} \tag{4.3}$$

Note that for the lookup table of Equation 4.3, and extrapolating the iterative steps, the cos(θ) multiplications result in the limit in the constant K = 0.607252935. As consequence, Equations 4.1 – 4.3 can be simplified to Equations 4.4 – 4.6.

$$x_{i+1} = K_i(x_i - (y_i d_i 2^{-i})) \tag{4.4}$$

$$y_{i+1} = K_i(y_i + (x_i d_i 2^{-i})) \tag{4.5}$$

$$z_{i+1} = z_i - d_i \tan^{-1}(2^{-i}) \tag{4.6}$$

Where:

x_i = x coordinate at iteration "i";

y_i = y coordinate at iteration "i";

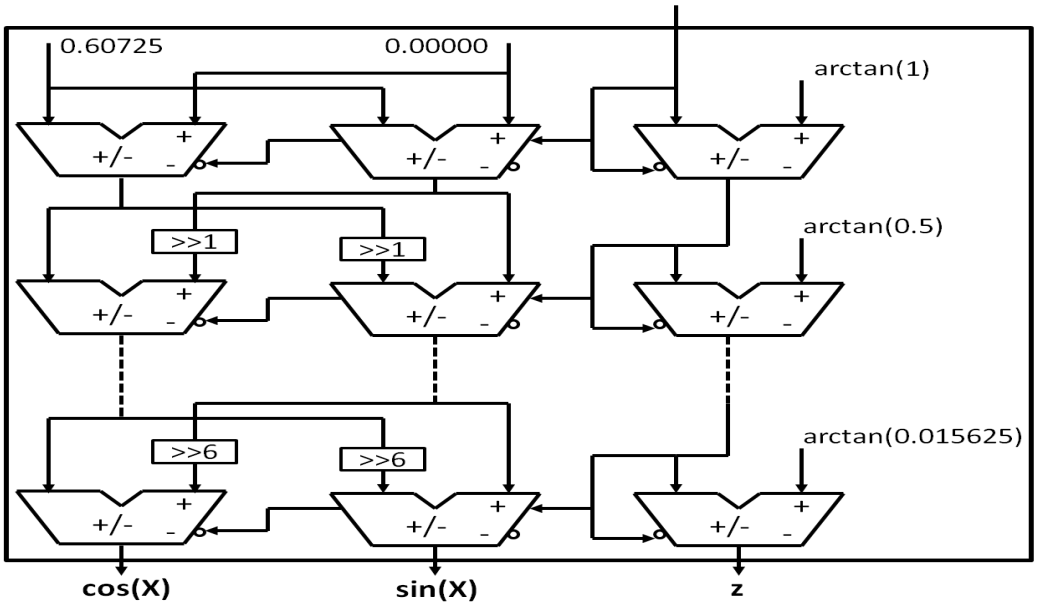
z_i = angle rotate at iteration "i";

d_i = sign of z_i at iteration "i";

Ki = constant resulted from cos(θ) multiplications and Cordic step size.

The Cordic Rotation algorithm is implemented in RTL and it is illustrated in Figure 4.8. Note that to keep the clock frequency untouched, the parallel version has to be implemented.

Figure 4.8 - Cordic rotation architecture



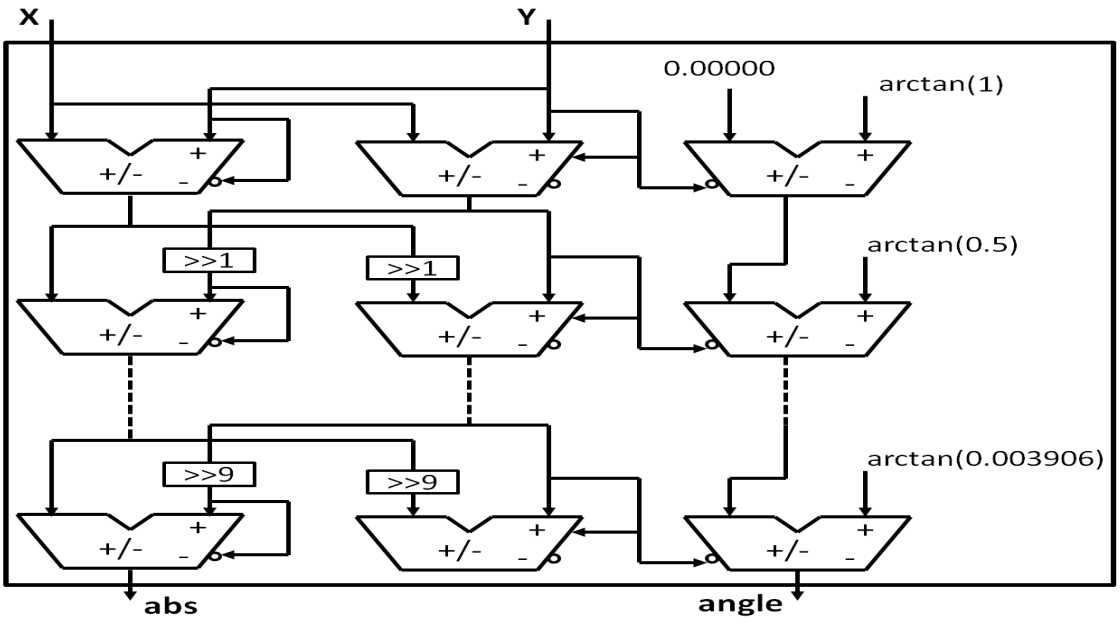
Source: The author

The Cordic Vectoring algorithm is similar to the Rotation, with the following modifications:

- Inputs are “x” and “y” coordinates instead of angle
- The operations are controlled by “y” sign instead of “z”
- Initial angle value is 0

Figure 4.9 shows the micro-architecture of Cordic Vectoring.

Figure 4.9 - Cordic vectoring architecture



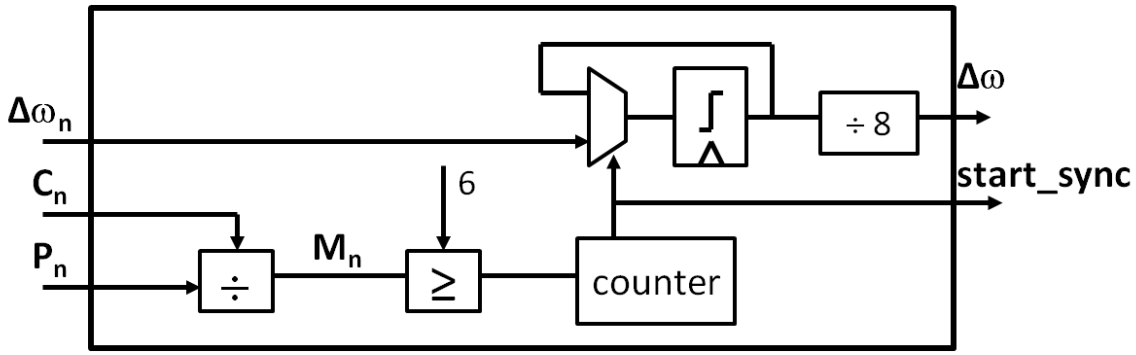
Source: The author

4.2.3 Decision

Decision block uses a defined threshold value to decide whether the incoming signal has an acceptable cross-correlation with the preamble. If the cross-correlation is above that threshold, Decision block increments the internal counter. By the time the counter achieves three, the block judges it is a valid packet, stores the frequency error estimation value, disables the Signed Packet Detector and starts the phase synchronization process enabling the Phase Detector block.

Figure 4.10 details the block micro-architecture.

Figure 4.10 - Decision architecture



Source: The author

4.2.4 Phase Estimator

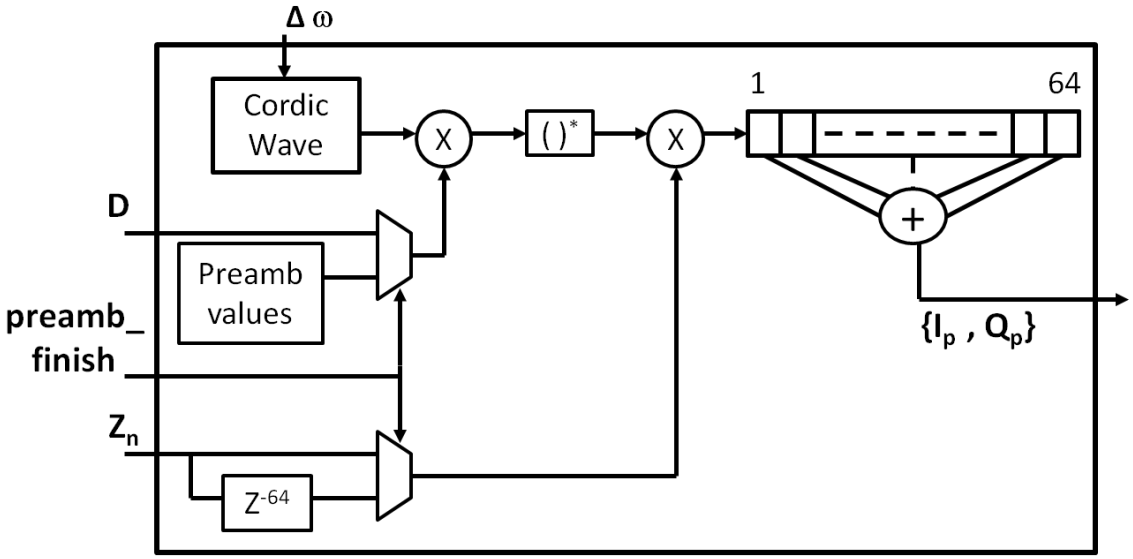
Phase Detector micro-architecture is designed according to algorithm detailed in section 3.2. To achieve the proper functionality, an internal Cordic Rotation block is required to generate a sin and cosine waves of frequency error.

In addition, Phase Detector generates waves of reference packet based on stored preamble vector or received vectors from despreading block, according to “preamb_finish” signal. For synchronization of input packet “Z_n” and reference packet, 64 samples of “Z_n” are buffered. The buffer output is used when the “preamb_finish” signal indicates finish of preamble and selects the Despreading feedback signal “D”.

To calculate the average of 64 phase estimation values, a FIR with 64 TAPs and containing unitary coefficients is implemented.

Figure 4.11 illustrates the Phase Estimator micro-architecture.

Figure 4.11 - Phase estimator architecture



Source: The author

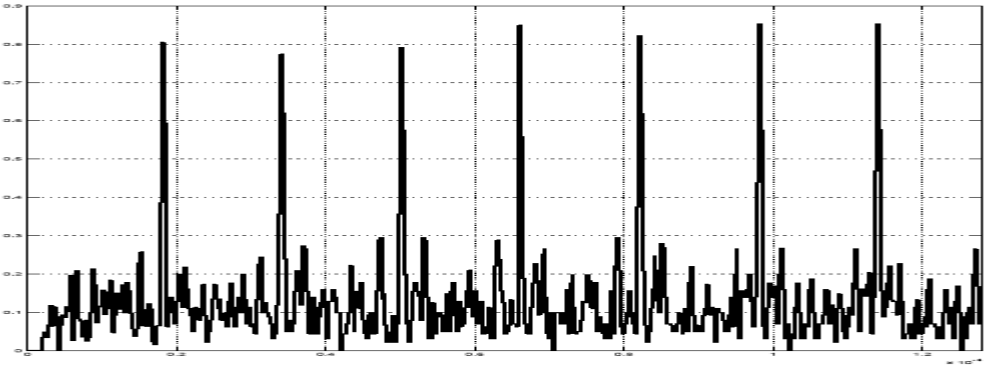
The HDL totalized 9 Verilog files: top-level, signed packet detection, cordic wave, cordic arctan, complex multiplier, phase detector, despreading, decision, and preamble comparator. In total, the baseband HDL spends 2014 Verilog lines of code.

4.3 RTL Simulation

Required in every HDL description to validate the proper functionality of the block, the current work develops and simulates four testbenches: 3 block levels and one top level. Also, to use the same values of the Matlab model, all Matlab simulation vectors after ADC model are saved in files and used as inputs in RTL simulation. For HDL simulation, Modelsim Simulator Student version tool was used (MENTOR GRAPHICS, 2014).

The first testbench created is to validate the Signed Packet Detector block. All input vectors, containing different SNR and frequency errors, are simulated. The frequency error estimation and packet detection peak values are compared with the Matlab model results and, besides the bit precision, both match due to signed architecture. Figure 4.12 shows model and RTL packet detector peak and frequency estimation results.

Figure 4.12 – Model and RTL packet detection peaks

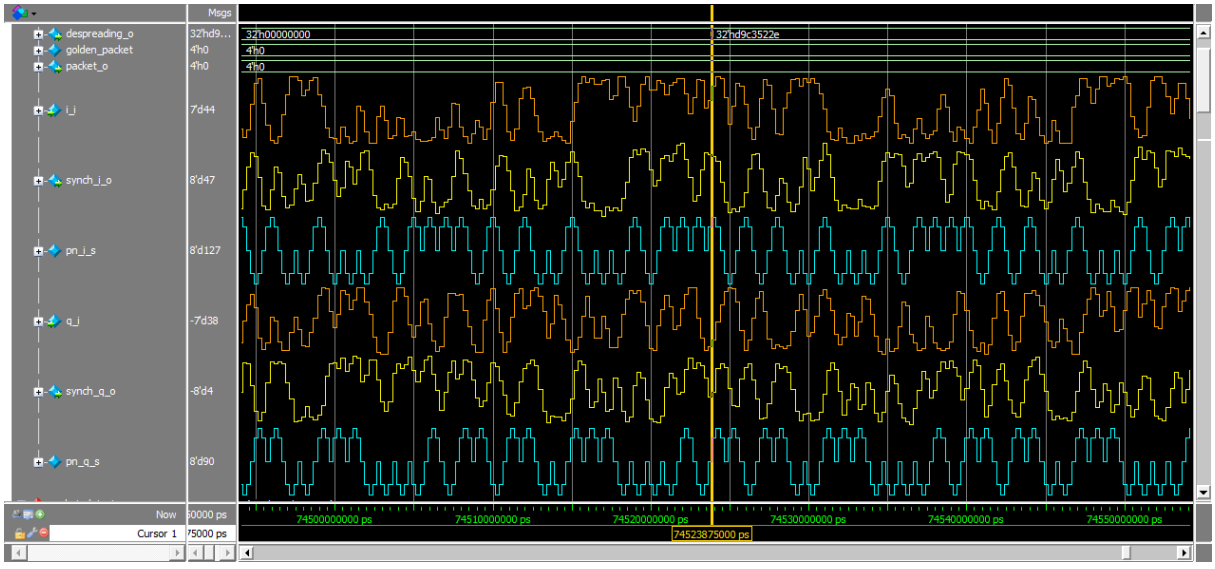


Source: The author

The second and third block testbenches validates the Cordic Rotation and Cordic Vectoring blocks implementation. They are simpler compared to previous one, using determined values of angle, *x* and *y* to check if the output corresponds to expected.

Finally, the top-level testbench uses a similar structure of the Signed Packet Detector testbench but applied to the system. To validate the functionality, the output packet of the system is compared to the input vector before spreading. Figure 4.13 illustrates the transmitted packet in blue, the received in receiver with SNR of 3dB and frequency error of minus 90 kHz in orange, and the baseband output to Despreading block in blue. Also, it is shown the instant in simulation in which the preamble is recognized by Despreading block.

Figure 4.13 - Modelsim simulation of digital baseband



Source: The author

4.4 Logic Synthesis

The power consumption is estimated after logic synthesis through early power analysis to the three input bits possibilities (7, 5, and 4). Decimation filter and digital baseband are synthesized using Cadence RTL Compiler tool (CADENCE, 2014) and the 180 nm process from X-FAB foundry (XC018) – same used in the Sigma-Delta ADC modulator design. The baseband uses a total 13188 cell gates which 3523 are sequential gates. The Table 4.1 shows the gate count and the estimated power consumption per block of the baseband architecture.

Table 4.1 – Baseband synthesis result

Block	Power (mW)	Gate Count
Signed Packet Detector	0.063	1838
Decision	0.001	166
Phase Estimator	1.163	6698
Cordic Rotation	0.078	606
Cordic Vectoring	0.013	868
Despreading	0.387	2321

Source: The author

The resulting netlist is simulated for a unique packet reception using Cadence IUS simulator. A toggle count format file (TCF) containing the switching activity of the gates and nets is feedback to synthesis tool. Finally, a power report from RTL Compiler tool is generated.

Table 4.2 shows the system power for each ADCs bit number (considered a pair of ADC - I and Q of modulation). The ADC modulators data were extracted from Cadence Virtuoso power analysis tool in layout view. It is important to remind that the analysis does not take into account the impact of ADC modulator with different gains in the integrators, remaining constant for the worst case (7 bits of resolution).

Table 4.2 - Power consumption early estimation

ADC Resolution	Modulator (mW)	Decimation filter (mW)	Digital Baseband (mW)	Total (mW)
7 bits	3.6	3.14	1.77	8.51
5 bits	3.6	2.55	1.77	7.92
4 bits	3.6	1.83	1.77	7.2

Source: The author

The table shows that reducing the ADC resolution, impacts up to 42% of power saving in the decimation filter and 15% in the system considered. The expense is a switched-capacitor frequency control in the ADC and digital multiplexer. LQI or BER calculations are already required from protocol and, therefore, do not impact in area overhead. These results were published in the International Instrumentation and Measurement Technology Conference in 2014 occurred in Montevideo – Uruguay.

To conclude, in this chapter the system micro-architecture was presented. Testbenches and simulation results were detailed. The power estimation in synthesis tool showed that a significant power (up to 15 %) could be saved using the adaptive system. Also, the solution is not constraint to IEEE 802.15.4 standard and can easily be applied to other standards transceivers.

5 CONCLUSION

The IoT is dominating the world and the main concern of most applications and devices is the power consumption to improve mobility and battery save. Seeking a contribution in this area, the current work gave an overview of the state of art research and standards, and proposed an adaptive system based in the ADC resolution, SNR robustness of digital baseband, and quality of the signal.

Chapter 2 described the wireless standards, their characteristics and applicability. It has target the IEEE 802.15.4 standard detailing the respective specifications and has discussed the main parts of the standard transceiver. The chapter concluded with an overview of the architecture proposals comprising the RF frontend, the converters, the digital baseband, adaptive systems, and the fields that still could be explored.

The proposed adaptive system was presented in chapter 3. It has described the system, the ADC topology and the digital baseband architecture used. Also, the system model using the Matlab tool containing transmitter, channel and receiver was detailed. The simulation parameters, ADC resolution required per signal SNR simulation results and conclusions also were presented.

Finally, chapter 4 detailed the hardware architecture implemented in Verilog hardware description language. The testbench, stimulus vectors extracted from Matlab simulations and results were presented. Further, logic synthesis using Cadence tool RTL Compiler was executed for early power analysis estimation. The estimation showed that up to 13 % of power save was achieved. The architecture overhead was a multiplexer and an ADC with configurable output resolution.

To future work an adaptive baseband bit width that follows the ADC resolution is planned.

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APPENDIX DESIGN FILES

The CD attached to this document contains the RTL code developed, the vectors for simulation, and the testbench.