UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
PROGRAMA DE PÓS-GRADUAÇÃO EM MICROELETRÔNICA

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Design of analog integrated circuits aiming characterization of radiation and noise

Thesis proposal presented in partial fulfillment of the requirements for the degree of doctorate in Microelectronics

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Porto Alegre,
2015

CIP – CATALOGAÇÃO NA PUBLICAÇÃO

Colombo, Dalton Martini

Design of analog integrated circuits aiming characterization of noise and radiation / Dalton Martini Colombo – Porto Alegre: Programa de Pós-Graduação em Microeletrônica, 2015.

92 f.:il.

Thesis (Doctorate) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Microeletrônica. Porto Alegre, BR – RS, 2015. Advisor: Gilson Wirth; Co-Advisor: Sergio Bampi.

1. Ruído Flicker. 2. Radiação 3. Referências de tensão. I. Wirth, Gilson, II. Bampi, Sergio.

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To Maria Aparecida Martini Colombo, Decio Colombo e Allan Martini Colombo

ACKNOWLEDGEMENTS

Aos meus pais, Maria Aparecida Martini Colombo, Decio Colombo, e meu irmão, Allan Martini Colombo por todo amor e apoio que sempre me deram.

Meu orientador Prof. Gilson Wirth, pelas várias oportunidades que me foram concedidas, apoio e pela confiança em mim depositada. Meu co-orientador, Prof. Sergio Bampi por todo apoio, motivação e suporte durante essa jornada.

À Maíra Malinoski, por todo amor, companheirismo e motivação na reta final do trabalho.

Ao André Luís Rodeguiero Rosa e Felipe Werle pela amizade, companheirismo e por todo apoio no término do projeto do chip fabricado em 130 nm.

Ao Alan Rossetto, pelo bom trabalho de organização e preparação do experimento de radiação realizado em IEAv (Instituto de Estudos Avançados) - Departamento de Ciência e Tecnologia Aeroespacial (DCTA), em São José dos Campos, Brasil.

Fernando Paixão Cortes, Antonio David Souza, Prof. Luiz Fernando Ferreira, Juan Pablo Brito, Arthur Liraneto, Luciano de Paula, Eduardo Conrad e Henrique Pimentel, pela amizade e apoio durante o doutorado, e pelas horas dividindo o mesmo laboratório (#110).

Ao Francisco Osman pela amizade e nossas idas ao forró. Ao amigo Alexandre Simionovski pelo suporte no projeto da PCB.

Fabrício Lara e Gabriela Furtado que fizeram bom trabalho de medição do circuitos.

À Estefânia Aquila, minha professora, que sempre me ensinou muito.

Rafael Cantalice, Gabriela Girardi, Rafael Laufer, Renata Sanfins de Carvalho, Antonio Carlos Beck, Renato Campana, Tatiana Bernardi, Carlo Bernardi, Angélica Anjos, Fabricío Mattos, Fernanda Borba, Vanderlei Borba e Marta Borba, Frederico Möller, Rafael Soares, Ismael Fraga, Dean Karolak, Jorge dos Santos, Sandro Binsfeld, Giovano Camaratta, Moacir Monteiro, André Constantino e Valeska, Mauricio Bartok, Germán Fierro, Prof. Ricardo Reis, Prof. Eric Fabris, Prof. Henri Boudinov, NSCAD, biblioteca e funcionários do Instituto Informática.

Ao Prof. Hamilton Klimach, Laurent Corcelle, Prof. Luiz Fernando Ferreira e Prof. Tiago Balen, por todas contribuições e revisão desse trabalho.

As agências de fomento, CNPq e CAPES, pois sem o auxílio financeiro este trabalho não seria possível.

In English... I´m very grateful to:

Prof. Christian Fayomi from Université du Québec à Montréal (UQAM), Canada. Working as a visitor researcher in his laboratory was really important to my personal and professional development.

Purushothaman Srinivasan, for our research project at Texas Instruments, USA, and all his support during my stay in Dallas.

Django Trombley, Andrew Marshall, Richard Taylor and Xin Zhang for all important support during my work at Texas Instruments.

Michelle Adame, Neil Dalal, Lihn Pham, Andrew Whitcomb, Mylinh Luong, Geneviève Leblanc, Hugues Lemarseillais, Jayanta Baral, special people who made my life happier while far away from Brazil.

ABSTRACT

This thesis is focused on two challenges faced by analog integrated circuit designers when predicting the reliability of transistors implemented in modern CMOS processes: radiation and noise. Regarding radiation, the concern of this work is the Total Ionizing Dose (TID): accumulation of ionizing dose deposited (electrons and protons) over a long time in insulators leading to degradation of electrical parameters of transistors (*e.g.* threshold voltage and leakage). This work presents a case-study composed by bandgap-based and threshold voltage-based voltage reference circuits implemented in a commercial 130 nm CMOS process. A chip containing the designed circuits was irradiated through -ray Cobalt source (^{60} Co) and the impact of TID effects up to 490 krad on the output voltages is presented. It was found that the impact of radiation on the output voltage accuracy was similar or more severe than the variation caused by the process variability for most of the case-study circuits. For the bandgap-based reference implemented using thin-oxide and thick-oxide transistors, TID effects result in a variation of the output voltage of 5.5 % and 12%, respectively. For the threshold voltage references, the output variation was between 2% and 15% depending on the circuit topology. Regarding noise, the concern of this work is the transistor flicker noise under cyclostationary operation, that is, when the voltage at transistor gate terminal is constantly varying over time. Under these conditions, the flicker noise becomes a function of V_{GS}; and its is not accurately predicted by traditional transistor flicker noise models. This thesis presents a case-study composed by voltage oscillators (inverter-based ring and LC-tank topologies) implemented in 45 and 130 nm CMOS processes. The oscillation frequency and its dependency on the bulk bias were investigated. Considering the ring-oscillator, the average oscillation frequency variation caused by supply voltage and bulk bias variation are 495 kHz/mV and 81 kHz/mV, respectively. The average oscillation frequency is 103.4 MHz for a supply voltage of 700 mV, and the measured averaged period jitter for 4 measured samples is 7.6 ps. For the LC-tank, the measured oscillation frequency was 2.419 GHz and the total frequency variation considering 1 V of bulk bias voltage was only ~ 0.4 %.

Keywords: Flicker noise. RTS noise. Radiation. Total dose effects. Voltage reference. oscillators. LC-tank. Bandgap. Threshold voltage.

PROJETO DE CIRCUITS INTEGRADOS ANALÓGICOS VISANDO CARACTERIZAÇÃO DE RUÍDO E RADIAÇÃO

Esta tese de doutorado trata de dois desafios que projetistas de circuitos integrados analógicos enfrentam quando estimando a confiabilidade de transistores fabricados em modernos processos CMOS: radiação e ruído flicker. Em relação a radiação, o foco desde trabalho é a Dose Total Ionizante (TID): acumulação de dose ionizante (elétrons e prótons) durante um longo período de tempo nas camadas isolantes dos dispositivos, então resultando na degradação dos parâmetros elétricos (por exemplo, a tensão de limiar e as correntes de fuga). Este trabalho apresenta um caso de estudo composto por circuitos referência tensões de baseados na tensão de bandgap e na tensão de limiar dos transistores. Esses circuitos foram fabricados em uma tecnologia comercial CMOS de 130 nm. Um chip contendo os circuitos foi irradiado usando raio gama de uma fonte de cobalto (^{60} Co), e o impacto dos efeitos da radiação até uma dose de 490 krad nas tensões de saída é apresentado. Foi verificado que o impacto da radiação foi similar ou até mesmo mais severo que os efeitos causados pelo processo de fabricação para a maior parte dos circuitos projetados. Para as referências baseadas na tensão de bandgap implementadas com transistores de óxido fino e grosso, a variação na tensão de saída causada pela radiação foi de 5.5% e 15%, respectivamente. Para as referências baseadas na tensão de limiar, a variação da tensão de saída foi de 2% a 15% dependendo da topologia do circuito. Em relação ao ruído, o foco desta tese é no ruído flicker do transitor MOS quando este está em operação ciclo-estacionária. Nesta condição, a tensão no terminal da porta está constantemente variando durante a operação e o ruído flicker se torna uma função da tensão porta-fonte e não é precisamente estimado pelos tradicionais modelos de ruído flicker dos transistores MOS. Esta tese apresenta um caso de estudo composto por osciladores de tensão (topologia baseada em anel e no tanque LC) projetados em processos 45 e 130 nm. A frequência de oscilação e sua dependência em relação à polarização do substrato dos transistores foi investigada. Considerando o oscilador em anel, a média da variação da frequência de oscilação causada pela variação da tensão de alimentação e da polarização do substrato foi 495 kHz/mV e 81 kHz/mV, respectivamente. A média da frequência de oscilação é de 103,4 MHz e a média do *jitter* medido para 4 amostras é de 7.6 ps. Para o tanque LC, a frequência de oscilação medida é de 2,419 GHz e sua variação considerando 1 V de variação na tensão de substrato foi de aproximadamente 0,4 %.

Palavras Chave: Ruído *flicker*. Radiação. Dose Total Ionizante. Referências de tensão.

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LIST OF ABREVIATIONS AND ACRONYMS

BGR	Bandgap voltage reference
BiCMOS	Bipolar Junction Transistor and CMOS technology
TC	Temperature coefficient
DTMOST	Dynamic-threshold voltage MOS transistor
PTAT	Proportional to absolute Temperature
$PTAT^2$	Square PTAT
CTAT	Complementary to Absolute Temperature
OA	Operational amplifier
VLSI	Very Large Scale Integration
CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar junction transistor
IC	Integrated Circuit
PSR	Power Supply Rejection
PSRR	Power Supply Rejection Ratio
BW	Bandwidth
DRAM	Dynamic Random Access Memory
PLL	Phase Locked Loop
TSMC	Taiwan Semiconductor Manufacturing Company
DAC	Digital to Analog Converter
ADC	Analog to Digital Converter
VLSB	Least Significant Bit
VR	Voltage Reference
PLL	Phase Look Loop
TC	Temperature Coefficient
SNR	Signal-to-noise-ratio

RMS	Root-mean-square
TEMP	Temperature
SoC	System-on-Chip
SiP	System-in-Package
VCO	Voltage controlled oscillator
DCO	Digital controlled oscillator
RTN	Random Telegraph Noise
RTS	Random Telegraph Signal
EDA	Electronic Design Assistant
TID	Total Ionising Dose
SEE	Single Event Effects
SED	Single Event Disturb
SEU	Single Event Upset
SET	Single Event Transient
SEL	Single Event Latchup
SESB	Single Event Snapback
SEGR	Single Event Gate Rupture
DD	Displacement Damage effects
STI	Shallow Trench Isolation
TIE	Time Interval Error
RBW	Resolution Bandwidth
VBW	Video Bandwidth
GSG	Ground Signal Ground

LIST OF SYMBOLS

Symbol	Description
f_{OSC}	Frequency of oscillation
T_{OSC}	Period of oscillation
f_C	Flicker corner frequency for MOSFETs
	Trap (flicker noise defect) time constant
$_e$	the duration of the trapped state or the mean time before emission occurs,
$_c$	the duration of the empty state of the trap
V_{REF}	Voltage Reference
V_{G0}	Bandgap energy of silicon extrapolated for zero Kelvin
V_{TH0}	Threshold voltage of transistor extrapolated to zero Kelvin
V_{BE}	Base-emitter voltage
ΔV_{BE}	The difference between the emitter-base voltages of two BJT´s
ΔV_{REF_TEMP}	Variation of the V_{REF} over the operation temperature range
V_{LSB}	Voltage that corresponds to 1 bit variation in a Data Converter
U_T	Thermal voltage
J_C	Collector current density
A	Geometric and fabrication process parameter
γ	Temperature coefficient
α	Temperature coefficient of the current source supplying the diodes
k	Boltzmann´s constant
q	Charge of electron
T	Absolute temperature
T_0	Room Temperature
β_F	Common-emitter current gain

I_C	Collector Current
I_B	Base Current
I_S	Saturation Current
n	Ratio of emitter areas
C	Temperature-independent constant
D	Temperature-independent constant
N	Temperature-independent constant
x	Arbitrary number defined by the temperature dependence of the current forced through the collector
V_{GS}	Gate-source voltage
I_{D0}	Process constant
n´	Subthreshold slope factor
W	Channel Width
L	Channel Length
V_{OV}	Overdrive Voltage
V_{OS}	Offset Voltage
V_{TH}	Threshold Voltage
β_N	Negative feedback factor
β_P	Positive feedback factor
$V_{PTAT}{}^2$	Square proportional to the temperature voltage
I_{Supply}	Supply Current
VDD_{MIN}	Minimum supply voltage for one traditional BGR
ΔV_{REF}	Variation in V_{REF}
ΔV_{REF_TOTAL}	Total Variation in V_{REF}
ΔV_{REF_i}	Variation in V_{REF} due to each error source
$V_{REF_MONTE_CARLO}$	Output voltage from Monte Carlo Analysis

$\Delta V_{REF_TEMP_MONTE_CARLO}$ Variation in V_{REF} over TEMP range from Monte Carlo Analysis

$V_{OS_MONTE_CARLO}$ Offset voltage from Monte Carlo Analysis

V_{REF_UPPER} 3σ behavior for the damaged output voltage

V_{REF_DOWN} 3σ behavior for the damaged output voltage

ΔV_{REF_NOISE} Variation of output voltage due the noise

$V_{PEAK\text{-}TO\text{-}PEAK}$ 3 value of noise behavior

V_{RMS} RMS noise

gm Transconductance

V_{FS} Initial full-scale tolerance expected

V_{LSB} Value of the least significant bit

K_F Device-specific noise model constant

ΔV_{TH_TID} Variation in the transistor threshold voltage due to TID

VDD_{RING} Supply Voltage of the ring oscillator

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1 INTRODUCTION

All the progress done in the semiconductor industry since early 70's is well known and it undoubtedly affects our life. It is one of the reasons why we are currently living in the era of "ubiquitous computing", where the human-computer interaction is each time closer and present in our daily life. The well known historical observation about the trends on the advances of semiconductor technologies done by Gordon Moore in 1965 (MOORE, 1997) was true for more than 30 years. The number of functionality per chip (bits and transistors) and the processor performance (clock frequency x instructions per clock) has doubled each 1.5 to 2 year during many years. However, in the last years, the number of transistors and clock frequency has not increased in this same slope as before (IWAI, 2009).

As a result of the evolution of the fabrication process of integrated circuits, huge improvements were done in the speed, power consumption, compactness, functionality and integration level of integrated circuits. Due to these improvements, the historical reduction in the cost per function implemented inside IC's were around 25-29% per year, while the semiconductor market growth were historically ~17% per year, but maturing to slower growth in more recent history (ITRS, 2012).

All this progress of MOS circuits has been accomplished by the downscaling of their components since early of 1970. For instance, in 1971 using a 10 µm CMOS process, Intel introduced the 4004 processor with 2,300 transistors and a clock speed of 108 kHz (INTEL, 2013). Nowadays, commercial processors fabricated in 22-nm process (*e.g.* Processor Intel Itanium 9500) have 8 cores, 3.1 billions of transistors and clock speed of more than 2.5 GHz (INTEL, 2013). Technologies such as strained silicon, high-k/metal gate and multi-gate transistors (*e.g.* tri-gate) are employed to increase performance of the new generation of processors (INTEL-b, 2013). In 2015, Intel announces the fabrication of a new processor called Skylake implemented using a 3D tri-gate (FinFET) transistors of 14 nm process (BOHR, 2015).

Nowadays, the miniaturization of digital functions sustained by the incorporation into devices of new materials and transistor concepts will still continue, although in slower ratio, what is called "More Moore" by some organizations (ITRS, 2012). One example of a new technique that will allow the increase of the number of components per mm^2 is the stack of

layers of transistors on the top of each other composing a monolithic 3D integrated circuit (XIE, 2008).

In addition, there is also a lot of work been done to enhance the compatibility of CMOS and non-digital technologies, which enable the migration of non-digital components from the PCB into the package containing the integrated circuits (System-in-Package, SiP), or even into the chip itself (System-on-Chip, SoC). For example, it would be possible to have an integration of digital circuits with: passive components, high-voltage devices, microelectromechanical systems (MEMS) or nanoeletromechanical systems (NEMS), sensors, actuators and micro-fluidic devices. This concept of functional diversification is called "More than Moore" (ITRS, 2010).

A significant part of the developments of CMOS fabrication process mentioned above was driven by the market of high-performance digital circuits, such as microprocessor (WHITE, 2013). Therefore, although there was a huge reduction on size, cost and power consumption of digital circuits, it is currently much more difficult to implement analog circuits using these modern IC technologies.

Examples of difficulties when designing IC with modern technologies that become even more challenging are the noise and the process variability (*e.g.* fluctuations of the threshold voltage). Because transistor mismatch and flicker noise are inversely proportional to the transistor area (PELGROM, 1989), (RAZAVI, 2001), their impact on the performance of integrated circuits tends to be worse with the transistor size downscaling. Moreover, due to the reduction of the supply voltage, the analog voltage range that can be handled in RF and mixed-signal circuits has decreased significantly. In addition, short channel effects, such as hot carrier effects (PAGEY, 2002), also imposes a challenge for the long-term circuit reliability of integrated circuits.

Other example of current concern on the design of integrated circuits is the radiation (BALEN, 2010) and (SIMIONOVSKI, 2012). The incidence of ionizing particles was previously considered an issue only for CMOS circuits used for aerospace industry and for high-energy physics applications. Moreover, due to the reduction of transistor dimensions, the supply voltage and the capacitance required to store data, integrated circuits are at the present time, more susceptible to the influence of ionizing radiation even when such circuits are operating at ground level (O'GORMAN, 1994).

Although the challenges to design RF and analog circuits has increased, its applications and fraction on semiconductor market has increased (ITRS, 2011). This happen, for instance, due to the fourth generation of cellular phones that requires analog and RF circuits to implement functions that are not properly and efficiently implemented by digital circuits. As analog circuits are bridges between the digital world and the analog real word, these circuits will be always a fundamental part on the design of new products. As a consequence, there is a crucial demand for research that face the challenges of designing high performance analog and RF circuits using new CMOS processes. This thesis focus on two of these challenges, transistor noise and radiation effects.

1.1 Motivation and Scope

1.1.1 Radiation Effects and Total Ionizing Dose

Circuits operating in space environment experience constant bombardment by a wide spectrum of energetic photons and particles coming from the sun and galaxies. The presence of these high-energy particles, ionizing particles (*e.g.* protons, neutrons, electrons, alpha particles or heavy ions) and electromagnetic radiation (*e.g.* gamma-ray) can cause temporary or permanent faults on the operation of the electronic circuits (BOUDENOT, 2007). As for instance, satellites and space telescopes can have its lifetime shorted due to the impact of these high-energy particles that come from cosmic rays, solar flares/winds, and radiation belts (XAPSOS, 2014).

The electronic used in nuclear power plants and physics research laboratories also suffer with high incidence of these participles. But besides of these specific applications, circuits operating at the ground level are also susceptible to the impact of the ionizing radiation, although in lower intensity (O´GORMAN, 1994). In (JUST, 2013), it was demonstrated that SRAM memories could suffer soft errors (*i.e.* the corruption of the information stored in the memory) due to natural radiation (*e.g.* atmospheric neutrons) at ground level.

When these high-energy ions, subatomic particles or atoms moving at relativistic speeds interacts with semiconductor, effects such as Single Event Effects (SEE) and Total Ionising Dose (TID) can happen (BOUDENOT, 2007).

Single Event Effects (SEE) are defined by a sudden high ionising dose deposition of particles (*e.g.* protons and heavy ions) in a sensitive region (*e.g.* transistor reverse-biased

junctions) resulting in functional anomalies of the integrated circuit. This instantaneous perturbation can be or not destructive.

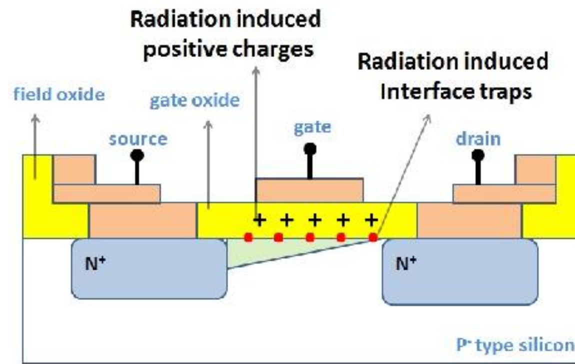
The permanent or momentary corruption of the information stored in a memory element (named as SED and SEU, respectively) or an impulse response of certain amplitude and duration (named as SET) are examples of nondestructive single event effects. A permanent corruption of the information does not mean that the electronic circuit is physically damaged or destroyed, and thus, it can be eventually reprogrammed. SED, SEU and SET are acronyms that means Single Event Disturb, Single Event Upset and Single Event Transient, respectively.

Examples of destructive effects on transistors are Single Event Latchup (SEL), Single Event Snapback (SESB) and Single Event Gate Rupture (SEGR) (DUZELLIER, 2004). In these cases, transistors and the electronic circuit is physically damaged and may not work.

All the above mentioned effects can cause several errors in integrated circuits, as for instance, error conversion in data converters, data corruption in memories (KAY, 2012), calculation errors in microprocessors and power drops in voltage regulators. It is important to see that with the advances of the CMOS technology and the increased speed of operation, effects like SET tend to become even more critical (DUZELLIER, 2004). Moreover, the modeling and simulation of such effects on the performance of complex circuits with reduced dimensions becomes also more difficult. Note that the size of sensitive areas of integrated circuits are in the same order of the size of ionizing particles.

Other effect, not instantaneous as SEE, but that happens over a long time is the Total Ionising Dose. It is the accumulation of ionising dose deposition (electrons and protons) over a long time in insulators (*e.g.* transistor gate oxide layers or field oxides) leading to degradation of electrical performance of the device (BOUDENOT, 2007). For instance, radiation can induce trapped charges in the gate oxide which causes a shift (ΔV_{TH_TID}) in the transistor threshold voltage (V_{TH}) (SCHRIMPF, 2007). If the shift is large enough, for instance, the NMOS Enhancement transistor cannot be turned off even with zero volts applied at its gate terminal (OLDHAN, 2003). Figure 1.1 shows the cross section of NMOS transistor with radiation-induced positive charges trapped in the gate oxide.

Figure 1.1- NMOS with radiation-induced positive charges and interface traps



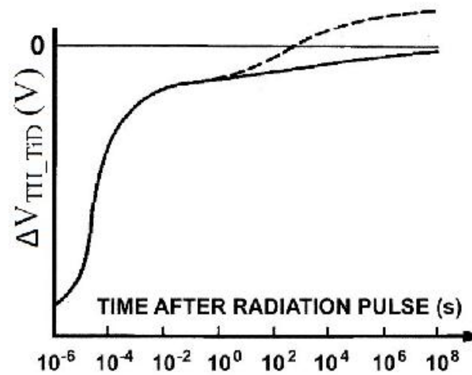
Source: the author

Figure 1.2 shows the variation in the threshold voltage caused by the irradiation ΔV_{TH_TID} (OLDHAN, 2003). Initially, due to the radiation energy that reaches the gate oxide, several electron/holes pairs are created. Some of these charge carriers quickly recombine. Due to the higher mobility, electrons that do not recombine are swept out of the oxide while holes stays trapped in the SiO_2 interface. These positive charges leads to an initial negative shift of V_{TH}. Subsequent carrier recombination tends to decrease the shift of the threshold voltage.

Moreover, the shift on V_{TH} can also becomes positive due to the radiation-induced buildup of interface traps at the Si/SiO_2 interface. These interface traps are shown in figure 1.1 and are similar to those ones induced by the fabrication process. These radiation induced defects can trap electrons and produce a positive shift of $V_{TH,}$ that is represented by the dotted line in figure 1.2. In summary, ΔV_{TH_TID} is roughly a result of two main processes with opposite effects: trapped holes and created interface traps (OLDHAN, 2003). Moreover, charges can be trapped in thick oxide isolation, resulting in an increase in drain-source leakage currents, both intra- as well as inter-devices, and thus, contributing to ΔV_{TH_TID}. More details of these processes will be explained in chapter 2.

Other issue caused by TID on CMOS process is the increase of gate leakage current. This problem is especially important in low power circuits implemented in recent CMOS technologies due to the very thin oxide thickness. Due to irradiation, many defects are created in the SiO_2 which can lead to trap-assisted tunneling current of electrons from the substrate to the gate contact, therefore increasing power consumption and causing failures (OLDHAN, 2003).

Figure 1.2 - Shift in the threshold voltage of NMOS due to TID



Source: the author, modified from (OLDHAN, 1981).

Besides TID and SEE discussed above, a third effect also can happen in semiconductors is the accumulation of crystal lattice defects caused by high energy radiation. Energetic particles (protons and ions) can displace atoms from their sites in the silicon lattice structure leading to displacement damage effects (DD) and electrically active defects that reduce the carrier lifetime (*i.e.* average time required by minority carrier to recombine) and carrier mobility (SCHRIMPF, 2007). This effect is also referred as "accumulation of non-ionising dose deposition" (DUZELLIER, 2004). Differently from ionising dose, this type of radiation has not enough energy to remove tightly bound electrons from atoms and thus creating ions.

This work is focused on the effects of TID on the performance of analog integrated circuits. As ΔV_{TH}_TID and the increased current leakage tend to damage the performance or even to cause permanent failures, they should be well understood with intention of properly designing analog circuits.

1.1.2 Transistor flicker and random telegraph noise

Regarding the noise generated by MOSFETs, one can mention the thermal noise and the flicker noise as the main important noise types. The most significant source of thermal noise is the transistor channel, while the ohmic sections of the transistor (*e.g.* gate, source, drain) can also have lower contribution. The thermal or white noise is caused by the random motion of electrons in electronics and its power spectrum is flat up to 100 THz (RAZAVI, 2001).

This work focus on the flicker noise. Flicker noise is mainly related to the trapping/de-trapping process of minority carriers into/from traps located at the silicon-oxide (Si-SiO_2)

interface or inside the gate oxide. Therefore, this type of noise is proportional to the number of available traps, that are physically, dangling bonds. Dangling bonds can be created by the IC fabrication process or lately formed by the rupture (*e.g*. due to hot carrier injection or radiation) (PAGEY, 2002) of weak Si-Si bonds caused by oxygen vacancies (DRUIJF, 1995). Carrier capture and emission back to the channel leads to current fluctuations (ΔI_{DS}).

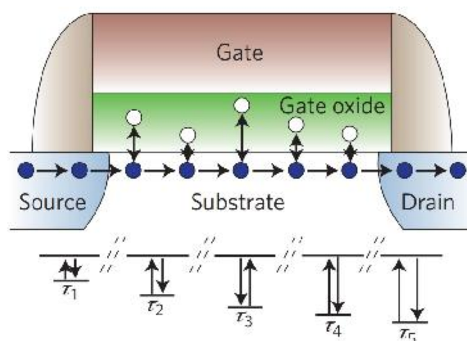
Figure 1.3 illustrates the defects in the $Si\text{-}SiO_2$ interface and the trapping and de-trapping mechanism. Note that traps are represented by white points and they are located inside the oxide gate. One could argue that a more precise illustration would be if the traps were located exactly at the $Si\text{-}SiO_2$ interface, since these traps are the main source of 1/f noise - as will be discussed in chapter 3. Each defect is characterized by its own time constant , which is function of its distance from the channel (z) according to the equation 1.1, where $_0$ is ~ 10^{-10} s and $_F$ is ~ 2 x 10^8 cm^{-1} is the tunneling parameter (BALANDIN, 2013).

$$\tau = \tau_0 \cdot e^{(\lambda_F \cdot z)} \tag{1.1}$$

Recent work, however, has shown that modern oxides are simply too thin to support the elastic tunneling model described by equation (1.1) (and still implemented in BSIM model) (CAMPBELL, 2009). Moreover, no correlation between trap distance from the interface (variable "z" in equation 1.1), and capture and emission time constants was observed by (NAGUMO, 2010). There is still a lot of work to be developed in the above subject.

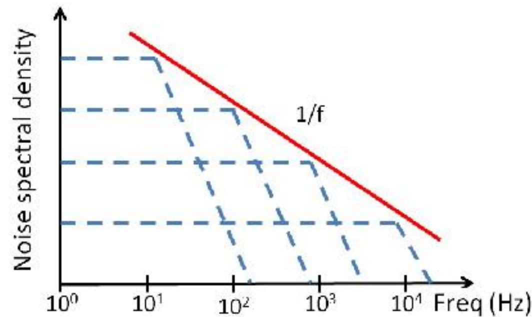
The contribution of all traps with different results in a set of trapping and de-trapping electrons, resulting in a noise spectrum density inversely proportional to the frequency range as it is shown in figure 1.4 . Each dotted line in figure 1.4 represents one trap (BALANDIN, 2013).

Figure 1.3 - Defects (dangling bonds) at $Si\text{-}SiO_2$



Source: (BALANDIN, 2013)

Figure 1.4 - Flicker noise spectrum



Source: the author, modified from (BALANDIN, 2013)

Flicker noise is a problem because it affects the performance of digital, analog and RF circuits. Few examples of the impact of 1/f noise on the performance of electronic circuits are listed below:

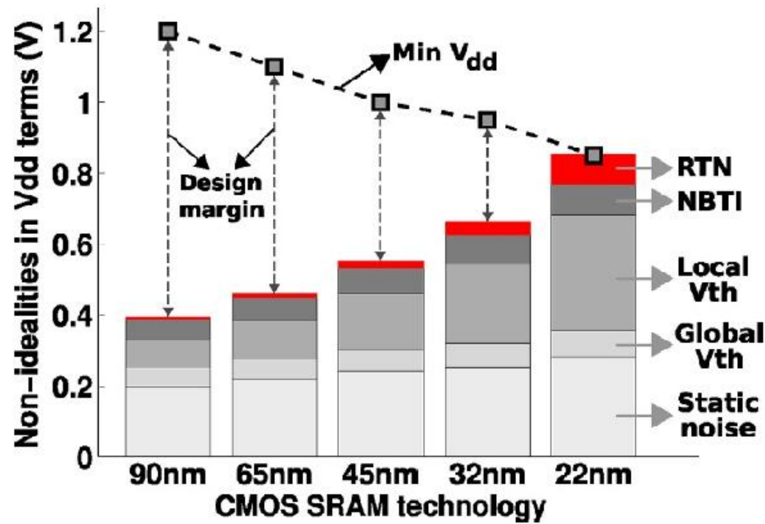
- degrades the phase noise and jitter of integrated oscillators (GIERKINK, 1999)
- causes erratic behavior in static random-access memory (AADITHYA, 2013)
- limits the number of effective bits achieved by data converters (NEU, 2010)
- limits the accuracy of voltage references circuits (HOLMAN, 1994)

The impact of 1/f noise is even more critical for small-area low power CMOS circuits implemented in recent nanometer CMOS technologies. The low supply voltage (*e.g.* lower than one volt) means lower signal to noise ratio. Small area transistors (*e.g.* transistor length < 100 nm) presents higher flicker noise since its 1/f noise is inversely proportional to transistor area. Moreover, the use of halo doping to reduce the short channel effects results in higher flicker noise performance (SRINIVASAN, 2012).

When the transistor length becomes very small (*e.g.* $L < 130$ nm), the number of traps in the Si-SiO_2 interface becomes also small, and in these cases, the discrete noise generated by these traps are not referred as 1/f noise, but as random telegraph noise (RTN) or random telegraph signal (RTS) (DIERICKX, 1992). As for instance, if the transitor has only one trap, the current (or resistance) fluctuations happens between only two discrete values, analogous to the telegraph signal.

Figure 1.5 shows the impact of RTS on the design margin of CMOS SRAM circuits has increased as transistor dimensions has decreased. Lower the technological node and the supply voltage, smaller the design margin and worse the RTS noise.

Figure 1.5 - RTN noise on the design margin of CMOS SRAM



Source: (AADITHYA, 2013)

This thesis is focused in a particular condition of the flicker or RTS noise, that is called cyclostationary (PHILLIPS, 2000). Circuits with time-varying operating points modulates the noise generated by bias-dependent noise sources, and therefore, modulates the transfer function from the noise source to the output and then, a non-stationary noise is generated. This periodic variation of the output noise, called cyclostationary noise, is especially important in oscillators, mixers and data converters since the bias voltage (gate-voltage) of some transistors are constantly varying with time. Traditional simulation tools (*e.g.* SPICE) do not properly estimate cyclostationary noise (PHILLIPS, 2000) (AADITHYA, 2013), what makes the subject of this thesis very important for circuit and electronic design assistant tool (EDA) designers.

1.2 Objectives of this thesis

This work deals with two challenges in the design of analog integrated circuits: the impact of TID and flicker noise (under cyclostationary conditions) in the performance of analog integrated circuits.

In order to verify the effects of TID in analog circuits implemented in advanced CMOS process, voltage reference circuits were chosen as case-study. Several architectures of voltage reference are available in literature and the most part of them are based on Bandgap voltage

(V_{BG}) and transistor threshold voltage (V_{TH}). Those ones based on V_{TH} are specially important when low-voltage and low-power operation is required, and therefore, were implemented in this work.

The most part of the designed circuits were designed to operate at 1 V due to the current low power and low voltage requirements of many applications. The CMOS process used to implement the voltage references is a standard and commercial 130 nm CMOS process. The most circuit implementation were done using core transistors (*i.e.* thin oxide and VDD = 1.2 V). However, since the impact of irradiation also depends on t_{ox}, a voltage reference using 2.5 V devices (thicker oxide) were also designed. Moreover, a traditional PTAT current reference and a simple voltage regulator were also implemented.

The temperature and supply voltage dependency, process variability and TID effects on the performance of the designed circuits were characterized. The TID effects were characterized after irradiation using -ray of a Cobalt source (^{60}Co).

The content developed in this thesis can be used for (i) better design of voltage references when radiation is the concern, (ii) a modeling of radiation effects and also for (iii) the development of simulation tools (EDA) for TID irradiation (Colombo, 2013)

Regarding the impact of flicker noise on analog circuits, voltage oscillators were chosen as case-study in our work. The implemented voltage oscillators have key transistors that operate in cyclostationary regime, whose gate voltage is constantly varying with time. As a consequence, the output noise of these circuits, normally called jitter or phase noise, can be used as case-study for the investigation of cyclostationary noise.

Our research group at UFRGS has been working in the developing of improved transistor flicker noise models for several years (DA SILVA, 2008). One of the fundamental steps of this work is the analysis of jitter and phase noise of fabricated circuits, and its comparison with simulation results. Therefore, the second part of this thesis works as a brick in the development of improved flicker noise models.

Two topologies of voltage oscillators were implemented: (a) ring-oscillator and (b) LC-tank oscillator. Ring-oscillator is a proper case-study because its jitter or phase noise is a direct function of flicker noise of transistors working in cyclostationary operation. It is a simple circuit that is composed only by transistors that are constantly switching in time and then, it is an useful case-study.

The LC tank oscillator is an important and complementary case-study due to its wide use in industry applications; and because its output voltage has improved robustness against the fabrication process compared to the ring-oscillator. Moreover, the output frequency practically does not depend on the bulk bias. This is an important feature because we want to verify the impact of the bulk bias on the output noise (jitter or phase noise) without changing the frequency of the output voltage. The LC tank circuits were implemented in a commercial 45 nm CMOS technology.

The content developed in this thesis is useful in the development of simulation tools for noise analysis and for the better understanding of the impact of flicker noise in the performance of voltage oscillators.

1.2.1 Voltage references

Voltage references are building blocks that are essential in various mixed-signal and radio frequency circuits. Such circuits include simple amplifiers, comparators, voltage regulators, data converters or phase-locked loops (PLL), for instance. The reference must generate a precise output voltage (V_{REF}) that is ideally independent of process, power supply line, load and temperature variations. Between the usual metrics used to characterize the performance of voltage references, one can exemplify (COLOMBO, 2009):

- output voltage drift or temperature coefficient (TC): it is the variation of V_{REF} over the temperature range of the application. It is frequently expressed in parts-per-million per degree Celsius (ppm/°C).

- line sensibility or regulation: it is the variation in V_{REF} caused by power supply variations. It is frequently expressed in percentage, µV/V or ppm/V. Moreover, power supply rejection ratio (PSRR) show how the line sensibility is degraded when the frequency of the power supply variations is increased (ANALOG DEVICES, 2015) and (MILLER, 2015).

- load regulation: It is the variation in V_{REF} caused by the effects of loading the reference. It is often expressed in ppm/mA (ANALOG DEVICES, 2015) and (MILLER, 2015).

- tolerance, variability or initial accuracy: the tolerance of V_{REF}, normally expressed in %, after the circuit is turned on.

The precise output voltage is used to bias others circuits to generate predictable and repeatable results. For instance, a digital to analog converter (DAC) produces an output voltage that is proportional to V_{REF} and the number of bits of digital input word (ALLEN, 2004). As a consequence, the minimum least significant bit variation (V_{LSB}) that a converter can compute depends directly on the accuracy of the voltage reference circuit (BAKER, 2009). This dependency is especially important for high precision converters with large number of bits employed in instrumentation and measurement systems. As voltage reference circuits play a significant part in determining the operation and performance of the entire systems, these circuits are adequate and useful for the characterization of the impact of radiation.

The widely used implementation for voltage references, for more than forty years, is the bandgap voltage reference (BGR). This type of circuit was named “bandgap” because its output voltage is close to 1.16 volts (HILBIBER, 1964), which is the bandgap energy per elementary electron charge in silicon extrapolated to zero Kelvin (V_{G0}). The bandgap technique was proposed by (HILBIBER, 1964), but it was only seven years later that the first integrated circuit implementation of this technique was published (WIDLAR, 1971). Since then, several improved voltage reference circuits based on bandgap principle has been published (TZANATEAS, 1979), (MEIJER, 1982), (NICOLLINI, 1991), (VERMAAS, 1998), (YAO, 2005) and (ANDREOU, 2012).

In order to design voltage references that attend all requirements of advanced RF and mixed-signal circuits employed in recent battery-operated portable equipments, these circuits must have low voltage (*e.g.* working under 1 volt of supply) and low power operation. For instance, power consumption of few tens of nW to a few μW is frequently required (COLOMBO, 2010). This requirement is needed because these circuits operates for long periods and then, requires a significant amount of energy from the battery. However, battery size is often a limiting factor as its volume is limited for portability. Moreover, other applications such as environment monitoring must harvest energy from natural (and sometimes limited) energy sources such as ambient light, heat and motion. In addition, the speed and high-integration density of transistors in single dies have increased heat dissipation to critical limits.

Therefore several alternative implementations for voltage references circuits that operate with 1 volt of power supply have been published on the last years (FAYOMI, 2010). A example of alternative topology of voltage references is that one which the output voltage is

proportional to the threshold voltage of transistor extrapolated to zero Kelvin (V_{THO}) (GIUSTOLISI, 2003) and (COLOMBO, 2011). The typical threshold voltages are in the range of 600 mV and 400 mV, for 0.25 µm and 90 nm CMOS technologies, respectively. As these voltage are less than 1 volt, it is completely feasible to design V_{TH0}-based references that operates under low supply.

1.2.2 Oscillators

Analogously to voltage reference circuits that provide a precise DC voltage for analog circuits, voltage controlled oscillators (VCO) and digital controlled oscillators (DCO) provide the precise frequency reference needed in RF systems, as for instance, in transceivers. Oscillators represents many times the bottleneck in radio design. The main features of these circuits are oscillation frequency, frequency-tuning range (*i.e.* how much the oscillation frequency can be controlled by the input voltage), power consumption and spectral purity - usually measured in terms of phase noise.

The phase noise is the frequency domain representation of rapid and random fluctuations in the phase of a waveform caused by time domain instabilities. This quantity is usually expressed in dBc/Hz and represents a trade-off with power consumption and tuning range (LEESON, 1996). In addition, the phase noise normally gets worse when the oscillation frequency increases (HAJIMIRI, 1998).

Ring oscillator is a circuit consisting of an odd number of stages larger than 1 in a loop which the output voltage oscillates between two voltage levels. Each stage delays the input signal for a certain period of time ( ), and at the output of the final stage, the total delay is equal to the product of and the number of stages (n). The oscillation frequency (f_{OSC}) is given by equation (1.2) (SEDRA, 1997):

$$f_{osc} = 1/(2 \cdot n \cdot \alpha) \quad (1.2)$$

As can be seen, the oscillation frequency is inversely proportional to the number of stages. The more stages there are, the lower the frequency will be.

For the traditional voltage controlled ring-oscillator formed by a chain of inverters, the fundamental frequency of a ring oscillator is proportional to the supply voltage. As the supply

voltage increases, both rise and fall-time decrease (more voltage for the same capacitance), and therefore, the oscillation frequency increases.

LC tank oscillator uses passive inductor with inductance (L) and capacitor with capacitance (C) in order to define the output voltage whose frequency, f_{OSC}, is roughly given by equation 1.3 (RAZAVI, 2001):

$$f_{OSC} = 1/\left(2 \cdot \pi \cdot \sqrt{L \cdot C}\right) \tag{1.3}$$

Ideally, at f_{OSC} the reactances of inductor and capacitor are equal and opposite. A common implementation for LC tank oscillator uses a cross-couple CMOS transistors with the LC thank connected in its gate terminals.

1.3 Thesis Organization

This thesis is organized as follow. Chapter 2 discuss the concepts and the challenges imposed by TID on the performance of analog integrated circuits. Effects such as shift in the threshold voltage, the increased leakage and degraded mobility are discussed.

Chapter 3 discusses the origin of transistor flicker noise, its behavior when the transistor is operating with a switched gate bias voltage, and the traditional models/simulation tools used to estimate this type of noise.

Chapter 4 presents the first group of case-study of this thesis, the voltage reference circuits, while Chapter 5 presents the ring-oscillator and LC-tank oscillator. Chapter 6 and 7 present the silicon results for the voltage references and oscillators, respectively. Finally, the conclusions are presented in Chapter 8.

2 TOTAL IONIZATION DOSE (TID)

Total ionizing dose results in a shift on threshold voltage, a degradation of carrier mobility, an increased leakage current and worse 1/f noise performance (BARNABY, 2006) and (FLEETWOOD, 1994) for CMOS transistors. In order to properly design analog CMOS circuit that are subject to irradiation and also correctly estimate the effects of TID on ICs, a good understanding about the physical processes of TID is needed.

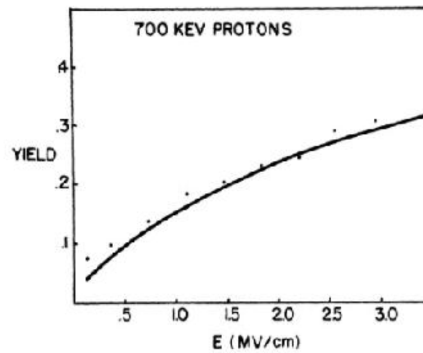
Although the damage impact of TID in circuits implemented in advanced CMOS technologies *(e.g.* thin oxide, high-k dielectric and shallow trench isolation) differs in some aspects from the old CMOS process (*e.g.* thick oxide, SiO_2 and LOCOS isolation), the basic physical process evolving the radiation damage are essentially the same. Thus, this chapter starts with general aspects of the impact of radiation in old CMOS process before going to the advanced CMOS processes.

2.1 Trapped holes, bond reformation and rebound

When radiation energy reaches the gate oxide and substrate regions of transistors, there is generation of many electron-hole pairs (OLDHAM, 1999). The number of generated electron-hole pairs is a function of the incident particle type and energy; and the most part of these pairs recombines soon after the incidence of the particle or electromagnetic wave. Recombination is a function of electric field and carrier concentration (SCHRIMPF, 2007); and higher the magnitude of the electric field (E), lower the rate of recombination because the carriers are swept out of the transistor oxide more quickly (OLDHAM, 1981).

The inverse of recombination rate is normally called "yield" (OLDHAM, 1981). Figure 2.1 shows the yield as a function of electric field in a experiment which a beam of protons with kinetic energy of 700 keV is thrown upon the gate oxide of MOSFET (OLDHAM, 1981). In figure 2.1, points represents the experimental results while line is the theoretical model.

Figure 2.1 - Yield of electron-hole pairs as a function of electric field



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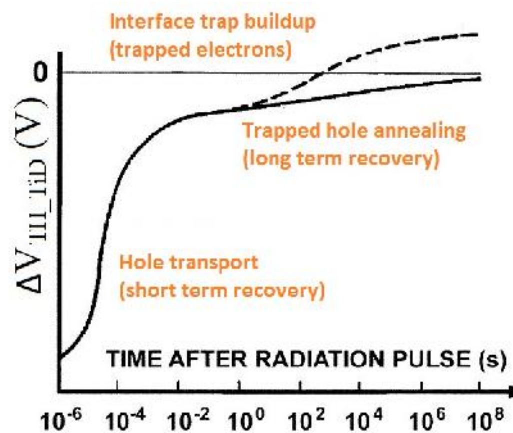
Source: (OLDHAM, 1981)

Electrons that escape of recombination are swept out of the oxide very rapidly, in a time on the order of a picosecond (OLDHAM, 1981). Note that electrons have higher mobility than holes in SiO_2. The holes that remained in the SiO_2 affect the electrical behavior of the transistor, and this effect can be modeled as a negative shift in the threshold voltage of the NMOSFET ($\Delta V_{TH_TID} < 0$).

The shift on threshold voltage after irradiation pulse is shown in figure 2.2. Figure 2.2 is a copy of figure 1.5 but including physical processes related to ΔV_{TH_TID}. As one can verify, as soon the radiation reaches the gate oxide, a large initial negative shift on V_{TH} is generated.

Figure 2.2 - ΔV_{TH_TID} as a function of time after irradiation pulse



Source: (OLDHAM, 1981)

The holes are then transported to the Si/SiO_2 interface in a mechanism that takes place over many decades in time, and it is strongly dependent of oxide thickness. This process is normally over in much less than 1 s at room temperature (OLDHAM, 1989), and it is described in (OLDHAM, 2003) as "the transfer mechanism seems to be a hopping of the

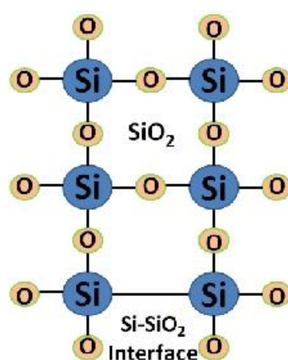
holes between localized shallow trap states having a random spatial distribution". During the transport of holes, recombination happens and ΔV_{TH}_TID tends to decrease. The reduction of ΔV_{TH_TID} is called short-term recovery and is shown in figure 2.2.

When holes approach the Si/SiO_2 interface, they are deep trapped due to defects existing in this region (*e.g*. oxygen vacancies) (LELIS, 1988). Figure 2.3 shows an simplified view of the atomic structure at Si/SiO_2 interface and the defects caused by oxygen vacancies. These defects are located, for example, within 50 Å from the Si/SiO_2 interface for old CMOS processes (LENAHAN, 1984).

As can be seen in figure 2.3, there is one oxygen atom missing from the usual lattice configuration and then, there is a weak Si-Si bond, where a Si atom is bonded to three oxygen atoms. The Si-Si bond can be break and the positive charges (holes) can be trapped (PERSHENKOV, 1995). The defects specially located in the first few monolayers of SiO_2 (*e.g*. 3 nm) are normally called "border traps" or "near-interface traps" and their time response is different from the others "oxide traps" (Fleetwood, 1996) and (BARNABY, 2006).

Oxide trapped holes are stable but they experiences long-term annealing at ambient temperature which can extend for hours or years (OLDHAM, 2003). The trapped hole annealing means that the trapped hole can be released and the bond Si-Si can be redone (bond reformation).

Figure 2.3 - Defects at Si/SiO_2 interface structure



Source: the author

The recovery of the V_{TH} can be speed up if the annealing is done at high temperatures (*e.g.* 100 ºC). Bond reformation is also referred as "true annealing" (OLDHAM, 2003). There is also other process called "rebound", that happens in parallel with the bond reformation, and it causes also the cancellation of the effects of trapped holes and the recovery of V_{TH} (SCHWANK, 1984).

The "rebound" is the process after irradiation in a NMOS devices which electrons from the silicon tunnel into the oxide and neutralize the oxide trapped charge (SCHWANK, 1984). This long-term annealing process is dependent of temperature and gate bias. Higher temperature and/or positive gate bias makes the "rebound" process faster. If the gate bias voltage is decreased during the "rebound", an incomplete annealing of the oxide trapped happen and the process takes more time (SCHWANK, 1984). However, the gate bias does not affect the final saturation voltage of V_{TH} (SCHWANK, 1984). The "rebound" similarly to the "bond reformation" causes a positive shift of V_{TH}.

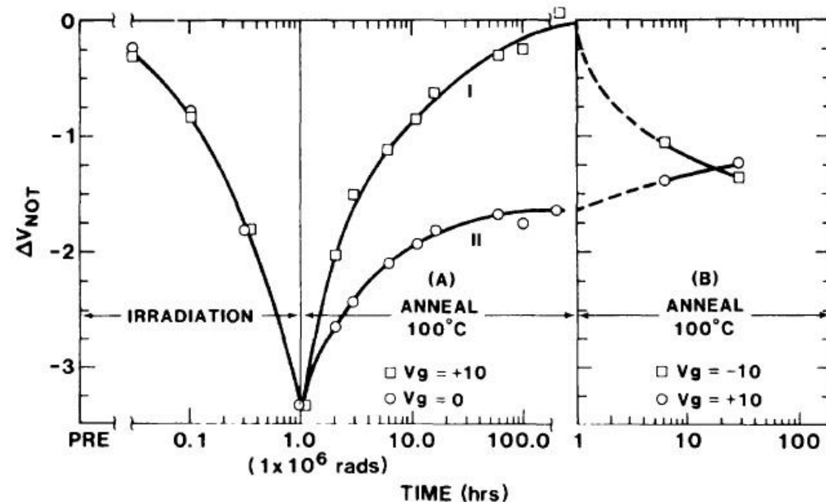
"Rebound" can be undone because the electrons are weakly bounded to the Si atom (defect) and then, they can be released and tunnel back into the silicon (SCHWANK, 1984). Figure 2.4 shows the impact of radiation on the V_{TH} caused by trapped oxides, during irradiation, annealing and "rebound" (SCHWANK, 1984). The radiation dose applied in this experiment is 10^6 rads, where rads is unit of absorbed radiation dose and 1 rads = 100 ergs (unit of energy)/g (unit of mass).

As can be seen in figure 2.4, before irradiation, there is no shift on the V_{TH} and ΔV_{NOT} is zero. During irradiation, ΔV_{NOT} becomes negative due to the holes trapped in the oxides defects at the Si/SiO_2 interface. During the annealing at 100 ºC phase, ΔV_{NOT} reduces due to the bond reformation and rebound process described previously.

Note that figure 2.4 has two curves, I for V_G = + 10V and II for V_G = 0V. The positive gate bias accelerates the annealing process and the reduction of ΔV_{NOT}. It seems that for curve I, all the trapped holes experience bond reformation or were neutralized by electrons from silicon. However, when the gate bias is switched to a negative value of - 10V, ΔV_{NOT} again tends to decrease due to the release of electrons that were initially trapped in the defects - reverse annealing (SCHWANK, 1984).

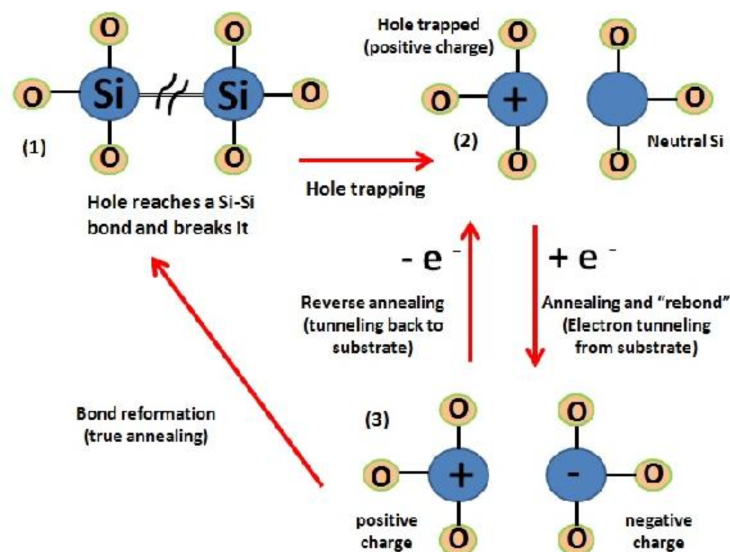
Figure 2.5, shown in (LELIS, 1988), summaries all processes discussed so far: hole trapping, annealing with rebound, reverse annealing (electrons tunneling back to substrate) and bond reformation.

Figure 2.4 - Shift on V_{TH} due to oxide trapped charge (ΔV_{NOT})



Source: (SCHWANK, 1984)

Figure 2.5 - Model of hole trapping, true annealing (bond reformation), "rebound" and reverse annealing



Source: the author, modified from (SCHWANK, 1984)

2.2 Interface state charges

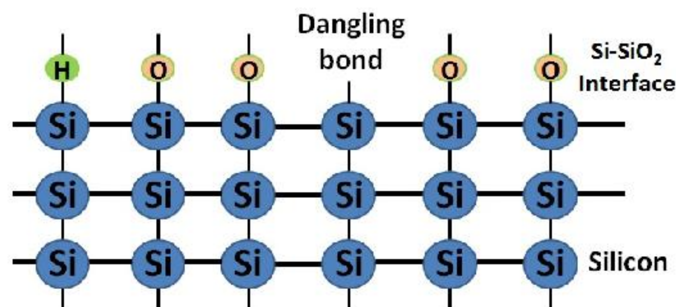
Ionizing radiation also results in interface states (or interface traps) located exactly at the Si/SiO_2 interface (SCHWANK, 1984). The interface state, shown in figure 2.6, is trivalent Si back-bonded to other 3 Si atoms but with a dangling bond extending into the oxide (LENAHAN, 1983). This defect can be either donor like (positively charged when empty and

neutral when occupied by an electron) or acceptor like (neutral when empty and negatively charge when occupied by an electron) (MCWHORTER, 1985). Note that figure 2.6 shows a bond Si-H that is produced after hydrogen passivation.

These defects leads to a loss of current drive capability, degradation of noise margin and mobility (FLEETWOOD, 2013). Defects induced by radiation are similar to those ones induced by fabrication process (OLDHAM, 2003).

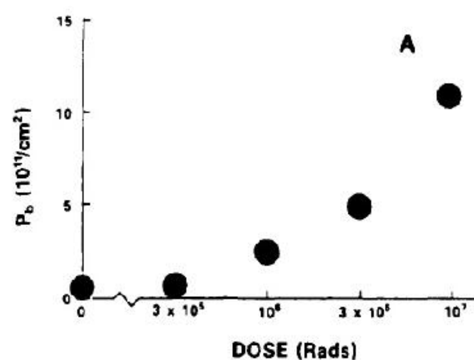
A incidence of protons caused by radiation process (in the form of H+) can break Si-H bonds at Si/SiO_2 interface, and results in H_2 and a trivalent Si defect (unpassivated dangling bond) (FLEETWOOD, 2013). The gate bias polarization during the irradiation process affects the number of defects that is produced by the radiation (*i.e.* positive gate bias results in more defects). Figure 2.7 (OLDHAM, 1989) shows that the number of interface state density (or dangling bonds defects) increases with the radiation dose.

Figure 2.6 - Dangling bond and Si-H at Si-SiO_2 interface



Source: the author

Figure 2.7- Interface states density (P_b) versus radiation dose



Source: (OLDHAM, 1989)

Besides the reaction of protons with hydrogen-passivated defects mentioned above, radiation-generated holes can release hydrogen trapped in the oxides and also creates interface

traps (SCHRIMPF, 2007). Moreover, it was found that the interface-trap formation does not depend of direct ionization radiation at the Si/SiO_2. The positive charge transport through the SiO_2 results in trap formation if the electron-holes pairs are generated at the interface or at the top of the oxide gate (FLEETWOOD, 2013).

Radiation-induced interface traps tend to be acceptor like in the upper half of the Si Bandgap and donor like in the lower half of Bandgap. For NMOS, the Fermi level is above midgap at V_{TH}, so the donor like traps in the lower half of bandgap are filled and neutral, while the filled acceptor like traps above midgap are negatively charged. When Fermi level is located at midgap, the net charge in the traps is nearly zero (SCHRIMPF, 2007).

Consequently, radiation interface states at Si/SiO_2 interface with applied positive gate bias (V_{GS} V_{TH}) trap electrons and becomes negatively charged. The effect of the trapped negative charges at the Si/SiO_2 interface is a positive shift on the V_{TH} ($\Delta V_{TH_}TID > 0$). Since the number of created defects is bias dependent (OLDHAM, 2003), ΔV_{TH_TID} is also a function of the V_{GS} during irradiation. The increase of V_{TH} due to interface states is shown in figure 2.2 by the dotted line.

The total shift on threshold voltage (ΔV_{TH_TID}) is given by equation (2.1) (SCHRIMPF, 2007):

$$\Delta V_{TH_TiD} = \Delta V_{NOT} + \Delta V_{NIT} \quad (2.1)$$

It is meanly composed by two components due to: oxide trapped charges (ΔV_{NOT}) and the interface state charges (ΔV_{NIT}), given by equations (2.2) and (2.3), respectively:

$$\Delta V_{NOT} = -\,Q_{OT}/C_{OX} \quad (2.2)$$

$$\Delta V_{NIT} = -Q_{IT}/C_{OX} \quad (2.3)$$

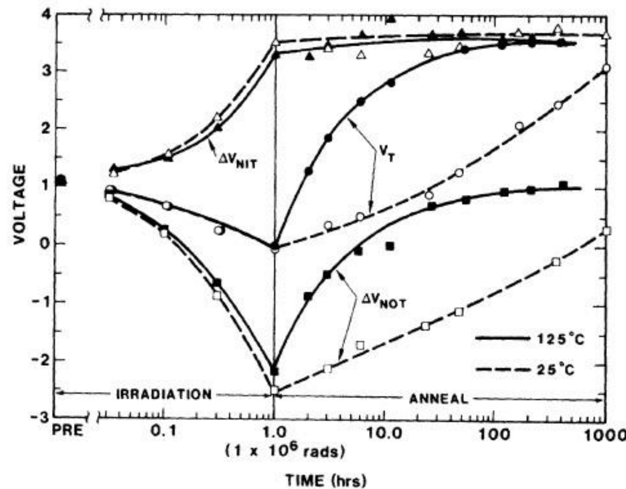
Q_{OT} is the oxide trapped charge density considering that all charges are projected to the interface, Q_{IT} is the area density of charge in the interface traps at $V_{GS} > V_{TH}$ (note that charges in interface states depends on surface potential), and C_{OX} is the gate oxide capacitance (SCHRIMPF, 2007).

Figure 2.8 (SCHWANK, 1984) shows V_{TH} (named as "V_T" in this figure), ΔV_{NOT} and ΔV_{NIT} during irradiation and annealing processes. The x-axis is given in hours, and the irradiation process occurred during 1 hour. V_{GS} for the NMOS device was fixed +10 V

during both irradiation and annealing process for this experiment with 4/3 μm polysilicon gate process with a thick gate oxide of 450 Å.

In Figure 2.8, V_{TH} of a NMOS transistor before irradiation is around 1 [V]. As discussed early, ΔV_{NOT} is negative due to trapped holes in the oxide, and ΔV_{NIT} is positive due to trapped electrons in the radiation induced interface states. The final value of ΔV_{NOT} does not depend on the gate bias, while ΔV_{NIT} is higher for positive gate bias. During the annealing, ΔV_{NOT} decreases due to the bound reformation, and its reduction is faster for high temperatures but saturating in the same value independently of annealing temperature. The annealing has very little effect on the number of defects in the Si/SiO_2 interface, and thereafter, ΔV_{NIT} remains practically constant during the annealing phase.

Figure 2.8 - V_{TH} , ΔV_{NOT} (trapped oxides) and ΔV_{NIT} (Interface state charge)



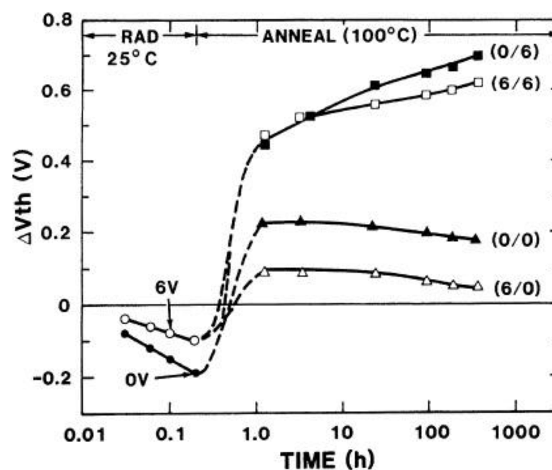
Source: (SCHWANK, 1984)

As the ΔV_{NOT} tends to zero, one can say that the final value of V_{TH} after annealing is higher than the pre-irradiated value and it is entirely defined by the interface state charges. The fact of having the final irradiated V_{TH} larger than the pre-irradiated one is named as "super-recovery" (JOHNSTON, 1984). During the irradiation phase, there was a compensation among the positive charges trapped in the oxides and the negative charges trapped in interface states, and as thus, ΔV_{TH_TID} is not so large as it is in the annealing phase.

In the above example, positive gate-source voltage = +10 V was fixed during irradiation and annealing because it represents the worst-case TID response for this thick oxide process. As mentioned early, ΔV_{NIT} is higher for positive gate bias.

More precisely, there is a complex interplay between oxide and interface traps, and a large built-in electric field that can lead to more negative initial ΔV_{TH_TID} for zero-gate bias at irradiation, and more positive ΔV_{TH_TID} for positive bias during annealing (FLEETWOOD, 2013) and (FLEETWOOD, 1987). It happens because more interface states are build up under zero gate bias during irradiation (FLEETWOOD, 1987). Figure 2.9 shows the mentioned scenario for a NMOS devices irradiated to 200 krad and annealed at 100 ºC for thin-gate process.

Figure 2.9 - ΔV_{TH_TID} during rad. and anneal for 32-nm CMOS process



Source: (FLEETWOOD, 1987)

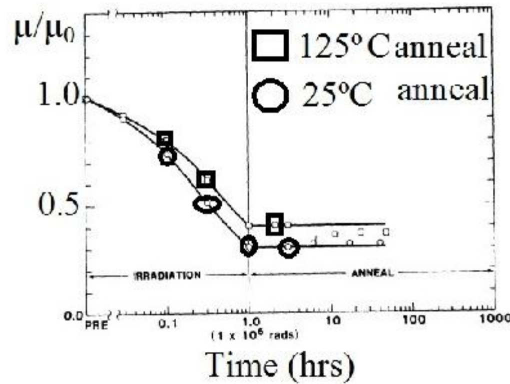
2.3 Mobility degradation

The inversion-layers mobility also changes significantly due to Coulomb scattering from radiation-induced charges, whether trapped holes in oxide or trapped electron in the interface states, although the last one has more impact because it is closer to the inversion-layer (SCHRIMPF, 2007).

Figure 2.10 shows the ratio of mobility before and after irradiation (μ/μ_0) for NMOS devices implemented in 4/3 µm polysilicon gate process (SCHWANK, 1984).

As can be seen in figure 2.10, mobility is decreased by roughly 60% due to the large amount of interface state charges. Mobility is not affected by the annealing phase because the number of interface states is not affected.

Figure 2.10 - Mobility ratio before and after irradiation (μ/μ_0)



Source: (SCHWANK, 1984)

2.4 Impact of transistor scaling on the radiation effects

Before discussing the impact of scaling on radiation effects, it is important to mention that the radiation effects in CMOS devices (*e.g.* shift on V_{TH} and μ degradation) do not normally depend on the dose rate, except in the case of extremely short intense nuclear-drive pulses (OLDHAM, 2003). The apparent dose rate effects are often observed if a given dose is delivered at two or more different rates test only because the exposure time are different (OLDHAM, 2003) and (JOHNSTON, 1984). Therefore, the threshold-shift due to the oxides and interface traps suffered by two identical transistors irradiated at low and high dose rate, followed by equivalent biased annealing, tends to be similar (FLEETWOOD, 2013).

In addition, the sensibility of transistors to the radiation depends on devices geometries and doping profiles, therefore varying between different technological nodes and even between different process of the same technological node (SCHRIMPF, 2007).

In the recent CMOS technologies, the effects of oxide-trapped charge tends to be reduced because of the small volume in which charge is generated. The oxide trapped charge density Q_{OT} in equation (2.2) is proportional to t_{OX}^{2}, and since t_{OX} is scaling, ΔV_{NOT} tends to be reduced (SCHRIMPF, 2007) and (OLDHAM, 2003).

Moreover, due to the very thin gate oxide, electrons can tunnel from silicon substrate to the oxide, therefore possibly neutralizing all positive charges trapped in the oxide (FLEETWOOD, 2013). And besides that, the tunneling of electrons into the gate allows recombination before converting holes into interface states (GROMOV, 2007).

In (GAILLARDIN, 2013), an irradiation experiment with intention of demonstrating the weak effect of trapped charges in oxide on the performance of 3.3 V I/O transistors of a commercial 0.18 µm CMOS process were carried out. Enclosed layout transistors were used in order to exclude the effects of trapped charges on shallow trench isolation (discussed in the next section). No significant shift on the threshold voltage was observed after a total dose of 1 Mrad in the SiO_2.

In the other side, advanced CMOS processes use high-k dielectrics materials (*e.g.* HfO_2, ZrO_2) that tend to be thicker, more defective and with more traps than high-quality SiO_2 gate oxides (FLEETWOOD, 2013).

Other negative aspect regarding radiation of advanced CMOS process is that the gate leakage current started to become an issue for irradiated circuits (BARNABY, 2006). In (SCARPA, 1997), it is shown that PMOS capacitors with t_{OX} of 4.4 nm experience an increased gate current leakage due to the creation of defects in the SiO_2 caused by irradiation, which can lead to trap-assisted tunneling current

The most susceptibly region in circuits implemented in advanced CMOS process (*e.g.* l 250 nm) is the shallow trench isolation (STI) (GAILLARDIN, 2013). The isolation oxide is used to prevent leakage between neighbor devices and it was previously implemented by means of LOCOS (Local Oxidation of Silicon) in old CMOS processes. STI trenches have their thicknesses range from 300 to 450 nm (BARNABY, 2006) in advanced CMOS process. The designed circuits in this thesis were implemented using IBM 130 nm CMOS process that uses STI as isolation oxide.

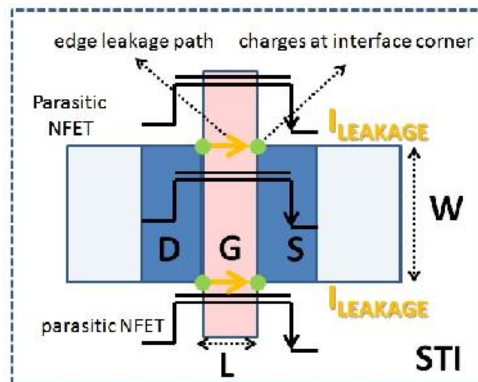
2.5 Shallow Trench Isolation, subthreshold slope and leakage

The thick oxides isolation structures, STI, are the most radiation sensitive regions in CMOS modern circuits and the effects of trapped charges in this oxide dominates the radiation response of the irradiated transistors.

For a NMOS device, positive charges trapped in STI structures induce negative charges in the nearby silicon that result in parasitic paths between source and drain terminals, or between terminals of two adjacent devices (*i.e.* inter- and intra-device leakages). The parasitic paths results in large increase on the leakage current and power consumption (SCHRIMPF, 2007).

Figure 2.11 shows a top view of NMOS with the edge leakage path connecting the source and drain terminal. Positive charges are trapped at the interface corner of STI, poly and active channel (indicated in the figure) and induces a inversion path exactly in the edge of the transistor. There is leakage not only in the intersection of Poly/Active channel/ STI sidewalls, but also in deep in the bulk along the STI/active channel (NIU, 1999).

Figure 2.11 - Top view of NMOS with STI and the edge leakage path

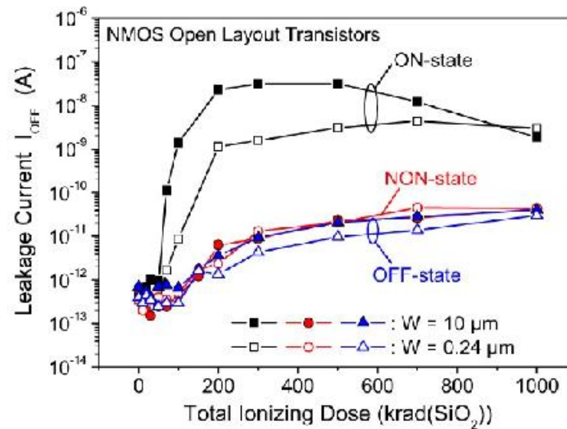


Source: the author, modified from (NIU, 1999).

$I_{LEAKAGE}$ shown in the figure 2.11 is the most contributor to the increased off-state (*i.e.* $V_{GS} < 0$ for NMOS transistors) I_{DS} leakage current of irradiated transistors (FLEETWOOD, 2013). It can be around 100 nA at 500 krad of total dose in NMOS devices with minimal dimensions implemented in TSMC 0.18 µm process (ESQUEDA, 2005). One can model these drain-source parasitic path as "parasitic NFETs" (GAILLARDIN, 2011), shown in figure 2.11. Other leakage paths created by the irradiation are drain-to-source terminal of two different transistors, and source-to-well leakage between two devices - although these two components are not significant (*e.g.* less than 1 nA after 500 krad(SiO_2)) (BARNABY, 2006).

Figure 2.12 in (GAILLARDIN, 2011) shows the drain-source leakage current with V_{GS} = 0 [V] for two transistors with different aspect ratios: W/L = 0.24 µm/0.34 µm (filled symbols) and W/L = 10 µm/0.34 µm (emptied symbols). The irradiation was done with 3.3 V I/O NMOS of a commercial 0.18 µm CMOS process for three bias conditions: ON-state (V_{GS} = 3.3 V), OFF-state (V_{GS} = 0) and NON-state (V_{GS} = -3.3 V) for several total dose steps. As can be seen in figure 2.12, the irradiation carried out with transistors biased V_{GS} = 3.3 V (ON-state) was the worst case scenario and the parasitic conduction channel increased the leakage current by about three orders of magnitude after 100 krad.

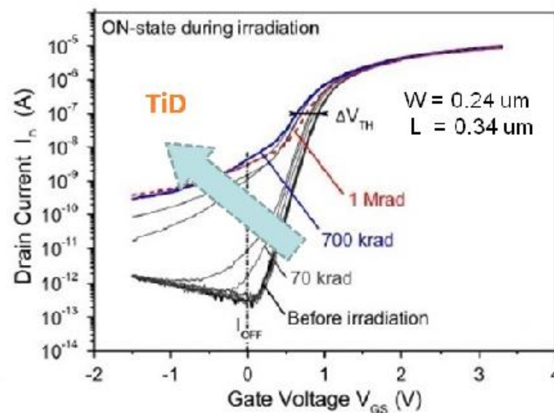
Figure 2.12 - I_{OFF} at $V_{GS} = 0$ of NMOS irradiated under three bias conditions



Source: (GAILLARDIN, 2011)

Besides the increased off state current ($V_{GS} = 0$), the subthreshold slope decreases and the MOSFET turns off more slowly after irradiation (MCWHORTER, 1985) and (Ma, 1989). In figure 2.13 (GAILLARDIN, 2011), it is presented I_{DS} versus V_{GS} for W/L = 0.24 µm/0.34 µm transistor. As one can verify, there was a significant reduction of the subthreshold slope and a negative shift on V_{TH} (roughly 300 mV). These effects are results of the positive-oxide trapped charges at the Si/STI interface.

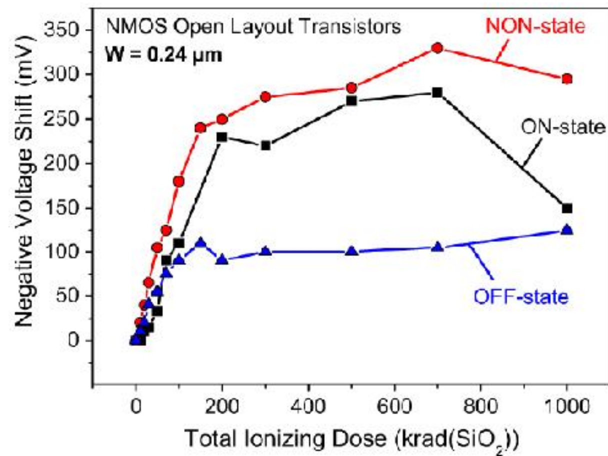
Figure 2.13 - I_{DS} versus V_{GS} of NMOS (W/L = 0.24 µm/0.34 µm) at several total dose steps



Source: (GAILLARDIN, 2011)

In Figure 2.14 (GAILLARDIN, 2011) presents the negative shift on the threshold voltage as a function of TID dose. It is clear that the impact of TID dose on ΔV_{TH_TID} strongly depends on the bias conditions during irradiation. Figure 2.15 (GAILLARDIN, 2011) shows the dependence of the ΔV_{TH_TID} on the transistor size. As can be seen, smaller transistor's width results in higher transistor sensitive to ionizing radiation.

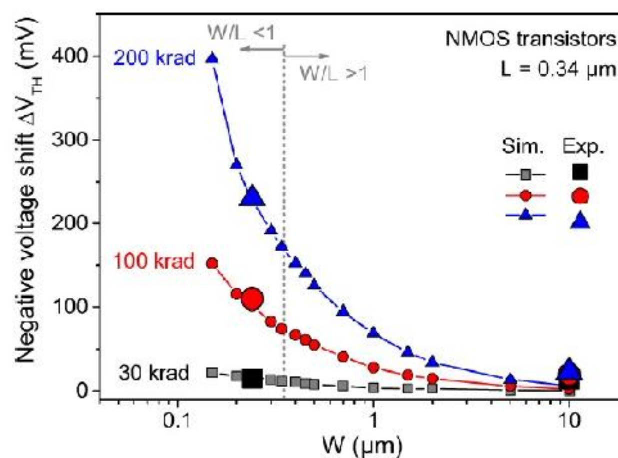
Figure 2.14 - Negative shift on V_{TH} of NMOS for 3 bias conditions



Source: (GAILLARDIN, 2011)

In a more recent work, (GAILLARDIN, 2013) verified that the threshold slope reduction and the threshold voltage shift were significant different for two commercial bulk 0.18 µm processes using STI. The nature and the doping of deposited oxide play an important role in the radiation effects. Moreover, it was shown that interface traps in these bulk 0.18 µm processes significantly annealed. This result is different than that observed for old technologies (thick gate oxide and without STI structures) as discussed in the beginning of this chapter. The annealing of interface traps for thin-oxide technologies with STI is still an open question (GAILLARDIN, 2013).

Figure 2.15- Negative shift on V_{TH} of NMOS as a function of W



Source: (GAILLARDIN, 2011)

2.6 Integrated resistors and 130 nm CMOS technology

In (WILCOX, 2010) is presented an investigation regarding the impact of TID on the resistance of several integrated resistors (*e.g.* high resistance P+ Poly) implemented in a IBM SiGe 5AM BICMOS process. In this experiment, no resistor shows more than 2% change after 1 Mrad of TID. In (AXNESS, 1991), other radiation experiment with integrated polysilicon resistors implemented using 1.25 µm CMOS technology shows no significant effect of TID on the resistor sheet resistance.

In (BOCHENEK, 2012), an investigation of the impact of TID on transistors implemented in 130 nm CMOS technology (the same one used in this thesis) was presented. In that experiment, thin-oxide and thick-oxide transistors were irradiated up to a TID of 100 Mrad using X-ray generator. Next sub-sections present the mean conclusions of that work.

The data bellow will be used as a reference and starting-point for the analysis of the irradiated circuits investigated in this thesis. The impact of TID in our transistors may be slightly different because -ray instead of x-ray was used.

2.6.1 Thin-oxide transistors (1.2 V) - (BOCHENEK, 2012)

Regarding leakage current, ($I_{LEAKAGE}$ = I_{DS} current when V_{GS} ~ 0), (BOCHENEK, 2012) shows that the impact of TID in n-channel devices is greater than in p-channel devices. The leakage was increased by a factor of 25 and 2 (worst case scenario) for minimum W/L thin-oxide n-channel and p-channel transistors, respectively. Moreover, a high increase in the subthreshold swing was also seen for n-channel compared to p-channel devices.

For long-channel transistors, the leakage current (inherently lower) increased in lower rate but still significantly. For instance, typically, the leakage current increase was in the range of one order of magnitude for short channel transistors and of factor 2.5 - 3.0 for transistors with a long channel.

Regarding the shift on the threshold voltage (ΔV_{TH_TID}) caused by TID, short channel transistors were also much more affected than long-channel transistors. Moreover, the magnitude of the ΔV_{TH_TID} decreases with the transistor width. For instance, considering the minimum length n-channel transistor (L = 0.12 µm), ΔV_{TH_TID} ~ - 80 mV for W = 0.16 µm, ΔV_{TH_TID} ~ - 42 mV for W = 0.64 µm and ΔV_{TH_TID} ~ - 20 mV for W = 2.0 µm.

For a long channel transistor n-channel device, (*e.g.* W/L = 10 µm/1 µm), ΔV_{TH_TID} was only ~ -8 mV. All these values were obtained considering the worst case variation in the range of pre-radiation to 100 Mrad. All values of ΔV_{TH_TID} were negative (V_{TH} decreased) for the n-channel transistors. In a different manner, for p-channel transistors, ΔV_{TH_TID} was positive and negative depending of the TID and the device dimensions. For instance, for the minimum size device, ΔV_{TH_TID} varies from -40 mV to + 40 mV for the minimum transistor.

Regarding the variation of I_{DS} (ΔI_{DS_TID}) for a given bias (V_{GS} and V_{DS}), the impact of TID was again much more severe in short channel than long-channel devices. For n-channel devices, the variation was about in the range of +2% to +10%. For the p-channel devices, the variation was about in the range -16% to +7%.

2.6.2 Thick-oxide transistors (2.5 V) - (BOCHENEK, 2012)

Regarding leakage current (*i.e.* I_{DS} when V_{GS} = 0), the impact of TID on thick oxide devices was greater than on thin-oxide devices. Although the initial (pre-irradiation) leakage of thick-oxide transistors (due to the larger V_{TH}) are low (*i.e.* < 10 pA), the overall change reached 3 - 4 orders of magnitude for short channel devices. Long channel devices are less sensitive to the TID effects but still with significant increase of 2 orders of magnitude. The impact of TID are also lower in p-channel than n-channel devices.

Regarding ΔV_{TH_TID}, the impact of TID on thick oxide devices were also greater than on thin-oxide devices. For a short-channel device, ΔV_{TH_TID} ~ - 200 mV was seen for TID of about 3 Mrad. For long-channel devices, the impact on ΔV_{TH_TID} are lower than on short-channel devices, but still significant. Other difference among thick and thin-oxide transistors was the signal of ΔV_{TH_TID}, achieving positive and negative values for the thick oxides. The TID effects on ΔV_{TH_TID} was also lower in p-channel than n-channel devices.

Regarding ΔI_{DS_TID}, variations of about +6% to -16% for short-channel n-channel devices, and about +3% to -30% for short-channel p-channel transistors were observed.

Finally, table 2.1 summarizes the main results obtained in (BOCHENEK, 2012) regarding impact of TID on V_{TH_TID}, I_{DS_TID} and $I_{LEAKAGE}$. These are approximated values extracted from plots.

Table 2.1: TID on V_{TH_TID} (mV) , I_{DS_TID} (%) and $I_{LEAKAGE}$

Device:	Thin oxide (W /L = µm/µm)					Thick oxide (W /L = µm/µm)		
TID (krad)	$\left(\frac{0.8}{0.12}\right)_N$	$\left(\frac{10}{1}\right)_N$	$\left(\frac{10}{10}\right)_N$	$\left(\frac{0.8}{0.12}\right)_P$	$\left(\frac{10}{10}\right)_P$	$\left(\frac{0.8}{0.24}\right)_N$	$\left(\frac{10}{1}\right)_N$	$\left(\frac{10}{1}\right)_P$
ΔV_{TH_TID} (mV)								
100	- 8	-1.5	- 5	~ 0	~ 0	- 37.5	- 6	~ 0
300	- 18	-1.5	-5	~ 0	~ 0	- 72	- 7	~ 0
500	- 20	-6	-5	~ 0	~ 0	- 87.5	- 7	- 3
ΔI_{DS_TID} (%)								
100	+ 0.7	+ 0.2	+ 0.2	+ 0.3	~ 0	+ 1.8	+ 0.1	+ 0.2
300	+ 1.0	- 0.1	- 0.1	+ 0.6	+ 0.1	+ 2.7	~ 0	+ 0.3
500	+ 1.0	- 0.2	- 0.2	+ 1.3	+ 0.2	+ 2.7	- 0.1	+0.4
$I_{LEAKAGE}$ (nA)								
pre-rad	0.5	12	11	n/a	n/a	0.001	0.006	0.02
100	0.6	13	14	n/a	n/a	0.050	0.020	0.03
300	3.0	14	16	n/a	n/a	2	0.5	0.03
500	2.2	23	17	n/a	n/a	10	0.9	0.01

Source: the author, data from (BOCHENEK, 2012)

2.7 Irradiated PMOS

The positive charges trapped in the oxide leads to an increase and decrease of V_{TH} for PMOS and NMOS devices, respectively. Regarding the positive charges in the interface states, for both PMOS and NMOS, the effect is the increase of V_{TH} (BARNABY, 2006). For PMOS, off-state current and drive capability tends to decrease due to the trapped oxide charges and interface states, therefore having the effects added instead of compensated as it occurs in NMOS devices.

PMOS devices were usually considered to be less sensitive to radiation in advanced CMOS process because they don't suffer with sidewall leakage current (GAILLARDIN,

2011). However, recent work (GAILLARDIN, 2011), shows ΔV_{TH_TID} of ~ 400 mV for TID dose of 1000 krad for PMOS I/O devices (thick-oxide) implemented in 180 nm CMOS process.

2.8 Irradiated BJTs

TID causes in BJT´s interface traps formation that increases the surface recombination resulting mainly in the increase of base current and the reduction of the current beta gain (= I_C/I_B). The surface recombination is caused by the interface-trap buildup at the interface of the base-emitter junction and the base oxide (FLEETWOOD, 2013) and (PIEN, 2010).

In (KRIEG, 1999), a radiation hardened silicon gate process, which gate oxides and dielectrics where chosen to minimize TID effects, shows that the base current increases by a factor of 3 for vertical PNP devices.

In (ADAMS, 2014), the post irradiation reduction is proportional to the square root of the total ionizing dose (TID). Experiments were run for 10 V and 40 V vertical NPN BJT implemented in BiCMOS technology. The reduction is worse at lower collector currents, for instance, achieving 35% or 50% of reduction for I_C of about 1 µA. The reduction was 10-15% at high collector current. These reductions were achieve for higher dose (*i.e.* 90 rad(si)second) up to 500 krad. However, for low dose rate up (*i.e.* 0.1 rad(si)/seconds) up to70 krad, the beta reduction was about 10%.

In addition, bipolar also may suffer from device-to-device or collector-to-emitter increased leakage current, as similar to CMOS transistors (SHRIMPFT, 2007).

2.9 Radiation hardening techniques

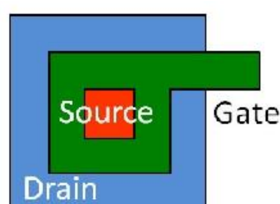
Several techniques were developed in the last years in order to reduce the impact of radiation on CMOS in the fabrication process level (FLEETWOOD, 2013). In parallel, there are also works dealing with design guidelines and recommendation for IC designers.

Guard rings, guard-drains and enclosed layout transistor (ELT) (edgeless) were demonstrated to be efficient against the impact of irradiation (BINZAID, 2008), (NARASIMHAM, 2008). In a ELT layout, shown in figure 2.16, the gate completely surrounds the source of the transistor, avoiding parasitic channels and eliminating the

threshold voltage shift caused by ionizing radiation in field oxides (BINZAID, 2008). The disadvantages of this technique are: (i) the area usage, significantly larger than in the standard approach; (ii) difficulty in modeling ELT transistor, since the W/L ratio is not straightforward and, (iii) the gate and drain source capacitances are larger than in the standard transistors (MALINOWSKI, 2006).

Moreover, guard rings around p-well and n-well are commonly used in order to reduce the triggered single-event latch-up.

Figure 2.16 - Top view of enclosed layout transistor



Source: the author, modified from (BINZAID, 2008)

2.10 TID on the performance of voltage references

As TID effects modify the electrical behavior of transistors, it is expected that precise voltage references are damaged due to irradiation. Many efforts have been done in the investigation of the impact of TID on voltage references (McCLURE, 2001).

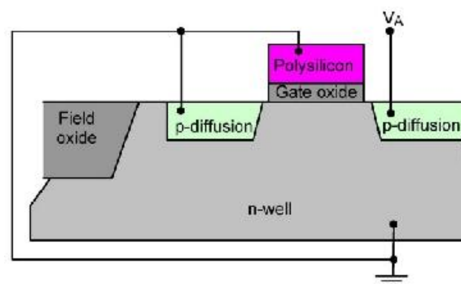
In (PICCIN, 2014), the impact of the layout on the sensibility to TID for a voltage reference circuit is presented. Basically, a couple of key transistors were laid-out in two different configurations, and the output voltage (V_{REF}) had significant difference sensibility to total dose. While voltage reference circuit with layout "A" shows sixteen times higher radiation sensibility ($\Delta V_{REF_DOSE}/V_{REF}$) than the same circuit with layout "B". The circuit with layout "A", presents a radiation sensitivity ($\Delta V_{REF_DOSE}/V_{REF}$) equal to 0.5 % for a dose rate up to 40 krad(Si) using a gamma ray ^{60}Co source. The voltage reference used as case-study in that work were designed in 130 nm CMOS technology and it operates with a minimum supply of 2.5 V while generating V_{REF} = 718 mV.

In (CARDOSO, 2014), voltage references where implemented in SiGe BiCMOS technology - technology commonly used for extreme environment applications. By means of Inverse-mode (IM) BJTs (devices with collector and emitter terminals electrically swapped)

an improved robustness of V_{REF} against radiation was achieved. Moreover, it was shown that the radiation effects were worse for X-ray source when compared to proton-source.

In (GROMOV, 2007), voltage references where implemented in standard 0.13 µm CMOS technology. It was reported that a conventional BGR using not radiation hardened technique achieves ΔV_{REF_DOSE} ~ 4% up to 79 Mrad. In order to decrease this variation, this work proposes to use dynamic threshold MOS diodes as shown in figure 2.17. Note that the gate, drain and n-well devices are shorted together.

Figure 2.17 - Cross section of dynamic-threshold MOS diode



Source: (GROMOV, 2007)

Conventional diodes are usually implemented using p-diffusion in nwell, with a shallow trench surrounding the active area (GROMOV, 2007). As discussed early, irradiation induced holes get trapped in the body of the field oxide and modifies its electrical behavior of the diode. The objective of using dynamic threshold devices were to avoid the proximity of STI to the body of the diode.

The first reference implemented in (GROMOV, 2007) uses open layout (traditional one) and dynamic diodes while achieving ΔV_{REF_DOSE} ~ 3% (12 mV) up to 40 Mrad (SiO_2). A second reference was implemented using enclosed layout and dynamic diodes, and the achieved ΔV_{REF_DOSE} was 1% (1.5 mV) up to 44 Mrad - (four times improvement when compared to the case without any radiation hardening technique).

In (McCLURE, 2013), a traditional bandgap reference composed by an amplifier, two diodes, current mirror and three resistors was implemented using 180-nm CMOS technology. Two extra versions of the reference using radiation hardening technique were also implemented. The first version implements the PN diode by means of dynamic-threshold MOS diode (figure 2.17). The second version uses the MOS diode and all other transistors with enclosed layout technique.

The traditional implementation using no radiation hardening techniques suffers complete failure (V_{REF} goes to zero) at TID between 50 and 100 kRad. The version using only MOS diode instead of PN diodes and no enclosed layout presented V_{TH_TID} around 130 mV what is a critical damage. Only the circuit version using MOS diode and enclosed layout achieved improved radiation robustness of V_{TH_TID} ~ 6 mV.

Table 2.2 summaries the impact of radiation on several BGR references. As these circuits have different topologies and were implemented in different technologies, the objective here is only to give an idea of ΔV_{TH_TID} instead of making a one-to-one comparison. RHBD stands for Radiation Hardening By Design, and it means that some technique was used in order to improve the circuit robustness against TID effects.

Table 2.2: Impact of TID on V_{REF} (V_{TH_TID}) of voltage references

Work	V_{REF} (V)	ΔV_{TH_TID} (mV)	ΔV_{TH_TID} (%)	Dose (krad)	Type	Process
(CARDOSO, 2014) No RHBD	1.083	28	2.5	2000	X-ray	SiGe BiCMOS 90-nm
(PICCIN, 2014) No RHBD	0.718	7	1	150	-ray	Bulk CMOS 130-nm
(MCUE, 2013) No RHBD	1.172	Failure	Failure	300	-ray	Bulk CMOS 180-nm
(MCUE, 2013) w/ MOS diode	1.024	130	10	300	-ray	Bulk CMOS 180-nm
(MCUE, 2013) w/ MOS diode and Enclosed layout	1.015	5.4	0.5	300	-ray	Bulk CMOS 180-nm
(CARDOSO, 2014) w/ Inverse-mode BJT	1.061	16	1.5	2000	X-ray	SiGe BiCMOS 90-nm
(GROMOV, 2007) w/ Enclosed layout	0.405	12	3	44000	X-ray	Bulk CMOS 130-nm

Source: the author

3 FLICKER AND RTS NOISE

MOSFET devices implemented in recent CMOS technologies (*e. g*. gate length of around 90 nm) have noise corner frequencies (f_C) approaching tens of MHz (BREDERLOW, 2006). Corner frequency is defined as the intersection point in the noise spectrum of the MOSFET where the power of flicker noise and thermal noise becomes equal (RAZAVI, 2001). Bipolar transistors have lower flicker noise corner frequency, around 1 kHz (Agilent, 2012) and due to this, the bipolars are employed in very-low noise applications.

Flicker noise of MOSFETs is basically related to the trapping/de-trapping process of minority carriers into/from traps located inside the gate oxide or at silicon-oxide interface. In MOSFETs, there are basically three types of traps considering the physical location of the defect: border traps (or "near interface"), interface traps and oxide traps. Border traps and interface traps are the responsible for the flicker noise, but being the first one the most contributor (FLEETWOOD, 1996). These two types of traps are called "switching states" due to the ability of exchanging charges with the Si (BARNABY, 2006). Interface traps are located exactly at the Si-SiO_2 interface, while border traps are located at the first monolayers of the SiO_2 (*e.g.* ~ 3 nm from the interface) (BARNABY, 2006).

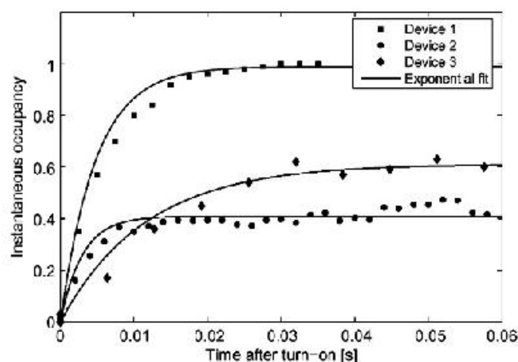
In the SiO_2, located above the border traps, there are oxide traps. Oxide traps have low probability of exchanging charges with Si due to its distance from the inversion layer. They do not contribute significantly to 1/f noise and are normally called "fixed states" (FLEETWOOD, 1996).

Flicker is then proportional to the number of available traps. Each trap is characterized by its switching time constant ( ), and different traps have different values of (BREDERLOW, 1999). More specifically, can classified as trapped state constant ($_e$) and empty state constant ($_c$) The first one, $_e$, is related to the duration of the trapped state or the mean time before the emission of charge occurs. The empty state constant, $_c$, is related to the duration of the empty state or the time constant for charge capture (VAN DER WEL, 2007).

Both $_e$ and $_c$ are instantaneous functions of the gate-source bias (V_{GS}). As for instance, it was found that for n-channel devices as V_{GS} is decreased, $_e$ decreases and $_c$ increases, leading the trap to be empty during more time (VAN DER WEL, 2007). Figure 3.1 shows the trap instantaneous occupancy for three different transistors after V_{GS} to be turned on (VAN DER WEL, 2007).

In this experiment, the device is turned on (V_{GS} higher than V_{TH}) in time 0, and after that, the trap reach their steady-state occupancy in a exponential fashion, indicating that the trap time constant is a function of gate bias (VAN DER WEL, 2007).

Figure 3.1 - Trap instantaneous occupancy after turn-on of V_{GS}



Source: (VAN DER WEL, 2007)

Going back to the origin of 1/f noise, it was mentioned that its origin is caused by the trapping/de-trapping of minority carriers, therefore causing a fluctuation of the number of free carriers (ΔN) at the interface of Si-SiO_2. This statement is actually a common simplification of the phenomenon that possibly really happens in Si. The fluctuation of the number of free carriers also cause fluctuations on the carrier mobility (Δμ) in the transistor channel due to the changes in the local electric field (VAN DER WEL, 2007).

Therefore, the trapping/detrapping mechanism results in variation of drain-source current (ΔI_{DS}) because: (i) a charge that is trapped no longer takes part in the conduction, and (ii) the trap that captures a carrier becomes charged by doing so, and this may modulate the position of the channel in the vicinity of the trap, thereby changing the macroscopic mobility of the device. The impact of the charged trapped depends on its position regarding in long of the channel. For example, traps located near drain terminal have negligible impact of 1/f noise of the transistor depending on transistor bias and technology (VAN DER WEL, 2007).

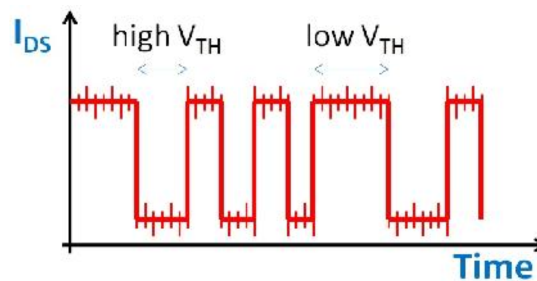
Since the number of traps and its location along the channel in the transistors varies accordingly to the fabrication process, 1/f noise shows extreme variability, especially for small-area devices. Flicker noise can vary more than 1 order of magnitude between different nominally identical devices (BREDERLOW, 1999). Regarding the energy level of traps, it is worth mentioning that trap densities in MOSFETs are commonly U-shaped in energy (DA SILVA, 2008). This means the most part of traps are located near the conduction and valance band edges, and only few traps are located near the mid gap.

3.1 Random Telegraph Signal (RTS)

On small submicrometer MOSFETs (*e.g.* active areas less than 1 μm^2), the number of traps can become so small that may have only trapping-emission of a single trap. In this case, the transistor flicker noise is called "random telegraph signal" (DIERICKX, 1991). The 1/f noise in large transistors can be considered as a superposition of many RTSs (DIERICKX, 1991). Figure 3.2 shows the impact of a single trap on the I_{DS} of a transistor.

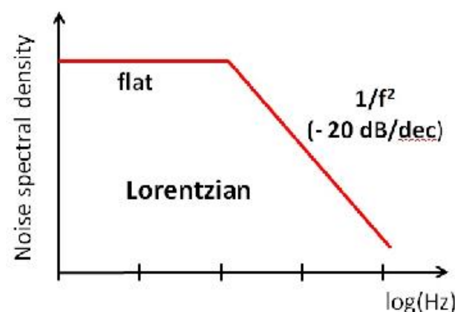
The two levels of I_{DS} shown in figure 3.2 are related to the capture or emission of charge in a single trap. When charge is trapped, the current is low and this electrical behavior can be interpreted (or modeled) as a increase in the transistor threshold voltage (high V_{TH} state). When the trap is empty, the current is high and this electrical behavior can be interpreted as a decrease in the transistor threshold voltage (low V_{TH} state). Extending this concept, if a transistor has eight traps along the channel, for example, therefore I_{DS} and V_{TH} would present eight possible levels (one for each trap). Fluctuations during a specific state show in figure 3.2 refer to the other sources of 1/f noise and other noises (BREDERLOW, 1999).

Figure 3.2 - Impact of single trap on I_{DS} for a MOSFET (RTS noise)



Source: the author, data from (DIERICKX, 1991)

Figure 3.3 - Power spectral density for a single trap



Source: (BREDERLOW, 1999).

The noise spectrum of large area devices with many traps has 1/f dependency and it was shown in figure 1.2. For a single trap, the power spectral density (PSD) of noise, shown in figure 3.3, has Lorentzian shape: flat at low frequencies and proportional to $1/f^2$ at high frequencies (BREDERLOW, 1999).

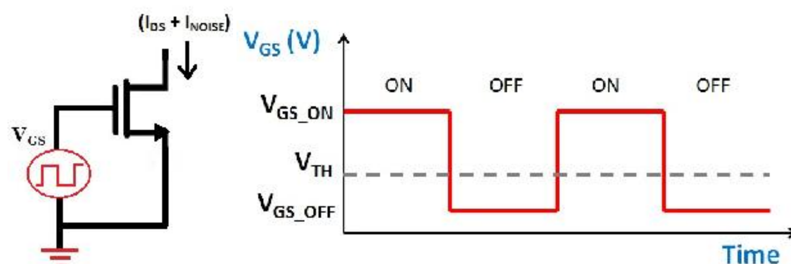
3.2 Flicker noise under switched bias (cyclostationary operation)

As discussed early, the switching time constant ( ) of traps depends on (is modulated by) V_{GS} (ŠIPRAK, 2009). As flicker noise is generated by the trapping/de-trapping mechanism, noise also becomes a function of V_{GS}. This dependence is especially important for circuits with transistors have their gate bias voltage constantly varying over time, as for instance, oscillators.

Figure 3.4 shows a switching bias voltage applied in the gate of NMOS. The input voltage applied to the gate terminal is switched between high and low levels during a pulse with 50% duty cycle. High level corresponds to $V_{GS} > V_{TH}$, whereas the low level corresponds to $V_{GS} < V_{TH}$ (transistor in moderate inversion, weak inversion or in accumulation).

Since flicker noise is a function of V_{GS}, transistor noise in switched bias condition is different from DC bias condition. (Bloom, 1991) was the first work to show that cycling a MOS transistor between strong inversion (V_{GS_ON}) and accumulation (V_{GS_OFF}) leads to a flicker noise reduction by a factor of 1.5 at 1 Hz. Moreover, it was also shown that the intensity of noise reduction depends on the V_{GS_OFF}. Lower V_{GS_OFF}, lower noise is generated because the device goes deeper in accumulation mode.

Figure 3.4 - Switching bias applied in the transistor gate



source: the author

The second work to show noise reduction in MOSFETs when cycled between inversion ($V_{GS} > V_{TH}$) and accumulation (V_{GS} 0) was (DIERICKX, 1991). For NMOS transistors, the

noise reduction achieved an average factor of 8.4 (at 1 Hz), while for PMOS, the reduction factor was 3.9.

When NMOS transistor is biased in accumulation, traps are forced to release the captured electrons, that then go to recombination with accumulation holes. In accumulation, the density of free electrons in the channel is negligible (ZANOLLA, 2010). This mechanism represents a reduction of $_{e}$ (trapped state) and an increase of $_{C}$ (empty state) (DIERICKX, 1991) and as thus, flicker noise is reduced.

It was also show in (DIERICKX, 1991) that the switching bias cannot completely eliminate RTS noise. A residual RTS noise above the thermal noise is still caused by other 1/f noise sources.

In (VAN DER WEL, 2000), 5 - 8 dB reduction of intrinsic 1/f noise power density is found for different transistors when switching bias is applied in the gate of these transistors. It was shown that the noise reduction was independent of the switching frequency (up to 1 MHz). The period T of the switching bias must be only smaller than $_{c}$ and $_{e}$, in such way that the traps in the device never reaches its steady-state occupancy (VAN DER WEL, 2007).

As similar done by (Bloom, 1991), (VAN DER WEL, 2000) shows also that the noise reduction is a function of the V_{GS_OFF}. That is, lower V_{GS_OFF}, higher is the noise reduction. For example, for $V_{GS_OFF} = V_{TH}$, this work achieves a noise reduction of roughly 6 dB, but when V_{GS_OFF} = zero, the noise reduction becomes 8 dB.

(GIERKINK, 1999) was one of the first works that reduced the phase noise of a ring-oscillator by means of flicker noise reduction of their devices using switching bias scheme. More specifically, through a set of resistors connected to the stages of the oscillator, it was possible to control and decrease the gate-source voltage of the MOS transistors during the off state (V_{GS_OFF}). Decreasing V_{GS_OFF} means driving the transistor into accumulation. By means of the control of V_{GS_OFF}, it was possible to achieve a reduction of 8 dB in the phase noise performance of the ring-oscillator.

Other work that explores the phase noise reduction of ring oscillator by means of switching bias is (KLUMPERINK, 2000). The flicker noise reduction and consequently the phase noise reduction were achieved applying a switched bias in the current source of the coupled saw tooth ring oscillator. It was reported nearly 8 dB of noise reduction in 1/f noise spectral density at low frequencies (around 10 Hz) for a NMOS transistor of W/L = 4 μm/0.8 μm (0.8 μm CMOS process). Transistors with the same aspect ratio were used in the design of

the oscillator. In turn, the phase noise was reduced by 8 dB (at 100 Hz of carrier-offset frequency) after applying switched bias than compared to constant bias.

(ZANOLLA, 2010) explains that the comparison of flicker noise of a transistor with constant bias and with switched bias should be understood carefully: "In the switched bias configuration, an intrinsic and trivial reduction of the flicker noise occurs, compared to DC constant bias, due to the fact that the device is off for half a switching period. This gives a 6 dB (factor of 4) reduction in the resulting noise PSD". Therefore, in order to make a fair comparison of transistor noise between (a) constant bias and (b) switched bias, the PSD measured under constant bias should be divided by a factor of 4. All the works cited above that presented comparisons of the noise under switched-bias and constant bias took into account the factor of 4 in their comparisons.

Turning the MOSFET periodically off with a switching frequency f_{SW} larger than the RTS characteristic frequency (f_C, corner frequency), modifies the emission and capture time constants compared to their steady-state, and therefore the trap occupation state becomes a cyclostationary random process (ZANOLLA, 2010). Since the trapping/detrapping process requires finites time, which are larger than the switching period, the trap occupation probably never reaches the value corresponding to constant bias (ZANOLLA, 2010). Note in figure 3.1, that trap occupation requires some time to achieved its steady sate.

3.3 Cyclostationary operation with forward bulk bias during the off-state

Last section shows that cycling a MOS transistor between strong inversion (V_{GS_ON}) and accumulation (V_{GS_OFF}) leads to a flicker noise reduction, and that lower V_{GS_OFF}, greater is the noise reduction. A complementary technique for flicker noise reduction that can be used during the OFF-state of the switched bias configuration is the forward bulk bias, that is $V_{BS} > 0$ for NMOS and $V_{BS} < 0$ for PMOS.

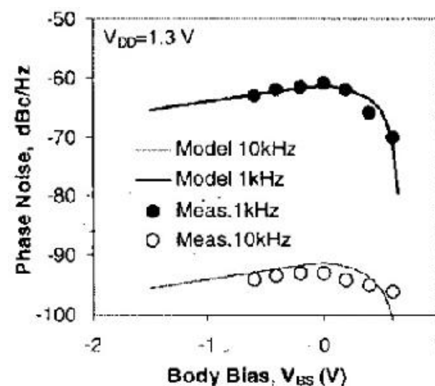
Consider a NMOS with a gate switched bias and $V_{GS_OFF} \sim V_{TH}$ during the OFF mode. If forward bulk bias is applied during the OFF mode (*i.e.* in opposite phase to the gate bias), V_{GB} tends to be reduced and the channel region tends to go transiently to accumulation. Since this bias condition is similar than reducing V_{GS_OFF} (*e.g.* applying zero or negative gate voltage), thus flicker noise reduction is achieved (ZANOLLA, 2010). This technique can be advantageous because it does not required negative gate voltage.

(ZANOLLA, 2010) shows an experiment with forward bulk bias with short channel transistors (L = 0.1 μm) implemented in 0.13 μm CMOS process with only 1 trap per device. The application of forward bulk-bias during off-state of transistors decreases the RTS noise PSD by about one order of magnitude. During the ON state (V_{GS} = VDD), the use of forward bulk bias did not significantly affects the PSD.

Possible issues associated with forwarding bias the body-to-source junction are: (i) increase latch-up susceptibility, (ii) increased junction current, (iii) increased shot noise and (iv) increased voltage gain degradation at a given power consumption related to a reduction of gm/I_{DS} (PARK, 2001). Regarding shot noise, it discussed in (PARK, 2001) that keeping V_{BS} below 0.5 V, this type of noise can be made negligible. Other effect of applying forward bulk bias is the reduction of the transistor depletion width (xd), that results in a increase in C_{CD} (depletion charge capacitance).

In (KAZEMEINI, 2003), the technique of applying forward bulk-bias with intention of reducing flicker noise (and consequently phase noise) was used in the design of a ring-oscillator with 501 stages of CMOS inverters. It shows that the phase noise significantly reduces when forward body bias of V_{BS} = 0.6 volts is applied in the body of NMOS and PMOS transistors during the operation of the ring-oscillator. Figure 3.5 shows the phase noise reduction achieved in (KAZEMEINI, 2003) when forward bulk bias ($V_{BS} > 0$) is employed. There is also a small phase noise reduction for very reverse bulk bias. However, this was not caused by flicker noise reduction but due to the reduced oscillation frequency (due to the larger threshold voltage). The lower frequency, the lower is the phase noise (KAZEMEINI, 2003).

Figure 3.5 - Phase noise of ring-oscillator as a function of V_{BS}



Source: (KAZEMEINI, 2003)

Several works (KWON, 2011), (MARIN, 2004) and (PARK, 2001) also investigated the impact of forward bulk bias on the flicker noise performance during the DC operation of transistor (not switched bias) . It was shown that applying forward bulk bias results in a decrease of 1/f noise for subthreshold voltage, but not in strong inversion. The experiments were carried out changing the bulk bias voltage but keeping a constant I_{DS} (constant V_{GS}) in order to make a fair comparison. The justification was that applying forward bulk bias increases depletion layer capacitance (and decreased depletion charges), therefore broadening of the inversion layer. Increasing the distance between free carriers (at the channel) and the border traps would decrease the trapping and detrapping rates , according to the (PARK, 2001).

3.4 Cyclostationary operation and traditional flicker noise models

Switched gate bias decreases the flicker noise of transistors, as shown in the previous sections. Therefore, some circuit may apply this technique in order to achieve low noise operation, while other naturally works under this conditions, as for instance, oscillators.

Therefore, it is important to properly predict the noise performance of circuit operating in cyclostationary regime. However, IC designers face an issue when simulating circuits with switched bias conditions because the transistor flicker noise models and some electric simulators does not properly predict noise under this condition (VAN DER WEL, 2007) and (PHILLIPS, 2000).

As they don't take into account the noise reduction caused by cyclostationary operation, they are pessimist (AADITHYA, 2013). Simulators like SPICE only predicts a 6 dB of reduction when the transistor is subjected to switching bias conditions that is caused by the off-operation during half of period (VAN DER WEL, 2007). Moreover, the variability of noise and the RTS behavior (2 levels of amplitude distribution) of small-area transistors are also not properly predicted (VAN DER WEL, 2007). As a result, an improved transistor noise model must be developed in order to allow accurate noise reduction predictions (KLUMPERINK, 2000).

Trying to properly predict cyclostationary noise, many efforts have been done. In (ZANOLLA, 2010), a Monte Carlo-based simulator for noise simulation was developed. In (AADITHYA, 2013), two CAD tools, SAMURAI and MUSTARD, in order to proper evaluate the impact of non-stationary RTN on SRAMs and DRAMs were developed. In

(BREDERLOW, 2006), a new low frequency models for MOSFETs working with period large signal excitation was developed.

The Spectre RF simulator, used in this thesis, generates proper simulation results for circuits operating in cyclostationary regime due to their algorithms (PHILLIPS, 2000).

3.5 Cyclostationary noise simulation using Spectre RF

The most common analysis implemented in commercial circuit simulators to simulate output noise of electronic circuits is the ".NOISE". This analysis is available in SPICE and Spectre simulators, for instance. In this analysis, the simulator assumes a stationary operating point and considers that device noise does not alter the operation point. After, the circuit is linearized around the operating point and by means of the superposition principle, the noise is calculated and can be separated from signals (Virtuoso Spectre Transient Noise Analysis - application notes). Analysis ".NOISE" is only valid for DC operation (*e.g.* noise analysis for voltage references).

For circuits that operate under Period steady state (*e.g.* oscillators, mixers and dividers), "PSS\.PNOISE" of Spectre RF is the proper analysis for simulating the circuit output noise. In this type of analysis, the DC operating point is varying in time but the circuit achieved a equilibrium condition. It works similar than ".NOISE", but here the simulator linearized the circuit around the Period state of interest. Small-signal noise analysis allows computing individual contributions of every noise source in the circuit to the output noise spectral density. Composite noise spectral density is calculated afterwards as mean-square sum (Virtuoso Spectre Transient Noise Analysis - application notes).

However, for the case of nonlinear and non-Period circuits (*e.g.* fractional-N PLLs, sigma delta modulators, data converters) the circuit cannot be linearized at the operation point, and the simulation tool for this scenario is the Transient Noise analysis. In this analysis, at each time step, device noise models are evaluated to generate random noise sources that are further injected into transient analysis (Virtuoso Spectre Transient Noise Analysis - application notes). Note that, the device noise model evaluation done at each time step is important because flicker noise is a function of V_{GS} - as mentioned in the beginning of this chapter

The time step is forced to be small to cover all the noise bandwidth. In addition, the simulation has to span large number of Period cycles in order to generate meaningful

statistical characteristics (or the simulation must be repeated many times). Therefore, this analysis requires a lot of simulation time.

For the case of Period circuits, PSS and PNOISE analysis provides the same information of transient noise analysis in less simulation time (Virtuoso Spectre Transient Noise Analysis - application notes) and therefore, it will be mainly used in this thesis.

3.6 Transistor flicker noise model proposed by Wirth and Silva

In order to overcome the limitation of traditional noise device models to properly model the flicker noise under cycle-stationary conditions, a new flicker noise model was proposed by (DA SILVA, 2008). This model computes the contribution of all traps at the Si-SiO_2 interface to the low frequency spectrum when considering the correct density of states of traps distributed at the interface. It is considered that traps in MOS transistors are distributed according to "U"-shaped curves. It means the greater number of traps has energy near the valence or conduction band, while few traps have energy near the middle of the bandgap.

This new flicker noise model was coded and included in the source code of the HSPICE electrical simulator by a student of our group at UFRGS. The modified HPSICE simulator is able to run transient simulation that properly takes into account the effects of the trapping/detrapping mechanism under cyclo-stationary effects. In (BANASZESKI, 2010), the modified simulator was used to simulate the period of oscillation of a three stage ring oscillator.

The simulator basically works as follow:

1) A number of traps in each transistor is chosen by lot following a Poisson distribution,

2) The values of pi (trap property whose values are a random uniform variable, $p1 < p < p2$), the initial state of each trap (occupied or unoccupied) and the bias condition (E_T-E_F), is randomly chosen. Therefore, the value of V_{TH} for these set of parameters, is calculated.

3) The simulation is started based on the netlist created in the previous step using the above information. After each simulation step, the simulator calculated the probability of each trap to change its state based on the current bias conditions.

Based on the probability of each trap to change its state, the simulator chooses by lot if a trap changes it state or not. Therefore, a new netlist is created with the new V_{TH} values, for each transient step.

3.7 Jitter definition

Jitter can be roughly defined as the deviation of the significant instance of a signal from their ideal location in time. The total jitter can be decomposed in two groups: Random jitter and deterministic jitter (AGILENT, 2012). Random jitter has a Gaussian distribution and it is mainly caused by flicker, thermal and shot noise. Determinist jitter does not present Gaussian distribution and it is caused by different sources as cross-coupling problems, bandwidth limitation, improper impedance termination, electromagnetic interference and so on (NATIONAL INSTRUMENTS, 2012). Normally, deterministic jitter sources appear as line spectra in the frequency domain (AGILENT, 2012)].

Based on (NATIONAL INSTRUMENTS, 2012) and (CADENCE-A, 2015), there are several definitions for jitter:

- **Absolute or edge to edge jitter (J_{ee})**: When a Period system has a reference time point, all events can be considered in relation to that time point. For instance, let's consider a transition of the input reference signal at time zero ($t = 0$). Ideally, after a certain delay ($t = t_{delay}$), the output signal should ideally change. However, the real transition affected by noise occurs at ($t = t_{delay} + \Delta t$), where Δt is measured as J_{ee} .
- **Period or Cycle jitter (J_C)**: It is the variation of period with respect of the nominal or average period. It is the RMS calculation of the difference of each period from a waveform average.
- **Cycle to Cycle jitter (J_{CC})**: It is the variation of the period with respect to the previous cycle. It is time differences between successive periods of a signal

Moreover, Time Interval Error (TIE) is a very common metric used when analyzing jitter. TIE is defined as the difference in time between the actual threshold crossing and the expected transition point (HANCOCK, 2004).

3.8 Phase noise definition

Phase noise is the frequency domain representation of the fluctuations in the phase of a waveform caused by time domain instabilities (jitter). For a oscillator, for example, the frequency stability is normally measured as the ratio of the frequency variation by the oscillation frequency ($\Delta f/f_{OSC}$) (CURTIN, 1999).

The output voltage of a real oscillator (V_{OUT}) can be described by (3.1), where a(t) and (t) are amplitude variation and phase noise variation, respectively. The power spectrum of V_{OUT} is shown in figure 3.6. The broadening of the output power is random noise fluctuation caused by thermal, flicker, and shot noise (CURTIN, 1999). Figure 3.6 also shows the power spectrum for an ideal oscillator with no noise.

$$V_{OUT} = [A + a(t)] * cos[2\pi f_0 \cdot t + \varphi(t)] \quad (3.1)$$

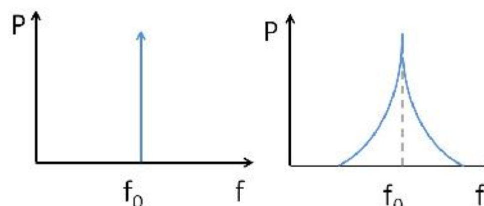
Regarding frequency stability, one can differentiate the long-term and short term stability. The long term refers to hours, days, months, or even year, while the short-term is frequency changes that occurs over a period of a few seconds or less. The short term stability can be random or periodic (CURTIN, 1999).

The short-term stability can be described as single-sideband (SSB) phase noise. The United States National Institute of Standard and Technology defines SSB as the ratio of two power quantities: the power density at a specific frequency offset from a signal carrier and the total power of the carrier signal. Phase noise L (f_m) is given by equation 3.2:

$$L(f_m) = \frac{P_{SSB}}{P_S} \quad (3.2)$$

L (f_m) is the phase noise represented in 1 Hz bandwidth at some frequency (offset) "f" away from the carrier frequency (f_m), PSSB is the power density at "f" frequency and PS is the total carrier power (ZHIQIANG, 2004). The units of measure are in decibels relative to the carrier per Hertz (dBc/Hz) over a 1-Hz bandwidth (CURTIN, 1999).

Figure 3.6- Power spectrum for ideal oscillator (left) and with phase noise (right)



Source: the author, based on (CURTIN, 1999).

3.8.1 Phase noise measurement

The phase noise measurement of a fabricated circuit is not simple task, and is time-consuming because its wide dynamic range (GOLDBERG, 2000). There are a lot of techniques in order to accurately measure the phase noise of oscillators (OVERDORF, 2015) and (DECKER, 2015). However, many of them usually require extra circuits (*e.g.* low noise mixer), different equipments and a lot of calibrations, therefore increasing cost and complexity of the measurements (CHEN, 2010).

The simplest way to measure the phase noise of a oscillator is doing a direct measuring using spectrum analyzer (POOLE, 2015). Although direct measurement has some limitations (GROBBELAAR, 2011) and (ZHANG, 1996), it gives good results in a fast and simple way. Therefore, this technique was planned to be used in this thesis.

As mentioned early, phase noise is usually defined in 1 Hz bandwidth. However, when using spectrum analyzers, the real resolution bandwidth filter (RBW) may not be 1 Hz. The equipment cannot be able to have such narrow filter or the measurement can become extremely slow. For a measurements which RBW is different from 1 Hz, phase noise, L (f_m), can be calculated by equations (3.3) and (3.4) (ZHIQIANG, 2004), (GHEEN, 2012), (AEROFLEX, 2015):

$$L(f_m) = P_{SSB}(f_m) - P_S - 10\log_{10}(B_n) + C \qquad (3.3)$$

$$B_n = 1.064 * RBW \qquad (3.4)$$

RBW is the resolution bandwidth filter of the spectrum analyzer and the term "10 log (B_n)" is used to normalize the results for a 1 Hz bandwidth. The multiplication by 1.064 takes in account the noise bandwidth of the RBW filter. C is the correction factor (usually 2.51 dB) in order to take account peak detector and log display mode errors (CURTIN, 1999) and (GHEEN, 2012).

Finally, when measuring phase noise and jitter in oscillators without any feedback control (free-running configuration) by means of the spectrum analyzer or oscilloscope, respectively, one may be aware about frequency drift caused by micro changes in temperature and supply voltage (YUEN, 2005). If the frequency drift is too large, phase noise, especially at low

frequency offset, cannot be correctly measured (CHEN, 2010). A typical value of frequency variation of a free-running oscillator is about 0.1 ppm per second if the environmental temperature change is less than 1°C in five minutes (YUEN, 2005).

3.8.2 Phase noise analytical models for oscillators

As mentioned above, phase noise is a continuous stochastic process indicating random accelerations and decelerations in the phase ( ) of the oscillation frequency of oscillators (ABIDI, 2006). It is a random variable that is specified by its PSD (Power spectral density).

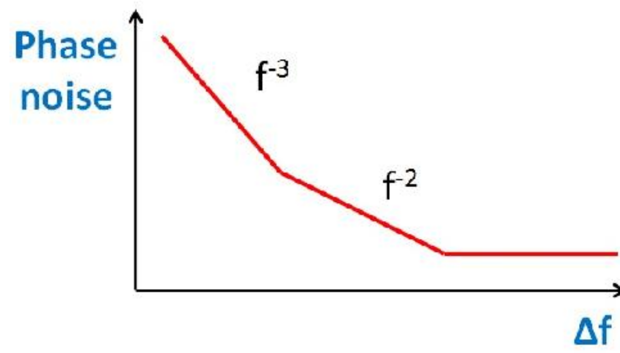
One of the first analytical models to estimate the phase noise of oscillator was proposed by (LEESON, 1996). Many years later, other works developed improved models to predict the phase noise and jitter in oscillators (WEIGANDT, 1994) and (MCNEILL, 1997). However, these models are based on liner time invariant system (LTI) and does not properly account for the cyclostationary effects of noise sources in oscillators (HAJIMIRI, 1998).

One of first works to present a phase noise model based on periodically time varying system nature of oscillators was (HAJIMIRI, 1998). The phase noise model proposed by this work is based on an impulse sensitive function that describes how much phase shift results when a unit impulse is applied in the oscillator. This model properly takes into account both stationary and cyclo-stationary noise sources.

The typical plot of phase noise as a function of offset frequency of carrier for an LC oscillator can be seen in figure 3.7 (HAJIMIRI, 1998). The $1/f^3$ corner in the phase noise spectrum is smaller than 1/f noise corner noise of the transistors used in the oscillator circuit, by a factor determined by the symmetry properties of the output waveform. The flicker noise is up converted and appears as $1/f^3$ dependence on the offset frequency, thermal noise appears as $1/f^2$ dependency. The flat region arises from the white noise floor of the noise sources in the oscillator.

It is important to mention phase noise in figure 3.7 is always negative and there is no sense to have phase noise higher than dBc/Hz for offset frequencies near the carrier (POORE, 2015). Positive phase noise means that noise power would be stronger than the frequency carrier, what there is no physical meaning. Traditional electric simulators (*e.g.* Spectre RF) can estimate phase noise higher than 0 dBc/Hz for offset frequencies near the carrier and the designer must be aware about that.

Figure 3.7- Typical phase noise of a LC oscillator versus offset from carrier



Source: the author, based on (HAJIMIRI, 1998).

4 VOLTAGE REFERENCES - CASE STUDY I

4.1 Concepts

Voltage references (VR) usually generate a temperature compensated V_{REF} using the summation of two voltages with opposite temperature coefficients (TC). The traditional BGR generates V_{REF} described by (4.1), using the summation of a diode voltage (V_D) to a properly scaled Proportional to Absolute Temperature (PTAT) voltage is given by:

$$V_{REF} = V_D + K_{PTAT} \cdot U_T \quad (4.1)$$

The thermal voltage (U_T) is ($k \cdot T/q$); where k is the Boltzmann constant ($1.38*10^{-23}$ J/K), T is the absolute temperature and q is the electron charge ($1.6*10^{-19}$ C). At 300 K, the thermal voltage is ~ 25.875 mV. Thermal voltage is usually generated through the difference between V_D of two diodes with the ratio of emitter areas higher than 1 (V_D). Typically, the required diode (V_D) voltage is generated using parasitic vertical or lateral bipolar transistors.

The constant K_{PTAT} is a temperature-independent (to first order) gain factor needed to achieve the proper temperature compensation, as V_D has a negative temperature coefficient. Voltages with negative TC are referred to as complementary to absolute temperature (CTAT).

If one takes the derivative of thermal voltage with respect to temperature, it is possible to verify that its TC is around + 0.087 mV/°C. For the CMOS process used in this work, the diode has TC roughly -1.7 mV/°C. This value is affected by the absolute value and the TC of the bias current injected on the diode.

Imposing (dV_{REF}/dt) = 0 in (4.1), one can find that the required value of K_{PTAT} should be ~ 20 to achieve the temperature compensation. Constant K_{PTAT} is usually defined by the ratio of two resistances with the same TC, and then, it is weakly influenced by the absolute value of resistance.

Aiming to make the voltage reference functional under low V_{DD}, additional techniques can be used to generate V_{REF} equal to a fraction of V_{G0}, as described by (4.2), where can be adjusted to be less than 1. In (BANBA, 1999), is implemented by means of a temperature independent resistor ratio.

$$V_{REF} = \omega \cdot (V_D + K_{PTAT} \cdot U_T) \quad (4.2)$$

An alternative solution to decrease the supply voltage required by traditional BGR is to replace the diodes by MOSFETs operating in the subthreshold region. In such cases, V_D is replaced by the gate source voltage (V_{GS}) and the generated output voltage is similar to that of (1), as given by:

$$V_{REF} = V_{GS} + K_{PTAT} \cdot U_T \tag{4.3}$$

The value of V_{REF} generated by (3) is given by V_{TH0} and a few process-dependent parameters (COLOMBO, 2014).

If the MOSFET is biased with a current less than a certain technology-dependent value, its gate-source voltage decreases with temperature in a quasi-linear fashion (FILANOVSKY, 2001). This behavior happens when the decrease in the threshold voltage - caused by the increase in temperature - outweighs the effects caused by the decrease in mobility of the carriers (FILANOVSKY, 2001).

The temperature dependence of V_{GS} is given by (4.4) and (4.5) (COLOMBO, 2014). The equations show the linear dependence between V_{GS} and T. Variables K_{T1} and V_{OFF} are BSIM4V4 parameters for temperature coefficient of V_{TH} and offset voltage in subthreshold region, considering very large W and L, respectively (COLOMBO, 2014). K_{T1} and V_{OFF} are equal to -0.4 and -0.078, respectively, for the 130 nm process used in this work.

$$V_{GS}(T) \approx V_{GS}(T_0) + K_G \cdot [(T/T_0) - 1] \tag{4.4}$$

$$K_G \cong K_{T1} + V_{GS}(T_0) - V_T(T_0) - V_{OFF} \tag{4.5}$$

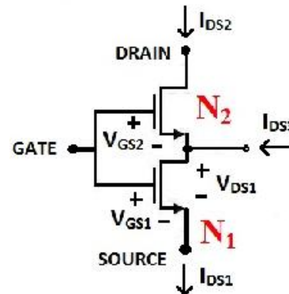
As mentioned earlier, V_D can be used to generate U_T. And an alternative way to generate it is through the difference of gate-source voltage ($V_{GS} = V_{GS1} - V_{GS2}$) of two MOS transistors operating in weak inversion mode (COLOMBO, 2014). The drain-source current (I_{DS}), for transistors working in weak inversion with drain-source voltage (V_{DS}) higher than 0.1 V (saturation operation), is given by:

$$I_{DS} = 2 \cdot n \cdot \mu_0 \cdot C_{OX} \cdot S \cdot {U_T}^2 \cdot exp[(V_{GS} - V_T)/\mathrm{n} \cdot U_T] \tag{4.6}$$

where S = (W/L) is the transistor aspect ratio, n is the subthreshold slope factor (1.1), μ is the effective channel mobility, C_{OX} is the gate oxide capacitance per unit area. The exponential dependence of the subthreshold current I_{DS} with V_{GS} can be used to generate U_T. Therefore, if a self-cascode transistor is used, as shown in Figure 4.1, V_{GS} appears as V_{DS} of M_1. The V_{GS} is given by:

$$\Delta V_{GS} = V_{GSN1} - V_{GSN2} = V_{DS1} = n \cdot U_T \cdot \ln[(S_{N2} \cdot I_{DS1})/(S_{N1} \cdot I_{DS2})] \quad (4.7)$$

Figure 4.1- Self cascode transistor



Source: the author, based on (COLOMBO, 2014)

In figure 4.1, the bulk of devices N_1 and N_2 (not shown in this figure) are connected to the ground. Equation (4.7) considers that both devices are in weak inversion operation and in saturation. The transistor aspect ratio (S_{N2}/S_{N1}) should be greater than 20 in order that N_1 may work in saturation under all conditions.

Note that (4.7) has PTAT behavior and it provides a very good estimation of V_{GS} and its TC. Moreover, it is worth to note that (4.7) neglects the body effect on N_2 and it considers the same threshold voltage for both devices. Although exactly equal threshold voltages cannot be achieved, due to transistor mismatch, the body effect can be avoided if NMOS transistors with isolated p-well are used.

If the bottom transistor of figure 4.1 works in linear operation, the term inside the brackets is summed to 1 as shown in (CAMPANA, 2015).

4.1.1 First-order temperature compensation

It is relevant to mention that the temperature compensation achieved by voltage references whose output voltage is described by equations (4.1), (4.2) and (4.3) is normally called as first order temperature reference. The reason for that is because only the first order (and the most important) term of V_D or V_{GS} voltage is temperature compensated by the thermal voltage. The diode or base-emitter voltage is actually not perfectly linear with the temperature, as described by (4.8) (TSIVIDIS, 2010).

$$V_{BE}(T) = V_G(T) - (T/T_r) \cdot [V_G(T_r) - V_{BE}(T_r)] - (\eta - \delta) \cdot (k \cdot T/q) \cdot \ln(T/T_r) \quad (4.8)$$

$V_G(T)$ is the bandgap voltage at temperature T, is a constant related to the mobility of minority carrier in the base (usually ~ 3.5), T_r is the room temperature (*e.g.* 300 K) and is given by the temperature dependence of the bias current of the bipolar.

As can be seen in (4.8), there is a small term proportional to $-T \cdot \ln(T)$ that is not compensated by U_T. This term is one of the major contributors to the curvature, usually downward concavity, of bandgap output voltages. For most part of the applications the curvature caused by the high-order terms of V_{BE} does not sufficiently degrade the required accuracy of V_{REF}.

In order to compensate the high-order terms of V_{BE}, a third term, usually a squared PTAT voltage is added in equation (4.1) (HSIAO, 2006) and (LEUNG, 2004). In (COLOMBO, 2012-b), the leakage current of a MOSFET with gate-source voltage equal to zero is used to generate a voltage, exponentially proportional to the temperature, with the objective of compensating the high order term of V_{BE}. Simulation results shows that a good temperature performance of 6 ppm/°C at nominal process (TT) can be achieved. Although great performance is achieved at typical conditions, the proposed technique is not robust against the impact of fabrication process variations because the large variability of the subthreshold currents. Thus, (COLOMBO, 2012-b), can be better considered as a didactic example of curvature correction technique.

Gate-source voltage of MOSFET operating in weak inversion also have high-order terms, similarly to equation (4.8) as described in (FERREIRA, 2005). Therefore, V_{TH}-based voltage reference also presents V_{REF} with a curvature, but usually with upward concavity (FERREIRA, 2005). All voltage references designed in this work are of first-order type.

4.2 I_{REF}: PTAT Current Reference

The traditional PTAT current reference, shown in figure 4.2, is used in the design of all V_{TH}-based references implemented in this work. Cascode transistors P_4-P_5 and N_1-N_4 are used mainly to decrease the effects of channel length modulation and increase the robustness of I_{REF} regarding fluctuations of the power supply.

Considering $P_1 = P_2$, the current that flows across R_{PTAT}, (I_{BIAS}) is described by (4.9), where V_{GS} is described by (4.7). I_{BIAS} has PTAT TC since V_{GS} is directly proportional to the temperature.

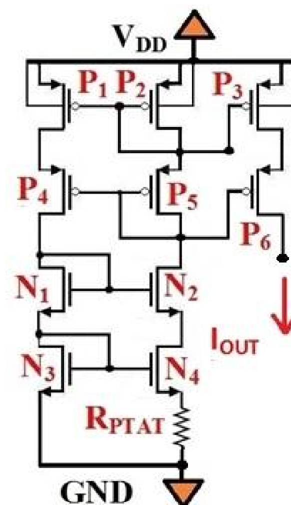
$$I_{BIAS} = (V_{GSN3} - V_{GSN4})/R_{PTAT} \tag{4.9}$$

If I_{BIAS} is required to have very low values of current (*e.g.* few nA), R_{PTAT} can be replaced by a transistor operating in deep linear mode in order to achieve significant reduction in silicon area. The gate of this transistor can be connected to the V_{REF} as shown in (UENO, 2009). As V_{REF} is expected to be stable over temperature and supply voltage, the resistance of R_{PTAT} is expected to not vary significantly over VDD and temperature corners. Using a transistor with aspect ratio of S_R acting as resistor, I_{BIAS} is given by (4.10):

$$I_{BIAS} = (V_{GSN3} - V_{GSN4})/S_R \cdot \mu \cdot C_{OX} \cdot (V_{REF} - V_{TH}) \tag{4.10}$$

Independently of the implementation for R_{PTAT}, this current source has a positive feedback loop and then, stability must be guaranteed keeping the loop gain less than 1. High values of R_{PTAT} (*e.g.* I_{BIAS} less than 1 µA) are usually enough to keep that gain less than 1. In addition, it is desired to design N_4 wider than N_3 (SEDRA, 1997). Table 4.1 shows the size of all devices of I_{REF}.

Figure 4.2 - Current reference with PTAT TC



Source: the author

As the above current reference is used in the design of implemented voltage references, the ability of measuring it separately can contribute for the comprehension of the impact of TID on the voltage references.

Table 4.1: Devices size of I_{REF}

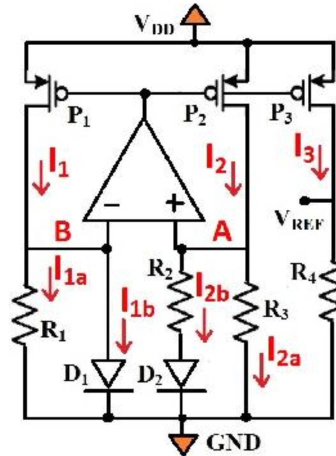
Device	$P_{1,2,3,4,5,6}$	$N_{1,2}$	N_3	N_4	R_{PTAT} (k)
Width (µm)	6	2.5	3	3	98.9
Length (µm)	5	5	8	8	
Multiplicity	2	2	2	10	

Source: the author

4.3 V_{REF}_1: Bandgap-based reference

This circuit was proposed by (BANBA, 1999) and it is shown in figure 4.3. The concept of this circuit is to generate two currents with opposite temperature coefficient (I_{1A} and I_{1B}) and inject them in a balanced way into a resistor.

Figure 4.3 - Low voltage Bandgap reference



Source: the author, based on (BANBA, 1999)

Considering that all the MOS transistors used in the current mirror (P_1-P_3) have the same sizes, $I_1 = I_2 = I_3$ if the channel length modulation effect is neglected. Moreover, if $R_1 = R_3$ and nodes A and B have approximately the same voltage due to the small offset of a high-gain amplifier, one can show that $I_{1b} = I_{2b}$ is given by equation (4.11), where V_D is given by (4.12) and x is the ratio of their diode (emitter) areas.

$$I_{1b} = I_{2b} = \Delta V_D / R_2 \tag{4.11}$$

$$\Delta V_D = (V_{D1} - V_{D2}) = U_T \cdot \ln(x) \tag{4.12}$$

I_{1b} and I_{2b} have positive TC. In turn, currents I_{1a} and I_{2b}, described by (4.13), are proportional to the diode voltage and have negative TC.

$$I_{1a} = I_{2a} = V_{D1}/R_1 \tag{4.13}$$

I_1 is the summation of I_{1a} and I_{1b} and it is described by (4.14). As can be seen, I_1 is a sum of two currents with opposite TC.

$$I_1 = I_2 = I_3 = V_{D1}/R_1 + U_T \cdot \ln(x)/R_2 \tag{4.14}$$

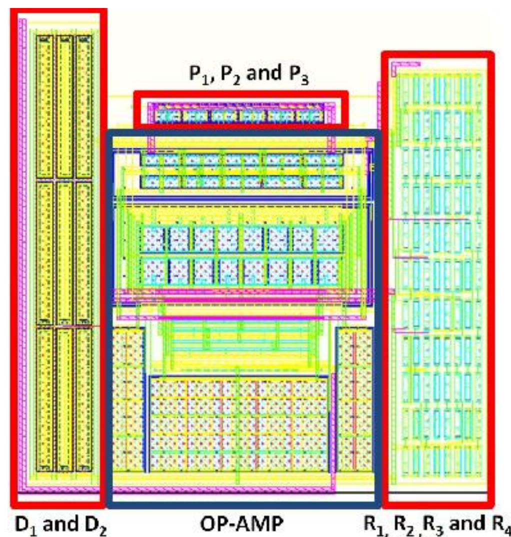
Through transistor P_3, I_3 is injected in R_4 and the generated output voltage of this circuit is given by (4.15):

$$V_{REF} = (R_4/R_3) \cdot [V_D + (R_3/R_2) \cdot \ln(x) \cdot U_T] \tag{4.15}$$

Note that (4.15) is similar to (4.2), where is given by R_4/R_3 and K_{PTAT}, responsible for the temperature compensation, is given by $\ln(x) \cdot (R_3/R_2)$. The value of R_4 is chosen to adjust the V_{REF} to the desired value.

Figure 4.4 shows the layout of V_{REF_1} circuit whose silicon area is approximately 140 µm x 125 µm. Diodes D_1 and D_2, and resistors R_1, R_2, R_3 and R_4 were placed in common centroid configuration.

Figure 4.4 - Layout of V_{REF_1}



Source: the author

Table 4.2 shows the size of all devices of V_{REF_1} circuit. The design of op-amp circuit is discussed in section 4.3.

Table 4.2: Devices size of V_{REF_1}

Device	$P_{1,2,3}$	D_1	D_2	$R_{1,3}$ (k)	R_2 (k)	R_4 (k)
Width (µm)	5	2	2	222.68	20	120
Length (µm)	3	40	40			
Multiplicity	2	1	8			

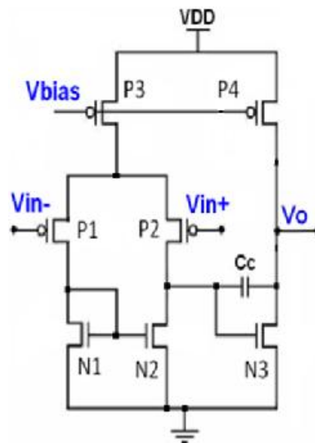
Source: the author

4.3.1 Impact of the operational amplifier on the performance of voltage reference

The operational amplifier used in the designed band-gap reference design is a two stage amplifier with PMOS input transistor and Miller compensation that it is shown in figure 4.5. Current reference I_{REF} (section 4.2) was employed to provide the bias current for the amplifier. A simple operational transconductance amplifier (OTA), symmetrical OTA or a folded-cascode amplifier could also be employed in the design of V_{REF_1} circuit depending on the minimal supply voltage required.

Large gain is the first requirement for the operational amplifier. The higher is the gain, the lower will be the difference between the voltages at nodes A and B ($_{ERROR}$). This voltage error appears at the output voltage amplified by the constant K_{PTAT}, and therefore it can degrades the temperature performance of this VR. Open-loop gain slightly higher than 50 dB is usually enough to guarantee $_{ERROR}$ sufficiently small in such a way temperature performance of the voltage reference is not degraded.

Figure 4.5 - Two stages PMOS input amplifier



Source: the author

The second requirement for the operational amplifier is the offset voltage (V_{OS}). The offset voltage also appears at the output amplified by K_{PTAT}, and therefore, it can increase the TC of V_{REF}. Part of V_{OS} voltage is caused local variations and it can be reduced by increasing the transistor area, while the contribution caused by global variations can be reduced using proper layout matching techniques to compensate for physical gradients, *e.g.* by using a common centroid layout (MONTORO, 2005).

Moreover, a proper design of the differential pair is also important in the offset voltage reduction. Consider that gm_{LOAD} and gm_{INPUT} are the transconductance of the load devices and the input pair. If the ratio of gm_{LOAD}/gm_{INPUT} is reduced, V_{OS} and also the output noise generated by the amplifier are minimized. This recommendation suggests biasing the input devices in weak inversion while load devices operate in strong inversion.

High value of power supply rejection ratio (PSRR) at DC and over the entire bandwidth frequency in which the application is working is also desirable for the op-amp. For the two-stages amplifier used in our design, the PSRR at low frequency is directly proportional to the open-loop gain. However, the bandwidth of PSRR usually decreases with the open-loop gain. Therefore, the open-loop gain should be chosen also taking into account the bandwidth of the external noise that can be coupled at the nodes of the voltage reference circuit.

Table 4.3 shows the transistor sizes for the operational amplifier.

Table 4.3: Devices size of operational amplifier

Device	$P_{1,2}$	$N_{1,2}$	N_3	P_3	P_4	*CC (pF)*
Width (µm)	7.5	0.2	0.2	5	5	20
Length (µm)	7	9	9	5	5	
Multiplicity	8	2	12	2	6	

Source: the author

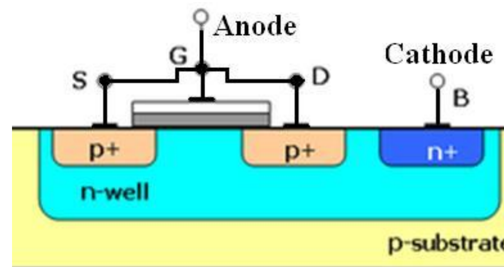
4.4 V_{REF_2}: Bandgap-based reference using PMOS diode

An alternative version of the bandgap-based reference, called V_{REF_2}, was implemented by using PMOS acting as diodes (PMOS_diode) instead of the vertical PNP transistors (*i.e.* D_1 and D_2) used in the last section. The same aspect ratio between D_1 and D_2 (*i.e.* 8) were kept. Figure 4.6 shows the cross-section of a PMOS transistor working as a diode. Drain, gate and source terminals are shorted, and act as the anode terminal, while the nwell bulk acts as

cathode terminal. Referring back to the figure 4.3, the cathode terminals are connected to the ground, while the anode terminals are connected to the op-amp input and resistor R_2.

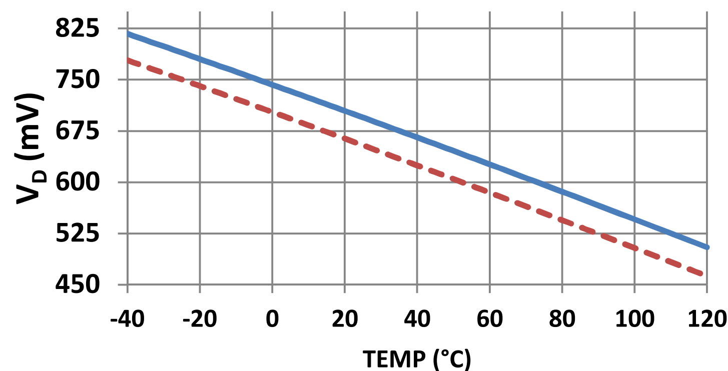
Figure 4.7 shows the diode voltage (V_D) for the vertical PNP transistor and the PMOS diode when biased with 1 µA. The emitter area of the PNP transistor has 80 µm^2, while the PMOS diode has a total area of 15 µm^2. The temperature coefficient (TC) of PNP transistor and PMOS diode are 1.97 mV/°C and 1.95 mV/°C, respectively. Since both devices has similar temperature performance, similar temperature compensation can be achieved by V_{REF_1} and V_{REF_2}.

Figure 4.6 - PMOS acting as a diode



Source: the author

Figure 4.7- Diode voltage vs temp for vertical PNP (line) and PMOS_diode (dotted)



Source: the author

The objective of replacing the PNP vertical transistor by a PMOS_diode were two. The first one was a tentative of improving the robustness of the bandgap reference against the impact of TID. As discussed in (GROMOV, 2007), the radiation-susceptibility of bandgap references implemented using advanced CMOS process is possibly dominated by the diodes. These diodes are usually implemented by means of vertical or lateral BJT devices in

commercial CMOS processes, and as discussed in section 2.8, these devices are really degraded by TID effects.

This hypothesis is based on the fact that CMOS transistors with very small oxide thickness has improved robustness against TID when compared to diodes. The reason for that is the low number of oxide traps (due to the small volume of the gate) and the compensation caused by electrons tunneling from silicon, as it was discussed in chapter 2. The diodes may be the most sensitive devices in bandgap references because their proximity to the STI structures (GROMOV, 2007). Therefore, it was decided to replace the diodes by the MOSFETs in order to verify if improved robustness against TID is achieved.

Moreover, the second reason for trying PMOS_diodes was to evaluate an alternative option for PNP transistors when implementing bandgap references - even when TID effects is not an issue. The most CMOS processes have PNP transistor or PN diodes characterized and well modeled, thus allowing its use in the design of voltage references. However, some digital processes may not have a parametric layout cell (possibility to define the emitter area) of the PNP transistor. For instance, it may be available only few options of layout for the PNP transistor. In this case, PMOS_diode could be used as a backup option (COLOMBO, 2012). Furthermore, using the PMOS_diode, it is possible to draw a very small area diode if a PMOS with minimal dimensions is chosen. Consequently, silicon results of a bandgap reference using PMOS_diodes would provide an estimation of how much of discrepancy we could expect of these diodes compared to PNP transistor

Table 4.4 shows devices size of V_{REF_2}. The difference between V_{REF_1} and V_{REF_2} is the implementation of diodes D_1 and D_2.

Table 4.4: Devices size of V_{REF_2}

Device	$P_{1,2,3}$	D_1	D_2	$R_{1,3}$ (*k*)	R_2 (*k*)	R_4 (*k*)
Width (µm)	5	9.86	9.86	226.68	20	120
Length (µm)	3	1	1			
Multiplicity	2	1	8			

Source: the author

4.5 V_{REF}_3: Simple V_{TH0}-based Reference

The third implemented circuit in this work is shown in figure 4.8. The voltage reference circuit is simply composed by a current source (I_{REF_1}), resistor R_2 and a diode-connected NMOS N_5.

Analyzing figure 4.8 it is possible to verify that I_{OUT} is given by (4.16), where S_{P3}/S_{P2} is the ratio of transistor sizes of P_2 and P_3. Note that I_{BIAS} is given by (4.9).

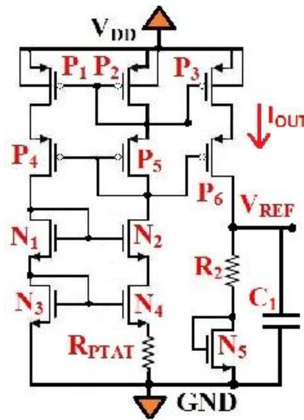
$$I_{OUT} = (S_{P3}/S_{P2}) \cdot I_{BIAS} \quad (4.16)$$

By means of (4.7), (4.9) and (4.14), the output voltage can be described by (4.17), where N is the ratio of S_{P3} and S_{P4}.

$$V_{REF} = V_{GSN5} + (S_{P3}/S_{P2}) \cdot (R_2/R_{PTAT}) \cdot \mathrm{n} \cdot \ln(N) \cdot U_T \quad (4.17)$$

Equation (4.17) is similar to (4.3), and K_{PTAT} here is mainly defined by the ratio of resistances and the ratio of transistors sizes.

Figure 4.8- Simple V_{TH0}-based voltage reference

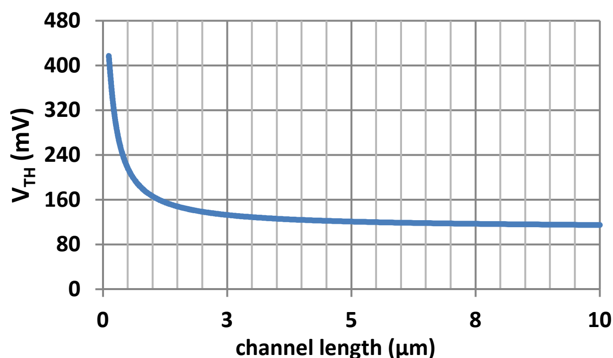


Source: the author

As previously mentioned, the V_{REF} generated by this circuit is equal to V_{TH0} and a few process-dependent parameters. Based on (4.14), the V_{GS} of transistor N_5 is employed to generate V_{REF} and thus, V_{REF} is directly proportional to the V_{TH} of N_5. It is well known that V_{TH} variability is inversely proportional to the transistor area (TSIVIDIS, 2010). Therefore, when designing the transistor channel length of N_5, the straightforward choice is to use large values of L (*e.g.* $L > 1$ µm).

However, for advanced CMOS technologies with very short-channels, V_{TH} is a function of L and thus, the output voltage of V_{TH}-based references also becomes a function of L. Figure 4.9 shows the simulation of V_{TH} as a function of L for a NMOSFET operating in saturation mode and W = 1 μm. This plot was obtained using the DC operation point analysis available in SPECTRE, in which the simulator extracts the threshold voltage for a given transistor dimension.

Figure 4.9 - V_{TH} as a function of L - reverse short channel effect



Source: the author

As shown in Fig. 4.9, V_{TH} varies by ~300 mV if L is swept from 0.13 to 10 μm. This increase in V_{TH} with decreasing L is called reverse short channel effect as described in (TSIVIDIS, 2010). In this design, a large value of channel length (*e.g.* L = 8 μm and consequently, V_{TH0} ~ 120 mV at 22 °C) was chosen in order to achieve V_{REF} nearly 300 mV.

Table 4.5 shows all devices size for V_{REF_3}, whose total layout area of V_{REF_3} is ~ 66 μm x 70 μm.

Table 4.5: Devices size of V_{REF_3}

Device	$P_{1,2,4,5}$	$P_{3,6}$	$N_{1,2}$	N_3	N_4	N_5	$R_{PTAT,1}$ (k)
Width (μm)	6	6.32	2.5	3	3	16	98.9
Length (μm)	5	5	5	8	8	8	
Multiplicity	2	5	2	2	10	1	

Source: the author

4.6 V_{REF_4}: Alternative V_{TH0} -based reference

The fourth designed circuit was proposed by (JIANPING, 2005) and it is shown in figure 4.10. Instead of directly adding two voltages with opposite TCs, V_{REF_4} circuit adds two currents with opposite temperature coefficient before converting it to voltage through the output resistor. Current I_{BIAS} is injected on N_6 and due to the feedback loop formed by devices P_4-P_5, N_5-N_6 and R_2, the gate source voltage of N_6 (V_{GSN6}) appears across R_2. As a consequence, I_{R2} described by (4.18), is generated across R_2.

$$I_{R2} = V_{GSN6}/R_2 \tag{4.18}$$

Current I_{R2} has negative TC since V_{GSN6} decreases with temperature. Both currents, I_{BIAS} and I_{R2}, are copied to the last circuit branch and added at the output node V_{REF}. Current I_{R3} is described by (4.19), where I_{BIAS} is given by (4.8).

$$I_{R3} = I_{P6} + I_{P7} = (S_6/S_5) \cdot I_{R2} + (S_7/S_2) \cdot I_{BIAS} \tag{4.19}$$

Therefore, the output voltage is given (4.19). Using (4.8), (4.15) and (4.16), equation (4.19) can be rewritten as (4.20).

$$V_{REF} = I_{R3} \cdot R_3 \tag{4.20}$$

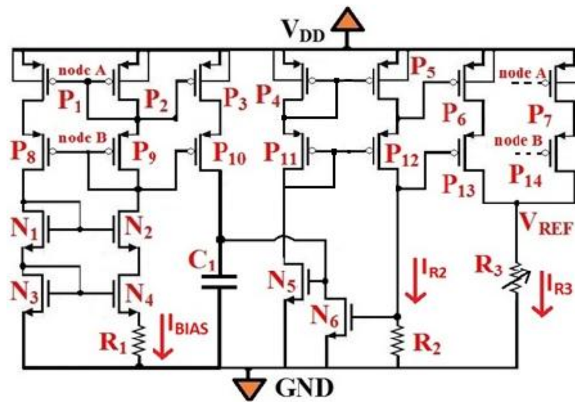
$$V_{REF} = R_3 \cdot \left[\left((S_6/S_5) \cdot V_{GSN6}\right)/R_2 + \left((S_7/S_2) \cdot n \cdot \ln(N) \cdot U_T\right)/R_1\right] \tag{4.21}$$

As can be seen in (4.20), the R_3 is chosen in order to define the value of V_{REF} without impact (to first order) on the temperature compensation. The temperature compensation is achieved by choosing properly the current gain or the transistor aspect ratio of P_2, P_5, P_6 and P_7.

In this voltage reference of Figure 4.10, it is the value of threshold voltage of N_6 plus some technological parameters that defines V_{REF}. For this design, large value of L (*e.g.* L = 6 µm) was chosen for N_6 in such a way to set the output voltage at nearly 300 mV.

Regarding the feedback loop composed by P_4-P_5, N_5-N_6, it is worth to add that capacitor C_1 sets the dominant pole at the gate of N_5. It also sets the gain-bandwidth product of the feedback loop (GIUSTOLISI, 2003). Therefore, C_1 should be properly sized in order to maintain the gain-bandwidth product well below the value of the other remaining poles, which are located at gate of P_4-P_5 and N_6 (GIUSTOLISI, 2003).

Figure 4.10 - V_{TH0}-based voltage reference (V_{REF_4})

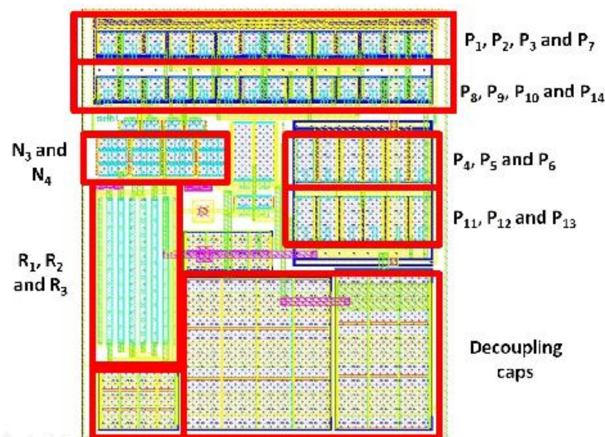


Source: the author

Resistor R_3 is composed by a fixed resistor plus five small resistors, that can be connected or disconnected, setting the effective R_3 by means of 5 bits of trimming. The trimming has binary weight and the least significant bit adds 800 to the value of R_3, and ΔV_{REF} of ~ 2.2 mV is added on V_{REF}. The second significant bit adds 1600 and so on.

Figure 4.11 shows the layout of V_{REF_4} whose silicon area is 105 µm x 125 µm. The main devices are shown in this figure. The current mirror, cascode devices and resistors are placed in a common centroid configuration. As for instance, N_4 is placed (multiplicity 10) surrounding N_3 (multiplicity 2). Table 4.5 shows the dimensions of all devices of V_{REF_4}.

Figure 4.11- Layout of V_{REF_4}



Source: the author

In order to help the understanding about the impact of TID on the performance of the voltage references, two additional pins (V_{PTAT_4}) and (V_{CTAT_4}) were included in this design.

Table 4.6: Devices size of V_{REF_4}

	$P_{1\text{-}3,8\text{-}10}$	$N_{1,2}$	N_3	N_4	N_5	N_6	$P_{4\text{-}6,11\text{-}13}$	P_7	P_8	$R_{1,2,3}$ (k)	C_1 (pF)
W (µm)	6	2.5	3	3	7	33	12.5	5.81	6	98.9	18
L (µm)	5	5	8	8	5	6	5	5	5		
m	2	2	2	10	1	1	2	8	8		

Source: the author

Pin V_{PTAT_4} is placed in the source terminal of N_4 and it makes possible the measurement of the PTAT voltage ($\Delta V_{GS} = V_{GSN3} - V_{GSN4}$). This measurement gives a relevant information since this voltage is used in the I_{BIAS} and V_{REF} generation for all V_{TH0}-based references.

Pin V_{CTAT_4} is placed in the gate terminal of N_6 and it makes possible the measurement of the CTAT voltage (V_{GSN6}). This measurement gives a relevant information because it gives an estimation of the TID impact on the threshold voltage of a NMOS transistor.

4.7 V_{REF_5}: V_{TH0}-based reference using composite transistors

The fifth designed voltage reference was proposed by (UENO, 2009) and it is shown in figure 4.12. This circuit uses I_{BIAS} (section 4.2) in order to bias two self-cascode transistors and produce the output voltage described by (4.22), where V_{DSN8} and V_{DSN6} are the drain-source voltages of transistor N_6 and N_8.

$$V_{REF} = V_{GSN9} + V_{DSN8} + V_{DSN6} \tag{4. 22}$$

Note that transistors N_5-N_6 and N_7-N_8 are arranged in a self-cascode configuration, and then, V_{DSN8} and V_{DSN6} are given by equation (4.7).

The current through P_3, P_4 and P_5 are respectively: $(S_{P3}/S_{P2})\cdot I_{BIAS}$, $(S_{P4}/S_{P2})\cdot I_{BIAS}$ and $(S_{P5}/S_{P2})\cdot I_{BIAS}$. Using (4.23) and the size ratio of the transistors in the current mirror, equation (4.22) can be rewritten as (4.23), if the channel length modulation effect is neglected. Note that (4.23) is similar to (4.3).

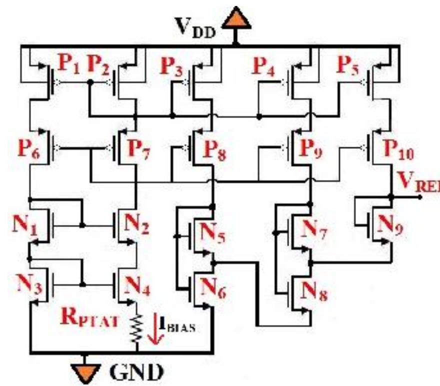
$$V_{REF} = V_{GSN9} + \mathrm{U_T} \cdot \mathrm{n} \cdot \ln\left\{\frac{[S_{N5} \cdot S_{N7} \cdot (S_{P3}+S_{P4}+S_{P5}) \cdot (S_{P4}+S_{P5})]}{(S_{N6} \cdot S_{N8} \cdot S_{P3} \cdot S_{P4})}\right\} \tag{4.23}$$

Through (4.23) it is possible to verify that the temperature compensation of V_{REF} can be performed with a proper sizing of devices P_3-P_5 and N_5-N_8. To estimate the required value of

the logarithmic term in (4.23), one can take its derivative with respect to temperature. Imposing (dV_{REF}/dT) = 0, one can find the required value through equation (4.24):

$$TC_{VGS}/TC_{UT} = n \cdot \ln(a) \qquad (4.24)$$

Figure 4.12 - V_{TH0}-based voltage reference (V_{REF_5})

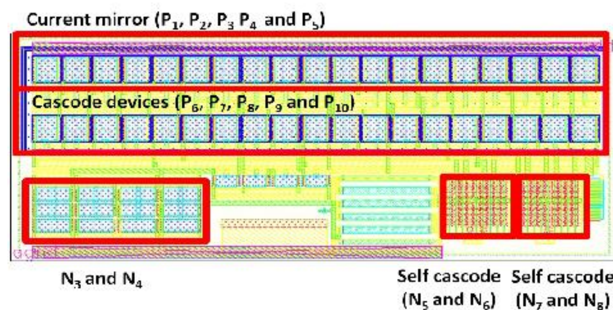


Source: the author, based on (UENO, 2009)

where “a” is the term inside brackets of (4.22), TC_{VGS} and TC_{UT} are the temperature coefficient for V_{GS} and U_T. Based on (4.22), the V_{GS} of transistor N_9 is employed to generate V_{REF} and thus, V_{REF} is directly proportional to the V_{TH} of N_9. In this design, we have chosen the minimal L (*i. e.* 130 nm) to achieve the largest possible value of V_{TH0} and V_{REF}. Note that choosing a large value of L (*e.g.* L > 3 µm) would decrease the variability of transistor N_9, and so the absolute variability of V_{REF}. However, this choice would also decrease the value of the V_{REF}, what would lead to a higher relative variability ($/V_{REF}$), where is the standard deviation.

The layout area is 140 µm x 55 µm and it is shown in figure 4.13. The current mirror, cascode devices and self-cascode transistors where designed in common centroid configuration. Table 4.7 presents all dimensions of V_{REF_5}.

Figure 4.13 - Layout of V_{REF_5}



Source: the author

Table 4.7: Devices size of V_{REF_5}

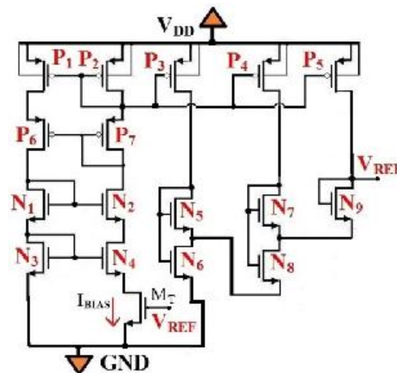
	$P_{1\text{-}3,6\text{-}8}$	$N_{1,2}$	N_3	N_4	N_5	$N_{6,8}$	N_7	$P_{4,9}$	$P_{5,10}$	N_9	R_{ptat} (k)
W (μm)	6	2.5	3	3	1	1	1	6	6	68.7	98.9
L (μm)	5	5	8	8	0.13	0.13	0.13	5	5	0.13	
m	2	2	2	10	73	1	72	5	8	1	

Source: the author

4.8 V_{REF_6}: Resistorless V_{TH0}-based reference using composite transistors

Voltage reference (V_{REF}_6), shown in figure 4.14, is the same circuit than (V_{REF}_5) but using no resistors in order to save silicon area. The poly resistor (R_{PTAT}) was replaced by a transistor operating in deep linear mode (M_T) whose gate is connected at the output node. As V_{REF}_6 is proportional to the V_{TH}, connecting the gate of M_T to V_{REF_6} tends to reduce the impact of fabrication process. For instance, if one consider that V_{TH} of M_T increases due to the global variations, V_{REF}_6 also tends to increase and thus, the overdrive voltage (V_{GS}-V_{TH}) of M_T tends to be constant. Perfect process compensation is not possible because the threshold voltages of M_7 and M_T are nominally different.

Figure 4.14 - V_{TH0}-based voltage reference (V_{REF_6})



Source: the author, based on (UENO, 2009)

It is important to mention that the temperature performance of V_{REF_6} depends on the TC of ON-resistance of M_T. In turn, TC of ON-resistance depends on mobility and threshold

voltage variations in the temperature range. Therefore, it is expected that TC of V_{REF_5} and V_{REF_6} be slightly different.

The layout area of V_{REF_6} is 71 µm x 104 µm and table 4.8 shows all dimensions of this circuit.

Table 4.8: Devices size of V_{REF_6}

	$P_{1\text{-}3,6\text{-}8}$	$N_{1,2}$	N_3	N_4	N_5	$N_{6,8}$	N_7	P_4	P_5	N_9	M_T
W (µm)	6	2.5	3	3	1	1	1	6	6	16.3	0.72
L (µm)	5	5	8	8	0.13	0.13	0.13	5	5	0.13	20
m	2	2	2	10	71	1	69	15	20	1	1

Source: the author

4.9 V_{REF}_7 and V_{REF}_8: Bandgap reference using 2.5-V transistors

All voltage references presented so far were implemented using core transistor (1.2 V of supply) of the 130 nm CMOS Process. As the impact of TID depends on the oxide thickness, a new topology voltage reference using 2.5 V devices were also implemented (COLOMBO, 2012). The designed circuit can be implemented without resistors if a resistor-less bias current is available.

The proposed circuit is shown in figure 4.15 and generates V_{REF} similarly to the traditional BGR approach: a diode voltage summed to a properly scaled PTAT voltage. The diode voltage is implemented by means of PMOS_diode (section 4.4), M_{14}, while the thermal voltage (U_T) is implemented by means of self-cascode transistors (section 4.1). The output voltage is called V_{REF_7}. A second version of this topology using PNP bipolar instead of M_{14} (W/L= 6 µm / 2 µm) was also implemented and its output voltage is called V_{REF_8}.

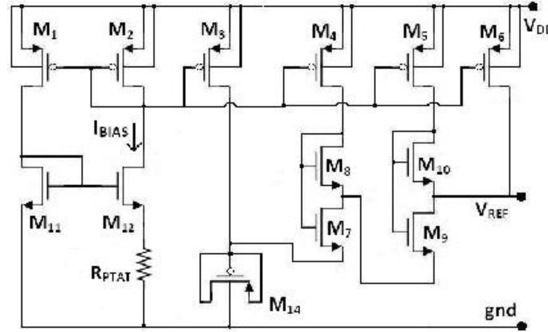
Transistors M_1, M_2, M_{11} and M_{12} are responsible to generate the bias current (I_{BIAS}) for the BGR. Considering that $S_{M1} = S_{M2} = S_{M3}$, the bias current is given by:

$$I_{BIAS} = (V_{GS11} - V_{GS12})/R_{PTAT} \tag{4.25}$$

For our circuit, we have chosen I_{BIAS} equal to ~ 357nA what requires R_{PTAT} to be around 100 K . This resistor can be replaced by a MOS transistor working in strong in version, deep triode operation if needed (UENO, 2009). Furthermore, the designed current source can be replaced by other current source without resistors, for instance, (ORGUEY, 1997) or

(KUSSENER, 2010). In these other possible configurations, the proposed circuit will not use resistors to generate V_{REF}.

Figure 4.15 - Bandgap (V_{G0}) - based voltage reference (V_{REF_7})



Source: the author

The output voltage generated by the proposed circuit is given by:

$$V_{REF} = V_{D14} + V_{DS7} + V_{DS9} \tag{4.26}$$

The current through M_4, M_5 and M_6 are respectively: $(S_4/S_2) \cdot I_{BIAS}$, $(S_5/S_2) \cdot I_{BIAS}$ and $(S_6/S_2) \cdot I_{BIAS}$. Using (4.7) and the size ratio of the transistors in the current mirror, equation (4.26) can be rewritten as (4.27), if the body effect is neglected.

$$V_{REF} = V_{D14} + U_T \cdot n \cdot \ln\left\{\frac{[S_8 \cdot S_{10} \cdot (S_4+S_5+S_6) \cdot (S_5+S_6)]}{(S_4 \cdot S_5 \cdot S_7 \cdot S_9)}\right\} \tag{4.27}$$

Through (4.27) it is possible to verify that the temperature compensation of V_{REF} can be performed with a proper sizing of devices M_4-M_{10}. To estimate the required value of the logarithmic term in (4.27), one can take its derivative with respect to temperature. Imposing $(dV_{REF}/dt) = 0$, one can find the required value through equation (4.28):

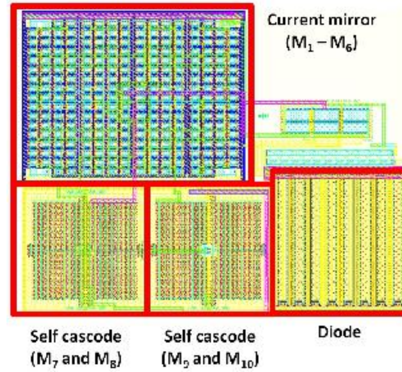
$$TC_{VD}/(TC_{UT} \cdot n) = \ln\left\{\frac{[S_8 \cdot S_{10} \cdot (S_4+S_5+S_6) \cdot (S_5+S_6)]}{(S_4 \cdot S_5 \cdot S_7 \cdot S_9)}\right\} \tag{4.28}$$

where TC_{VD} and TC_{UT} are the temperature coefficient for the diode voltage and U_T, whose simulated values are nearly -1.69 and 0.087 mV/°C, respectively. The substrate factor is roughly around 1.1 for the used technology (Binkley, 2008). The found value for the logarithmic term is nearly 15.

The size of all transistors in the proposed circuit is presented in table 4.9. The only different between V_{REF_7} and V_{REF_8} is the multiplicity of devices M_8 and M_{10} (self cascode devices), and the diode implementation. The layout is shown in Figure 4.16 and the occupied

area is ~ 100 μm x 100 μm. Common centroid layout configuration was used for the self-cascode devices and also for the current mirror.

Figure 4.16 - Layout of V_{REF_8}



Source: the author

In order to compare the impact of TID on the electrical behavior of the two implemented diodes (PMOS diode and PNP), output pins were added in the design. For V_{REF_7}, the gate of M_{14} (diode voltage) can be measured through V_{CTAT_7} pin. For V_{REF_8}, the emitter terminal of the PNP device (diode voltage) can be measured through V_{CTAT_8} pin. Comparing these two voltages, it is possible to verify if the use of diode implemented by means of PMOS transistors improved the robustness against TID effects.

Table 4.9: Devices size of V_{REF_7} and V_{REF_8}

Device	M_1	M_2	M_3	M_4	M_5	M_6	M_7
Width (μm)	1.25	1.25	1.25	1.25	1.25	1.25	1
Length (μm)	2	2	2	2	2	2	0.25
Multiplicity	4	4	4	2	100	150	4
Device	**M_8 (V_{REF_7})**	**M_8 (V_{REF_8})**	**M_9**	**M_{10} (V_{REF_7})**	**M_{10} (V_{REF_8})**	**M_{11}**	**M_{12}**
Width (μm)	1	1	1	1	1	3	3
Length (μm)	0.25	0.25	0.25	0.25	0.25	8	8
Multiplicity	262	291	1	155	291	2	4

Source: the author

4.10 V_{REF_9}: Low dropout (LDO) regulator

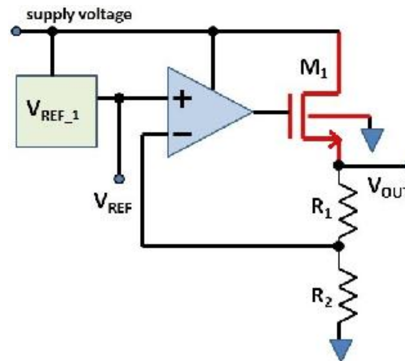
A DC linear regulator shown in figure 4.17 was designed using V_{REF_1}. The op-amp circuit is the same described in section 4.3.1 and the power device was implemented with a zero V_{TH} transistor in order to achieve output voltages around 1 V even with a supply voltage of 1.2 V. The output voltage is given by (4.29)

$$V_{OUT} = \left(\frac{R_1}{R_2} + 1\right) \cdot V_{REF} \tag{4.29}$$

R_1 and R_2 are equal to 33.33 k and 100 k , and V_{OUT} is around 1.34*V_{REF_1}. The size of M_1 is (W = 20 µm*50/ L = 0.7 µm) and the provided output current is 1 mA.

The objective of this case-study is the investigation of the impact of TID on the offset of the operation amplifier (the same op-amp used in the design of V_{REF1}). The first output pin of this circuit is V_{REF1} (positive input of operational amplifier) while the second output pin is V_{OUT} (regulator output voltage). By means of these two voltages (V_{REF3} and V_{OUT}); and by the mismatch of the ratio R_1/R_2 (obtained in the technology manual), it is possible to have a rough estimation of the offset voltage (V_{OS}) and verify the impact of radiation on it.

Figure 4.17- Voltage regulator using V_{REF_1}



Source: the author

4.11 Post extraction simulation results

This section presents the simulation results for all designed circuit. BSIMv4 transistor models and Spectre simulator were used. Circuits were simulated in a temperature range of -40 to 125ºC, and the output voltage variation was measured as V_{REF_TEMP}. Lately, the

temperature coefficient (TC, given in ppm/°C) is calculated by equation (4.30), which is the definition used in this work:

$$TC = V_{REF}(T_0)^{-1} \cdot (\Delta V_{REF_TEMP}/\Delta T) \quad (4.30)$$

The output voltage variations caused by V_{DD} fluctuation (V_{REF_VDD}) was simulated considering a variation of 1.0 to 1.2 V in V_{DD} for 1.2 V references and from 2.3 to 2.5 V for the 2.5 V references. Moreover, the output noise (V_{REF_NOISE}) and the power supply rejection (PSR) were also simulated.

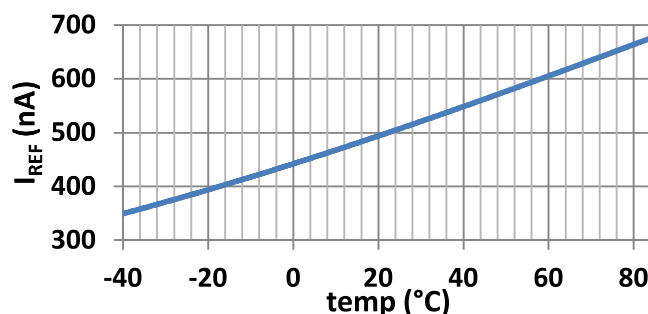
Table 4.10 shows all performance parameters simulated at typical process conditions (TT). A second version of V_{REF_1}, called, V_{REF_1A} was designed only be used as comparison, and it was neither laid out nor fabricated. V_{REF_1A} has the same dimensions than V_{REF_1A} with only a lower ratio of R_4/R_3 in order to decrease the output voltage.

Circuits V_{REF_1} and V_{REF_5} were designed to have practically the same output voltage ~ 680 mV. Circuits V_{REF_1A}, V_{REF_3} and V_{REF_4} were designed to have practically the same V_{REF} ~ 300 mV.

The temperature performance of I_{REF} (nA) is shown in figure 4.18, and it is about 2.5 nA/°C. The temperature behavior of I_{REF} is important because it affects directly the TC of V_{REF_3}, V_{REF_4}, V_{REF_5}, V_{REF_7} and V_{REF_8}.

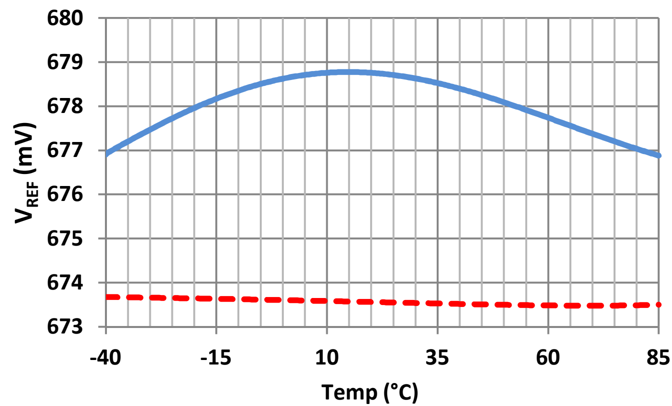
The simulated V_{REF_TEMP} for circuits V_{REF_1} (V_{G0}-based) and V_{REF_5} (V_{TH}-based) are 1.9 mV and 200 µV, respectively as shown in figure 4.19. The bandgap reference achieves better temperature performance because its PTAT and CTAT voltages are more linear than the PTAT and CTAT voltage generated by the V_{TH0}-based circuit. For instance, the linearity of PTAT voltage generated by self cascode transistors is hampered by body effect. Figure 4.20 shows the temperature behavior of V_{REF_6}.

Figure 4.18 - I_{REF} vs. temperature



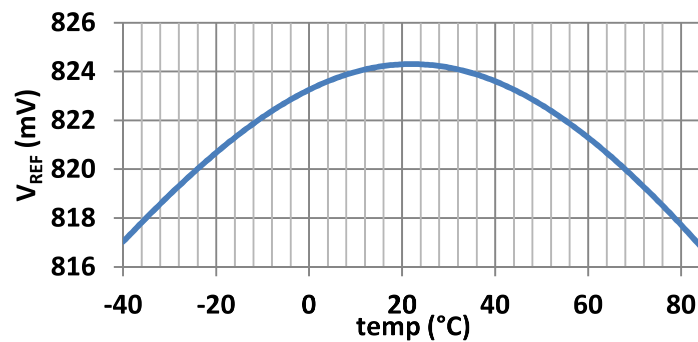
Source: the author

Figure 4.19 - V_{REF} Vs Temp: V_{REF_1} (dotted) and V_{REF_5} (line)



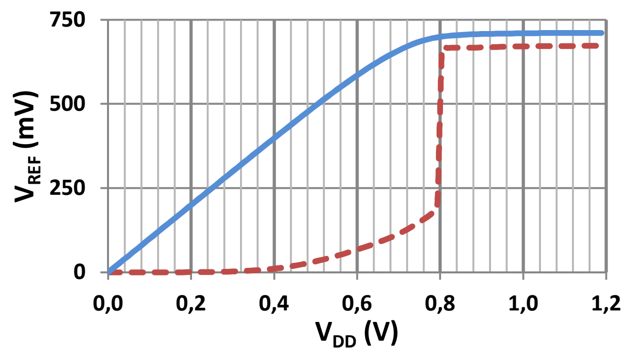
source: the author

Figure 4.20 - V_{REF_6} vs. temperature



Source: the author

Figure 4.21 - V_{REF} Vs VDD: V_{REF_1} (dotted) and V_{REF_5} (line)



Source: the author

Figure 4.21 shows the supply voltage dependency of V_{REF_1} and V_{REF_5} using SS models.. It is possible to see that both circuits are turned on when the V_{DD} is greater than 800 mV. The integrated output noise in a 1 MHz bandwidth (V_{REF_NOISE}) was found to be 191µV and 741

μV for circuit V_{REF_5} and V_{REF_1}, respectively. The BGR architecture implemented in this work is found to be a bit noisier because of the noise amplification from the differential pair is determined by its closed-loop gain.

Table 4.10: Simulated Performance parameters using TT models

Circuit	V_{REF} **(mV) @ 22.5 °C**	V_{REF_TEMP} **(mV)**	***T (ºC)***	V_{REF_VDD} **(mV)**
V_{REF_1}	673.7	0.2	125	1.5
V_{REF_1A}	316.3	0.4	125	2.2
V_{REF_2}	697.1	0.2	125	1.4
V_{REF_3}	316.3	6.8	125	0.65
V_{REF_4}	307.3	6.3	125	0.86
V_{REF_5}	678.7	1.9	125	0.41
V_{REF_6}	824.3	7.6	125	5.5
V_{REF_7}	1473	3.61	125	8.8
V_{REF_8}	1434	3.84	125	8.4
V_{REF_9}	897.5	0.2	125	2.0
Circuit	V_{REF_NOISE} **(μV)**	***PSR*@DC (dB)**	I_{SUPPLY} **(μA)**	***area* (μm²)**
V_{REF_1}	741	-40	20	25430
$V_{REF_1_A}$	382	-43	15	32000
V_{REF_2}	771	-40	20	22730
V_{REF_3}	172	-50	2.3	4690
V_{REF_4}	232	-47	6.8	13230
V_{REF_5}	191	-59	4.8	7700
V_{REF_6}	214	-32	11.8	7500
V_{REF_7}	387	-27	24.3	10000
V_{REF_8}	358	-27	24.3	10820
V_{REF_9}	443	-37	30	46560
I_{REF} **(nA)**	I_{REF_TEMP} **(nA)**	I_{REF_VDD} **(nA)**	***T (ºC)***	***area* (μm²)**
500.5	328.7	3	125	7000

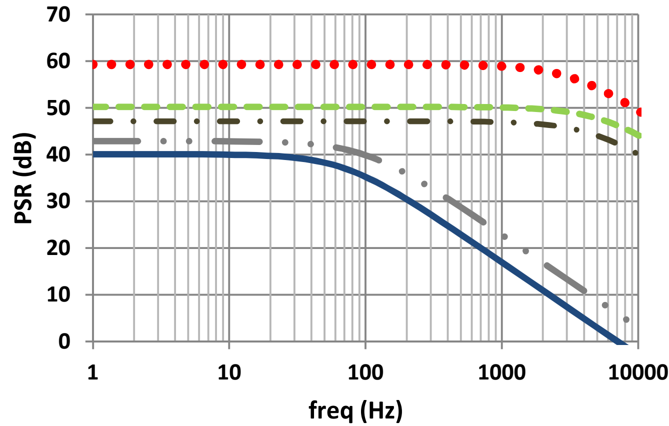
Source: the author

Furthermore, PSR at DC for V_{REF_5} and V_{REF_1} are -59 dB and -40 dB, respectively, as can be seen in figure 4.22. For V_{REF_5}, a -3dB reduction of the PSR happens at 3.6 kHz which represents a good performance compared to (UENO, 2009).

The output voltage as a function of supply for the circuits V_{REF_1A}, V_{REF_3} and V_{REF_4} can be seen in figure 4.23. The same behavior than the previous circuits (V_{REF_1} and V_{REF_5}) is expected and also observed. All three circuits started to operate at 800 mV of supply voltage.

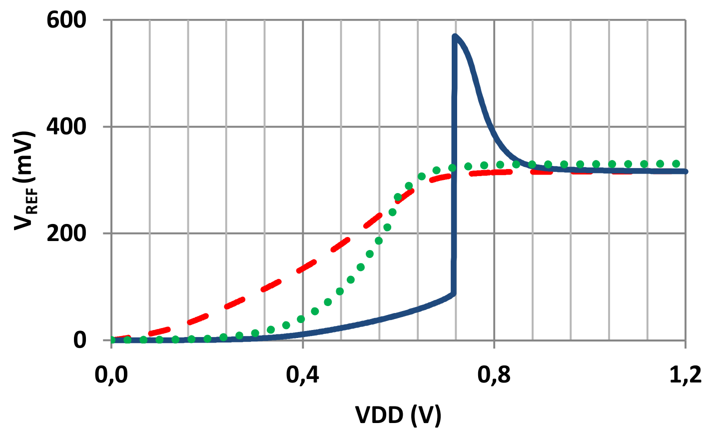
Circuits V_{REF_3}, V_{REF_4} and V_{REF_1A} present the line regulation performance of 3 mV/V, 4 mV/V and 11 mV/V, respectively.

Figure 4.22 - PSR: Highest to the lowest values: V_{REF_5}, V_{REF_3}, V_{REF_4}, V_{REF_1A} and V_{REF_1}



Source: the author

Figure 4.23 - V_{REF} vs. VDD: V_{REF_1A} (line), V_{REF_3} (broken line) and V_{REF_4} (dotted)

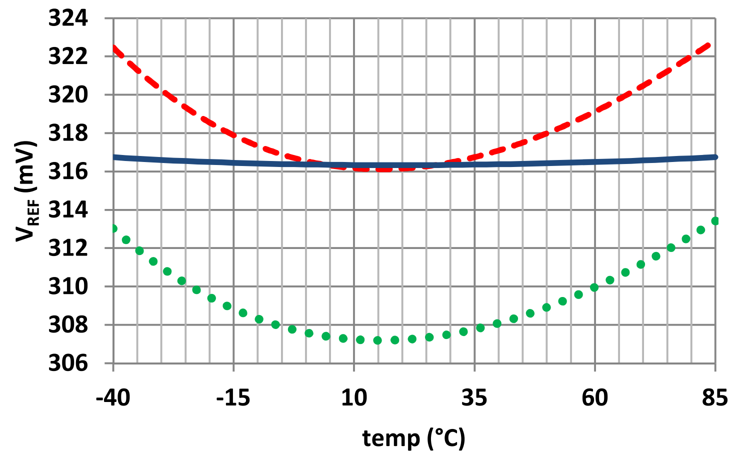


Source: the author

The output voltage as a function of temperature for the circuits V_{REF_1A}, V_{REF_3} and V_{REF_4} can be seen in figure 4.24. Due to the best linearity of V_{PTAT} and V_{CTAT}, V_{REF} of the bandgap circuit has lower curvature than compared to the V_{TH0}-based reference.

Regarding PSR at DC, circuits V_{REF_1A}, V_{REF_3} and V_{REF_4} have - 43, -50 and - 47 dB, respectively. As expected, the cascode transistors used in V_{REF_3} and V_{REF_4} circuits increased its PSR performance. Regarding the output noise, V_{REF_1A}, V_{REF_3} and V_{REF_4} have 382, 172 and 232 μV, respectively.

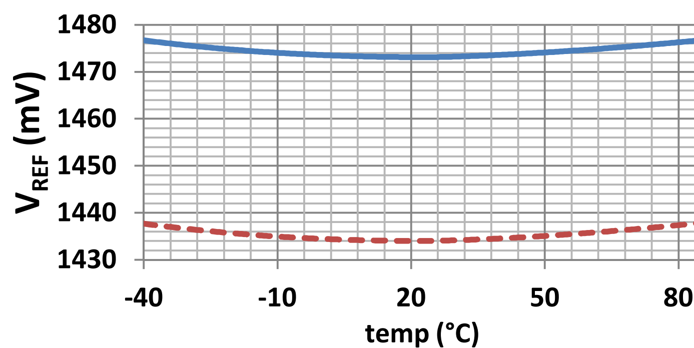
Figure 4.24 - V_{REF} vs. temp: V_{REF_1A} (line), V_{REF_3} (broken line) and V_{REF_4} (dotted)



Source: the author

Figure 4.25 shows V_{REF_7} (line) and V_{REF_8} (broken line) as a function of temperature for a supply voltage of 2.5 V. Both circuits presents TC calculated through equation 4.58 of about 22 ppm/ºC at TT process. V_{REF_7} and V_{REF_8} achieve only -27 dB at DC of power supply rejection. These values of line sensibility and PSR can be not acceptable for certain applications. Both values are mainly result of a poor VDD regulation performed by the current source circuit. Improved performance can be achieved if cascode devices are included in the current source and mirror.

Figure 4.25 - V_{REF} vs. tem: V_{REF_7} (line) and V_{REF_8} (broken line)



Source: the author

4.11.1 Impact of fabrication process effects

To estimate the impact of fabrication process in the designed circuits, simulation using process corners were performed and the results are shown in table 4.11. Transistor corner

models typical (T), fast (F) and slow (S); and corner models for resistor and BJT (max and min) were also employed. These models corresponds to the 3 sigma ( ) of variation of the devices parameters (*e.g.* μ_0, V_{TH}, resistance). In table 4.11, +res and -res mean plus and less 3 , respectively. BJT and resistor model varies together in the same direction.

Table 4.11: Simulated V_{REF} and I_{REF} using corner models

circuits	***models***								
		SS		**FF**		**SF**		***FS***	
	TT	**+res**	**- res**	**+res**	**- res**	**+ res**	**- res**	**+ res**	**- res**
	V_{REF} (mV) or I_{REF} (nA)								
V_{REF_1}	673.6	663.3	688.4	664.4	689.2	663.5	688.5	664	689
V_{REF_1A}	316.3	312.9	321	314	322	313.8	321.8	313	321.1
V_{REF_2}	697.1	692.7	701.5	693.9	702.3	692.9	701.7	693.5	702
V_{REF_3}	316.3	331.2	357.3	280.5	305.2	328.5	354.4	285.7	310.6
V_{REF_4}	307.3	321.5	347.2	273	297	319.1	344.6	277.7	301.9
V_{REF_5}	678.7	698.5	726.6	636.1	661	688.3	716.2	649.9	675
V_{REF_6}	824.3	847.7	847.6	797.4	797.3	838.8	838.8	809.6	809.5
V_{REF_7}	1473	1457	1561	1415	1502	1448	1548	1423	1513
V_{REF_8}	1434	1408	1540	1370	1480	1399	1527	1374	1491
V_{REF_9}	897.5	883.7	917.1	885.3	918.2	883.9	917.3	884.8	918
I_{REF}	500.5	411.4	658.1	403	641.8	410.1	655.7	404.4	644.5
	V_{REF_TEMP} (mV) or I_{REF_TEMP} (nA)								
V_{REF_1}	0.2	3.2	5	3.3	4.8	3.5	4.9	3.1	5
V_{REF_1A}	0.4	1.6	3.3	2.2	2.7	2.1	2.8	1.7	3.2
V_{REF_2}	0.2	0.9	1.6	1.2	1.2	1.3	1.3	0.8	1.5
V_{REF_3}	6.8	8.4	14.1	10	11.3	8.4	14	10	11.4
V_{REF_4}	6.3	7.9	12.6	9	10.8	7.6	12.9	9.2	10.5
V_{REF_5}	1.9	9.4	9.3	2.7	15.8	10	8.5	2.7	15.8
V_{REF_6}	7.6	13.6	13.6	16	15.9	13.1	13.1	14.4	14.5
V_{REF_7}	3.6	3.4	53.1	32	8.8	7.8	42.5	26	16.2
V_{REF_8}	3.8	5.8	60.4	36	14.9	11.6	49.8	30	23.4
V_{REF_9}	0.2	3.9	6.9	4.2	6.5	4.4	6.7	3.9	6.8
I_{REF}	328.7	269.4	437.2	262.6	424.6	268.8	435.4	263	426.3

Source: the author

Table 4.12 shows the maximum and minimum values of V_{REF} and I_{REF} using corner models, the spread (maximum - minimum), named as "ΔV,I" and also the maximum temperature variation, named as "ΔV,I_{TEMP}". As can be seen in table 4.12, circuits V_{REF_1}, V_{REF_1A} and V_{REF_2} are weakly sensitive to the process variation because its V_{REF} are proportional to the bandgap voltage.

The threshold voltage references ($V_{REF_3,4,5,6,7}$) are strongly dependent on the corner process. A maximum variation of almost 76 mV and 90 mV is expected between the fast and slow corner for V_{REF_3} and V_{REF_5}, respectively. This type of topology can be used as a process sensor, that indicates the value of threshold voltage of transistors on the wafer. Regarding the temperature performance, V_{TH}-based references also seen to be more susceptible to the process or global variations.

Simulation using process corner models provides some directions about how the V_{REF} can be affected by the fabrication process. However, since mismatch between the electrical parameters are not taken into account, Monte Carlo analysis should be done to provide better estimation of V_{REF} and ΔV_{REF_TEMP} after fabrication.

Monte Carlo analysis was performed in 1,000 samples by including process and mismatch variations. Table 4.13 shows the Monte Carlo results for the designed circuits. It is shows the standard deviation of V_{REF} and I_{REF} ( ), the maximum and minimum values of V_{REF} and I_{REF}; and the total spread (maximum - minimum), names as "ΔV" and "ΔI". Moreover, the dispersion factor (/mean) is also presented in this table. Finally, the last row of table 4.15 shows the total variation of V_{REF} and I_{REF} in percentage (±%). Figure 4.26 shows the histogram of V_{REF_1} at 22 °C.

The mean value and standard deviation ( ) of V_{REF} @ 22 °C for circuit V_{REF_5} (V_{TH}-based reference) are 681.8 mV and 27.8 mV, respectively. For the circuit V_{REF_1} (V_{G0}-reference) the mean value and are 674 mV and 16.1 mV, respectively. This would mean that the V_{TH}-based reference generates a V_{REF} with a variability ( ) 11.7 mV (72%) higher than that generated by BGR.

For a 3-sigma requirement (99.73% of samples), V_{REF_5} have an additional dispersion of 88 mV in the V_{REF} than compared to V_{REF_1}. Note that the ΔV of V_{REF_1} and V_{REF_5} are equal to 95.6 mV and 184.3 mV, respectively.

Table 4.12: V_{REF_MAX} and V_{REF_MIN} using corner models

	$V_{REF\ 1}$	$V_{REF\ 1A}$	$V_{REF\ 2}$	$V_{REF\ 3}$	$V_{REF\ 4}$	$V_{REF\ 5}$	$V_{REF\ 6}$	$V_{REF\ 7}$	$V_{REF\ 8}$	$V_{REF\ 9}$	I_{REF}
V,I$_{MAX}$ **(mV),(nA)**	689.2	322	702.3	357.3	347.2	726.6	847.7	1561	1540	918.2	658
V,I$_{MIN}$ **(mV),(nA)**	663.3	312.9	692.7	280.5	273	636.1	797.3	1415	1370	883.7	403
V,I (mV),(nA)	25.9	9.1	9.6	76.8	74.2	90.5	50.4	146	170	34.5	255
V,I$_{TEMP}$ **(mV),(nA)**	5	3.3	1.6	14.1	12.9	15.8	16	53.1	60.4	6.9	437

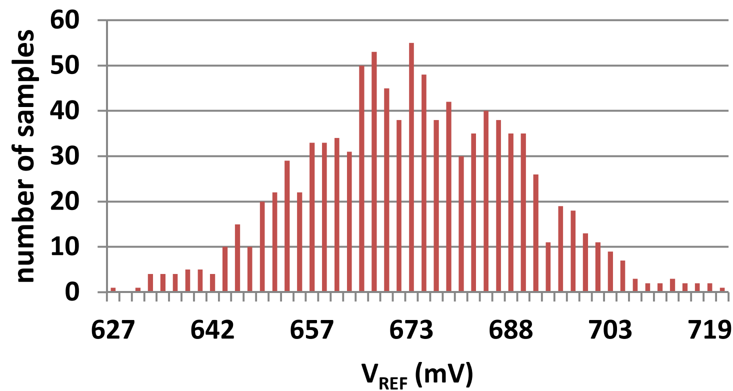
Source: the author

Table 4.13: Monte Carlo analysis of V_{REF} and I_{REF} @ 22.5 °C

	$V_{REF\ 1}$	$V_{REF\ 1A}$	$V_{REF\ 2}$	$V_{REF\ 3}$	$V_{REF\ 4}$	$V_{REF\ 5}$	$V_{REF\ 6}$	$V_{REF\ 7}$	$V_{REF\ 8}$	$V_{REF\ 9}$	I_{REF}
mean	674	316.3	697.3	316.6	313.7	681.8	827.3	1477	1438	898.5	504.5
(mV),(nA)	16.1	10	16.1	15.7	15.9	27.8	28.9	25.3	25.8	21.7	53.3
V,I$_{MAX}$ **(mV),(nA)**	722.5	353.4	745.6	369.2	365.3	784.7	929.7	1572	1540	963.6	714.5
V,I$_{MIN}$ **(mV),(nA)**	626.9	284.7	641.6	268.6	270	600.4	748.3	1394	1354	832	376.1
V, I (mV),(nA)	95.6	68.7	104	100.6	95.3	184.3	181.4	178	186	131.6	338.4
/mean (10^{-3})	23.9	31.6	23.1	49.6	50.7	40.8	34.9	17.1	17.9	24.2	105.6
V, I (±%)	7.1	10.9	7.5	15.9	15.2	13.5	11	6	6.5	7.3	33.5

Source: the author

Figure 4.26 - Histogram of V_{REF_1} at 22 °C



Source: the author

The ratio (sigma/V_{REF}) can be used as a comparison parameter and it is $40.7*10^{-3}$ and $23.8*10^{-3}$ for V_{REF_5} and V_{REF_1}, respectively. This higher dispersion is mainly due to the fact that V_{TH} is a parameter that is hard to control in state of the art technologies, showing large variability.

For applications involving high accuracy, trimming circuits can be added in both circuits in order to mitigate the impact of fabrication process. However, the number of bits required by V_{TH}-based references will be much greater than that required by V_{G0}-based references. A larger number of bits probably results in larger number of pins and larger area, which results in higher fabrication costs.

Comparing the mean of V_{REF} for V_{REF_1A}, V_{REF_3} and V_{REF_4}, again, it is possible to verify that V_{TH}-based references are more sensitive to process variability. References V_{REF_3} and V_{REF_4} have sigma of V_{REF} about 15.7 and 15.9 mV, while reference V_{REF_1A} has 10 mV. The ratio sigma/V_{REF} is equal to $31*10^{-3}$, $49*10^{-3}$ and $50*10^{-3}$ for V_{REF_1A}, V_{REF_3} and V_{REF_4}, respectively.

Table 4.14 shows the Monte Carlo analysis for ΔV_{REF_TEMP} and ΔI_{REF_TEMP}. It shows the mean, sigma and worst case of variation (ΔV_{TEMP_MAX}) obtained in a Monte Carlo analysis with 1,000 samples. For I_{REF}, it is presented the maximum and minimum values of ΔI_{REF_TEMP}.

Additionally, table 4.14 shows the mean value of TC (last row) calculated using equation (4.30), where T is 125 °C and V_{REF_TEMP} is given in the first row of this table. Note that as TC is inversely proportional to V_{REF}, circuits V_{REF_7} and V_{REF_8} whose output voltage is ~ 1400 mV, present the lowest value of TC.

Table 4.14: Monte Carlo analysis of V_{REF_TEMP} and I_{REF_TEMP}

	V_{REF_1}	V_{REF_1A}	V_{REF_2}	V_{REF_3}	V_{REF_4}	V_{REF_5}	V_{REF_6}	V_{REF_7}	V_{REF_8}	I_{REF}
Mean (mV),(nA)	10.7	7.2	10.8	8.3	7.6	4.7	9.7	10.0	10.0	328.4
(mV),(nA)	8	5.4	8.2	1.6	1.4	2.8	1.9	5.9	5.9	28.9
ΔV_{TEMP_MAX}, ΔI_{TEMP} (mV),(nA)	55	31	43	18.1	14.9	15.9	18.3	44.8	48.8	455.7 256.9
Mean TC (ppm/°C)	127	182	124	210	194	55	94	54	56	5208

Source: the author

Comparing the last line of table 4.12 (worst case of temperature performance) and table 4.14, one can see that the device mismatch (not taken into account in the corner simulations)

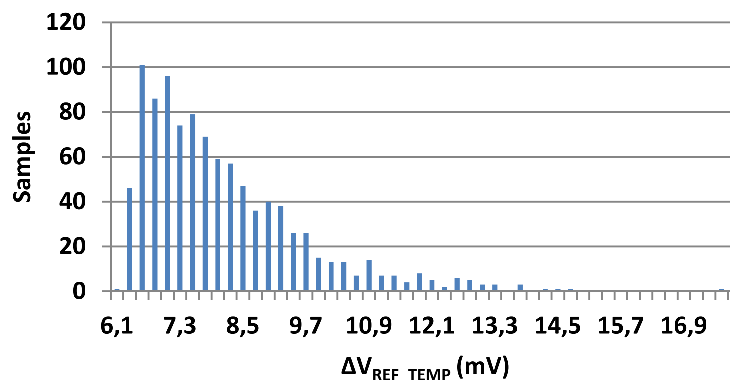
significantly degrades the temperature performance of the designed circuits. As for instance, V_{REF_1} has the worst case of temperature variation equal to 5 mV and 55 mV according to corner simulations and Monte Carlo analysis, respectively.

Verifying the mean value of V_{REF_TEMP} of the Bandgap references (V_{REF_1}, V_{REF_1A} and V_{REF_2}) given by table 4.14, it is possible to see that the nominal value of V_{REF_TEMP} presented in table 4.10 is only achieved with a perfect device matching and it is not realistic. As for instance, for V_{REF_1}, the nominal value of V_{REF_TEMP} is 0.2 mV while its mean value predicted by Monte Carlo analysis is around 10 mV. For the threshold voltage references (*e.g.* V_{REF_3}), the nominal (6.8 mV) and mean value (8.3 mV) of V_{REF_TEMP} are closer each other.

Through table 4.14, it is possible to compare the mean and sigma of V_{REF_TEMP} of bandgap-based references (V_{REF_1} and V_{REF_1A}) and threshold-based references (V_{REF_3} V_{REF_4} V_{REF_5} and V_{REF_6}). One can verify that the temperature performance of the designed threshold voltage references are less degraded by the process variability than the bandgap-based reference. This is an interesting observation; because at room temperature, the bandgap-based reference is less degraded due to the process variability than V_{TH0}-based references, as one can see in the last line of table 4.15 (V, I).

Finally, it is important to note that only very few samples have the temperature performance so degraded as V_{TEMP_MAX} in table 4.14. For instance, figure 4.27 shows the histogram of ΔV_{REF_TEMP} for V_{REF_3}. As can be seen, the most part of samples have ΔV_{REF_TEMP} lower than 13 mV (more than 99% of samples).

Figure 4.27 - Histogram of ΔV_{REF_TEMP} for V_{REF_3}



Source: the author

Therefore, for the design circuits, we can conclude that the nominal value of V_{REF} at room temperature of bandgap-based reference is less affected by process variability, while its temperature performance is worse affected when compared to the V_{TH0}-based references.

The higher variability of V_{REF} at room temperature for the threshold voltage references is expected due to the larger variability of V_{TH0} compared to the bandgap voltage. The temperature performance of bandgap references depends on the circuit topology its design decisions, and therefore, the worse performance observed in our circuits cannot be true for other bandgap topologies.

4.11.2 Impact of radiation effects (TID)

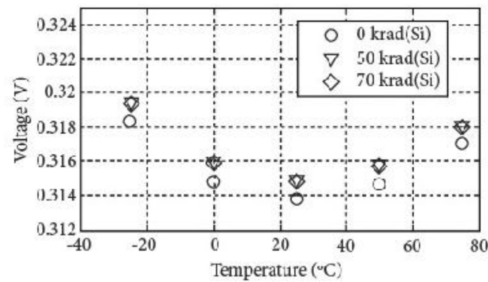
In this section we present a discussion regarding the impact of TID effects on the output voltage for the V_{TH}-based voltage references (V_{REF_3}, V_{REF_4}, V_{REF_5} and V_{REF_7}). The simulated results of the impact of TID was published in our work (BOTH, 2013) and it was carried out by Thiago Both and Ricardo Dallasen, students of our research group.

The impact of TID on the electrical behavior of transistors was modeled by a shift on the threshold voltage of transistors. The value of the shift on V_{TH} (ΔV_{TH_TID}) due to irradiation was extracted from (HAUGERUD, 2005). ΔV_{TH_TID} was considered to be about $\pm$ 1.5 mV for 70 krad of irradiation for transistors implemented on 130 nm CMOS process.

The effects of ΔV_{TH_TID} were verified in a temperature sweep simulation by means of a Monte Carlo analysis, where the threshold voltage of each transistor of the voltage reference circuits was randomly modified for each Monte Carlo run. The objective here, instead of providing precise prediction, was only to have a first and rough estimation of the impact of TID on V_{REF}. Moreover, this analysis is used as first case-study in the development of simulation methodology for TID effects.

The simulation shows that the output voltage of the irradiated circuit would suffer few milivolts (~ 2 mV) due to TID effects (70krad). Figure 4.30 shows the simulated V_{REF_4} before and after irradiation.

Figure 4.28 - Simulated V_{REF_4} before and after TID



Source: the author, from (BOTH, 2013)

4.12 Integrated circuit with the designed circuits

Figure 4.29 shows the layout of the entire integrated circuit containing the voltage references, current reference and CMOS Ring oscillator. Other students of our group were responsible for the design of a LNA, radiation sensor, stacked CMOS pairs and a linear voltage regulator. The total area including I/O pads is 2 mm x 2 mm. The integrated circuit was packaged in an open-cavity ceramic 64-pins Quad Flat Package (QFP).

Figure 4.29 - Layout of the integrated circuit designed in 130 nm CMOS

Source: the author

All outputs (V_{REF} and I_{REF}) were connected in ESD protection circuits basically composed by two PN diodes placed in a back to back configuration. This design decision was taken in order to protect our circuits since it would be handled many times by different engineers and different machines during the packaging process, soldering and measurements. Protection diodes have large area (*e.g.* emitter area of 100 μm^2) and may present significant leakage current that may degrade the measurement of the low power and low current circuits. In simulations, the leakage current of these diodes were less than 150 pA at 125ºC and therefore, it was decided to use it.

5 OSCILLATORS - CASE STUDY II

5.1 Basic concepts

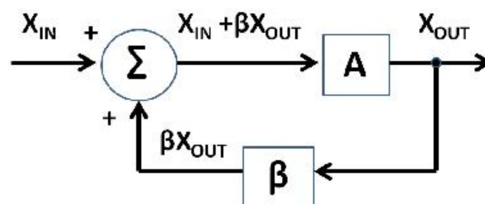
Oscillators are circuits that generate periodic output signals, usually in the form of voltage, through the conversion of DC power from the power supply to AC signal without the need for an AC input source.

Regarding the type of the output waveform, one can classify oscillators as: (i) linear or sinusoidal; and (ii) non-linear, like the relaxation oscillator. The output waveform of (i) is sinusoidal or close to it; and an example of this type of circuit is the LC-tank oscillator. The output waveform of (ii) is normally a sawtooth, triangle or square wave, as those produced by CMOS ring-oscillators.

Figure 5.1 shows a simple model for an oscillator composed by a linear amplifier with gain A and a frequency-selective feedback network, which both are connected in a loop configuration (RAZAVI, 2001). As can be seen, the positive feedback returns part of the output signal to the amplifier input. The signal returned by the feedback must have proper amplitude and phase in order to sustain the oscillation, as it is discussed bellow.

The feedback network is typically composed of passive components that determine the frequency of oscillation. Moreover, A and β are a function of frequency and it would be better written as A(s) and (s), where $s = j \cdot \omega$. For a CMOS ring-oscillator, the linear amplifier is replaced by active devices working as switches.

Figure 5.1: Linear model for an oscillator



Source: the author, based on (RAZAVI, 2001)

The external signal X_{IN} shown in figure 5.1 is only applied initially and it does not exist during the steady-state operation of the oscillator. Noise signals and the transient associated with the circuit turning on work as X_{IN} needed to initiate the oscillation.

If we assume that a input signal X_{IN} is initially present (*e.g.* during the power on of the supply voltage), one can write the transfer function for the oscillator of figure 5.1 by equation (5.1):

$$X_{OUT} = \frac{A(s)}{1 - A(s) \cdot \beta(s)} \cdot X_{IN} \tag{5.1}$$

If X_{IN} is subsequently removed, the only condition which X_{OUT} is nonzero is if $A(s) \cdot \beta(s) = 1$; which is known as Barkhausen criterion (RAZAVI, 2001). More precisely, in order to have oscillation at frequency w_0, the Barkhausen Criterion calls for two requirements for the loop gain:

(i) $|A(j \cdot \omega_0) \cdot \beta(j \cdot \omega_0)| = 1$: Magnitude (real part of loop gain) equal one,

(ii) $< |A(j \cdot \omega_0) \cdot \beta(sj \cdot \omega_0) = 0$: Phase angle (imaginary part of loop gain) must be zero or 360° in the frequency of oscillation.

If A is an inverting amplifier (non-inverting amplifier), the phase angle should be 180° (0° or 360°). In oscillator design, the loop gain is usually designed to be slightly larger than unity (*e.g.* twice or three times) at the desired frequency of oscillation.

If the gain is designed to be very high, the oscillation grows in amplitude with time until it be clipped by the amplifier and therefore, a constant-amplitude oscillation is resulted. If exact unity gain loop is designed, an eventual slight reduction in the gain caused by fabrication process effects would result in oscillations that decays to zero.

5.2 Ring oscillator implemented in 130 nm CMOS process

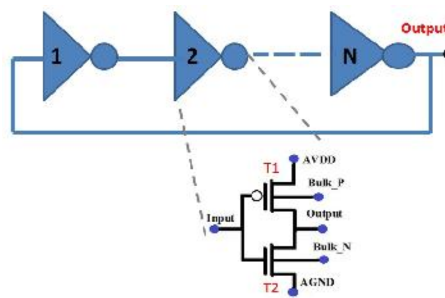
A CMOS ring oscillator is a closed loop comprising an odd number of identical inverters, which forms an unstable negative feedback circuit whose the period of oscillation is twice the sum of the gate delays in the ring. This type of oscillator is widely used because its low area, low power and high frequency capability - although it is noisier than other oscillators, as LC-tank oscillators.

A ring oscillator with eleven stages (N = 11), shown in figure 5.2, was designed using the 130 nm CMOS process. Each stage of this ring is composed by inverter with the following

dimensions: NMOS with W/L = (160 nm/130 nm) and (ii) PMOS with (W/L = 770 nm/130 nm).

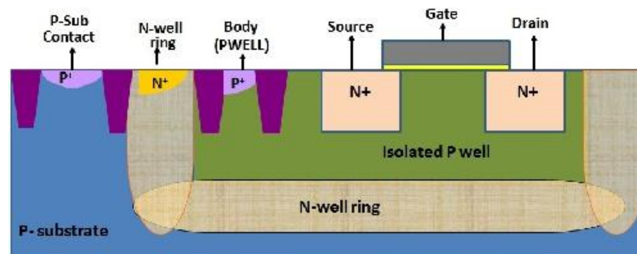
Triple-well NMOS device, shown in figure 5.3, were used due to the possibility to bias its bulk terminal since it is an isolated p-well layer. The isolation is accomplished by inserting a buried n-type layer between the local p-well and the P^- substrate. The isolating n-type layer should be tied to a quiet power supply that is at a high enough potential to prevent forward biasing the substrate diodes.

Figure 5.2 - Ring oscillator composed by CMOS inverters



Source: the author

Figure 5.3 - Triple well NMOS transistor



Source: the author

The bulk terminal of NMOS and PMOS transistors are connected to input pins in order to make possible its voltage control. The bulk bias is used for two objectives: (i) verify the impact of bulk bias in jitter performance and (ii) to allow fine tune of the oscillation frequency (f_{OSC} depends on V_{TH}, and V_{TH} depends on bulk bias).

Since the objective of this case-study in our work is the analysis of jitter or phase noise, as part of the comprehensive investigation of transistor flicker noise that have been developed in our research group, it is important to understand the impact of transistor area and number of stages on the jitter and phase noise performance.

In (ABIDI, 2006), it is presented an analytical equation for the phase noise induced by flicker noise for inverters-based ring oscillator. Verifying the proposed equation, one can verify that an improvement of phase noise (reduction of flicker noise) can be achieved if (i) number of inverter stages is increased, (ii) W/L is increased in order to flow as much current as possible, and (iii) use the longest channel length that is possible in order to increase transistor area.

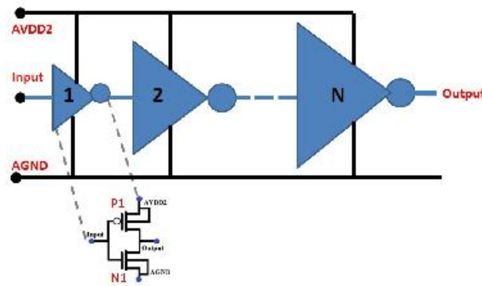
Regarding the phase noise and jitter caused by thermal noise, (ABIDI, 2006) shows that it is independent of the number of inverter stages; and it only decreases with the increase of supply voltage and the current consumption. Moreover, (ABIDI, 2006) also gives an analytical equation that converts phase noise caused by white noise into jitter. The phase noise, caused by flicker noise, is not easily analytically converter to jitter - although approximate equations can be found in literature (LIU, 2004).

We decided to have a small number of inverter stages and low area transistors in order to have a large contribution of transistor flicker noise in the jitter performance of the designed oscillator. We are especially interested on the measurement of the jitter induced by the flicker noise. More precisely, the flicker noise of transistors that are under cycle-stationary operation. And for this objective, a ring-oscillator is a useful case-study because its transistors are switching during the operation - there is no transistor constantly turned on. Moreover, the ring oscillator was designed to have the oscillation frequency (f_{OSC}) lower than 500 MHz in order to not require a precise impedance matching during the silicon measurements.

With aiming of driving low impedance loads, such as 50 of spectrum analyzer, the ring-oscillator was connected to an output buffer shown in figure 5.4. It is composed by 9 stages of inverters whose each stage is about 3 times larger than the previous one. These inverters were implemented with low V_{TH} transistors in order to save silicon area. The first stage has NMOS with W/L = (160 nm/120 nm) and PMOS with (W/L = 770 nm/120 nm). The ninth and last stage has NMOS (1049 µm/120 nm) and PMOS with (W/L = 5052 nm/120 nm). Lately, it was verified that the output buffer was over dimensioned. The supply voltages of the ring-oscillator and output buffer were connected in different pins in order to reduce induced noise caused by the switching activity of the output buffer.

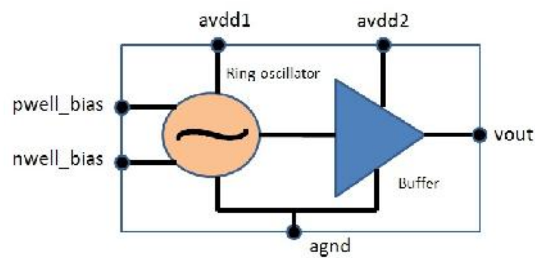
Figure 5.5 shows the complete circuit containing the ring-oscillator and the output buffer. The layout of the ring-oscillator and output buffer occupied an area of 90 µm x 45 µm and 250 µm x 132 µm, respectively. Figures 5.6 and 5.7 show the layout of the ring and output buffer.

Figure 5.4: Output buffer composed by CMOS inverters designed in 130 nm



Source: the author

Figure 5.5: Oscillator and output buffer design in 130 nm



Source: the author

Figure 5.6: Layout of the ring-oscillator design in 130 nm

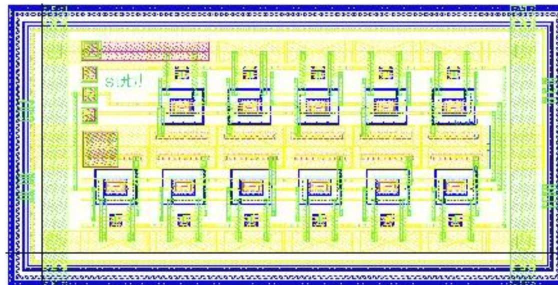


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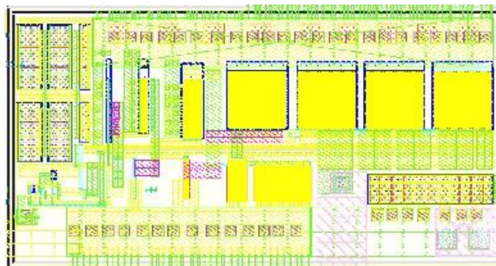
Figure 5.7: Layout of the output buffer designed in 130nm process



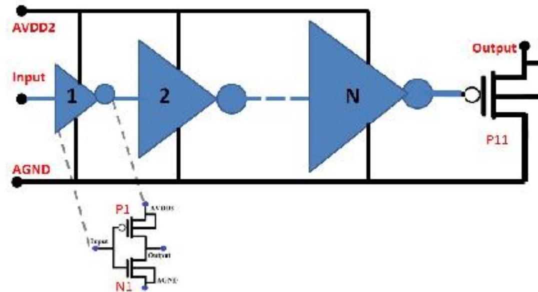
Source: the author

5.3 Ring oscillator implemented in 45 nm CMOS process

During the Ph.D. internship at Texas Instruments, a CMOS inverter-based ring-oscillator with the same topology of that one shown in figure 5.2 was also designed but using 45 nm CMOS process. With fifteen inverters (N = 15), each stage is composed by an inverter with NMOS with W/L = (330 nm/110 nm) and (ii) PMOS with (W/L = 870 nm/110 nm). Each stage has a layout area of 6 µm x 12 µm, while the ring oscillator has 75 µm x 26 µm.

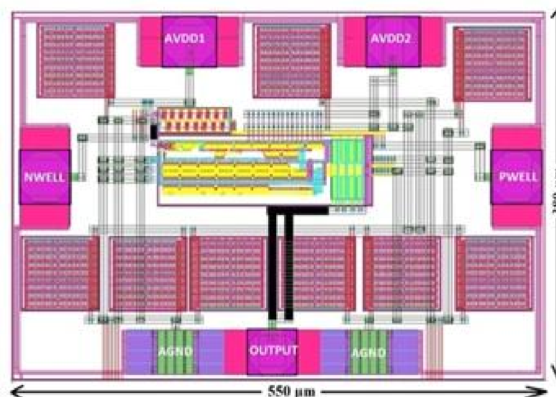
Triple well devices were also used in order to allow bulk bias. The output buffer is similar than one shown in figure 5.4 with exception of the last stage that is composed by a common source amplifier as shown in figure 5.8. The output node of P_{11} is connected to a power supply voltage by means of a variable resistor used to set the output impedance nearly to 50 . The output buffer is composed by 10 inverter stages and a common source amplifier and its total area is 220 µm x 73 µm.

Figure 5.8 - Output buffer designed in 45 nm process



Source: the author

Figure 5.9 - Layout of ring oscillator designed in 45 nm process



Source: the author

Figure 5.9 shows the layout of the complete circuit containing the ring oscillator and the output buffer. The total area is 550 µm x 380 µm. As can be seen, there are 4 DC pads for the supply lines (oscillator and buffer), and bulk bias (PMOS and NMOS). The output voltage is available through a RF pad with Ground-Signal-Ground configuration (GSG). There are a lot of decoupling capacitors surrounding the supply nodes.

5.4 Cross-coupled LC tank oscillators

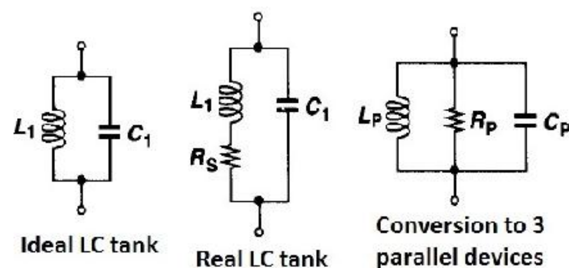
LC resonator-based oscillators have larger area than ring-oscillator but it achieves higher oscillation frequencies and better phase noise performance (ABIDI, 2006). The development of LC oscillators only became possible due to the integration of planar inductors, which are typically implemented as metal spiral structures (DOS ANJOS, 2012).

In order to understand the LC tank oscillator, we start presenting the ideal LC tank shown in figure 5.9. It is composed by an inductor L_1 and a capacitor C_1, and it resonates at f_{OSC} given by equation (5.2) (RAZAVI, 2001):

$$fosc = \frac{1}{2\pi\sqrt{L_1 \cdot C_1}} \quad (5.2)$$

However, if the inductor is real, a more realistic LC-tank is still shown in figure 5.9, where R_S models the series resistance in the wire of the inductor. The exact resonance frequency of the real LC tank has some dependency of R_S, but it is yet well approximated by equation (5.2) (RAZAVI, 2001).

Figure 5.9 - Ideal, realistic LC-tank and its conversion



Source: (RAZAVI, 2001)

The quality factor of the LC-tank, given by equation 5.3, is defined as the energy stored to the energy dissipated per cycle. Typically, the Q_L of the inductor

dominates the total Q of the tank circuit, and then, $Q \sim Q_L$ (Bunch, 2002). The quality factor of L_1 is given by (5.4) (RAZAVI, 2001):

$$Q = 2 \cdot \pi \cdot \frac{Maximum\ energy\ stored}{energy\ dissipated\ per\ cycle} \tag{5.3}$$

$$Q_L = \frac{L_1 \cdot \omega_{OSC}}{R_S} \tag{5.4}$$

In order to make the circuit analysis easier, the inductor L_1 with R_S can be converted to an inductor L_P in parallel with a resistor R_P. The LC-tank with three devices in parallel is shown in figure 5.9, where L_P L_1, $C_P = C_1$, and R_P is described by equation (5.5) (RAZAVI, 2001).

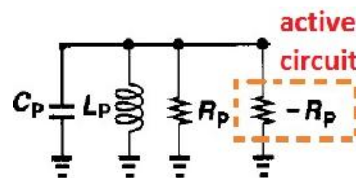
$$R_P \approx \frac{L_1^2 \cdot \omega_{OSC}^2}{R_S} \approx Q^2 \cdot R_S \tag{5.5}$$

The series to parallel conversion is not valid for frequencies substantially differently than f_{OSC} (RAZAVI, 2001). At f_{OSC}, the tank impedance is reduced to R_p and there is no phase difference between current and voltage of the tank. Moreover, the relation of R_P, f_{OSC} and Q is given by equation (5.6) (Rogers, 2010):

$$R_P = 2\pi \cdot f_{OSC} \cdot L_p \cdot Q \tag{5.6}$$

If a current impulse stimulates the LC-tank shown in figure 5.9, an oscillation starts but it decays in every cycle because energy is lost in the form of heat in the resistor. If a resistor with resistance "$-R_P$" is placed in parallel with resistor R_P as shown in figure 5.10, the LC-tank oscillates indefinitely (RAZAVI, 2001). The topology shown in figure 5.10 is called one-port oscillator.

Figure 5.10 - One port oscillator



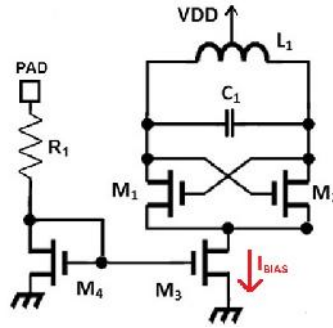
Source: (RAZAVI, 2001)

The negative resistance can be implemented by means of an active circuit with a loop gain sufficiently negative (RAZAVI, 2001) as will be presented in section 5.4.1. A negative resistance (an incremental quantity) indicates that if the applied voltage increases, the current drawn by the active circuit decreases.

5.4.1 NMOS cross couple LC-tank

The cross couple LC-tank, also called "negative-G_m oscillator", is shown in figure 5.11 ant it generates $-R_P$ between the LC tank terminals by means of the transistors M_1 and M_2.

Figure 5.11- NMOS cross couple LC-tank oscillator



Source: the author, based on (RAZAVI, 2001)

The small signal resistance (R_{DPAIR}) seen from drain nodes of M_1 and M_2 is given by equation (5.7) (RAZAVI, 2001) if one considers that $g_m >> g_{ds}$ (large value of R_{DS}) and $g_m = g_{m_M1} = g_{m_M2}$.

$$R_{DPAIR} \approx \frac{-2}{g_m} \tag{5.7}$$

Note that R_{DPAIR} is the implementation of $-R_P$ shown in figure 5.10. The parallel combination (R_{eq}) of R_{DPAIR} and R_P is given by equation (5.8):

$$R_{eq} \approx \frac{(-2 \cdot R_P/g_m)}{R_P - \frac{2}{g_m}} \tag{5.8}$$

Note that the minimal condition for oscillation is when R_{eq} is infinite and it happens when the denominator of (5.8) is zero. In this condition, there is no loses in the LC-tank and it oscillates continually. It means that the dissipated energy in R_P is restored by the energy produced by active circuit.

If the denominator is positive, R_{eq} is negative and the circuit experience large swings such that each transistor is nearly off for part of the period, thereby yielding an "average" resistance of $-R_P$ (RAZAVI, 2001).

If the denominator is negative, R_{eq} is positive and the oscillation decays due to the heat dissipation in the resistor. For that reason, in order to have to a continuous oscillation, equation (5.9) must be satisfied:

$$g_m \geq \frac{2}{R_P} \tag{5.9}$$

The LC-oscillator is fully differential and voltages at the drains of M_1 and M_2 are 180° shifted. The advantage to be differential is the common mode voltage rejection, as for instance, reducing noise coming from V_{DD}.

The start-up procedure of the LC oscillator works as follow. At time zero (t_0), the oscillator starts with both drain nodes nearly equal to the V_{DD}, and M_1 and M_2 sharing I_{BIAS} provided by current source M_3. Thus, at t_0, $I_{DS_M1} = I_{DS_M2} = I_{BIAS}/2$.

Noise components at the oscillation frequency are then amplified by devices M_1 and M_2, and as a consequence, the oscillation starts to grow. Since $I_{DS_M1} + I_{DS_M2} = I_{BIAS}$, when the drain voltage of M_1 (M_2) increases, I_{DS_M1} decreases (increases). The oscillation amplitude grows until the loop grain drops at the peak. If the gain is large enough, I_{DS_M1} e I_{DS_M2} varies from I_{BIAS} to zero, turning off one transistor while the other is conducting the entire I_{BIAS}.

The single ended output voltage swing in the above condition is given by (5.10) (Rogers, 2010). At high frequencies, the current waveform may be approximated more closely by a sinusoid (not square any more) and the tank amplitude can be better approximated as (5.11) due to the finite transistor switching time and limited gain. (HAJIMIRI, 1999):

$$V_{OUT_SE} = \frac{R_P \cdot I_{BIAS}}{\pi} \tag{5.10}$$

$$V_{OUT_SE} \approx R_p \cdot I_{BIAS} \tag{5.11}$$

The above mode of operation is referred as current-limited (HAJIMIRI, 1999), where the tank amplitude is solely determined by the tail-current source and the tank equivalent resistance.

If I_{BIAS} is continuously increased, V_{OUT} increases and approaches the supply voltage. At this condition, NMOS devices will enter in triode region at the peak of the voltage. Moreover, even the tail current device (M_3) may operate in linear region. This operation is called voltage-limited because further increase in I_{BIAS} will not increase V_{OUT_SE} because it is limited by the supply voltage and/or triode operation (HAJIMIRI, 1999).

As described above, I_{BIAS} limits the amplitude of the oscillation and defines the power consumption. It is desirable to have I_{BIAS} with low noise performance, since its low-frequency noise (flicker noise) significantly degrades the phase noise because it is converted to

frequencies around F_{OSC}. Therefore, M_3 and M_4 were designed with large area larger than 100 μm^2.

Regarding phase noise performance (remember that phase noise is the ratio of noise power by carrier power), the increase of I_{BIAS} results in increased V_{OUT} and improved phase noise performance (HAJIMIRI, 1999) as soon the oscillator operated in current limited mode.

For voltage-limited mode, V_{OUT} does not increase with I_{BIAS} and as a thus, the optimum operation point regarding phase noise for the LC-tank is the edge of voltage-limited operation as recommend by (HAJIMIRI, 1999).

Regarding the parasitic, it is important to note that drain junction capacitances of M_1 and M_2 are connected to the tank and it affects F_{OSC}. As these junction capacitances depends on the transistor gate source voltage, it varies as a function of V_{DD}. It is desirable to have C_1 much larger than the parasitic capacitances. Thus, devices M_1 and M_2 were designed with length equal to twice the minimum value permitted by the technology (*i.e.* $L_{M1} = L_{M2} = 80$ nm).

Many applications requires that the LC oscillator has its output frequency as a function of a control input voltage ($V_{CONTROL}$). The tuning voltage is used to deal with the impact of fabrication process and temperature, and consequently guaranteeing the correct oscillation frequency for the application. $V_{CONTROL}$ is usually used to change C_1, commonly implemented by means of varactors (Ham, 2001).

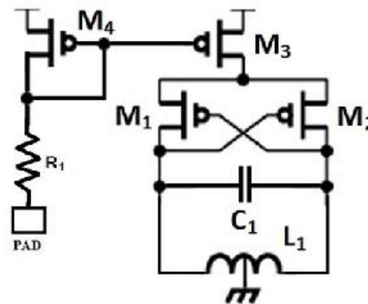
However, the input control voltage may inject noise in the oscillator circuit thus worsening the phase noise performance. In order to avoid this type of noise and make easier the silicon measurements, it was decided to not use any input control voltage.

5.4.2 PMOS cross couple LC-tank

An alternative implementation of the cross-couple LC-tank oscillator using PMOS devices is shown in figure 5.12. The NMOS and PMOS versions provides swings around V_{DD} and GND potentials, respectively. Since g_m of PMOS are lower than NMOS (*i.e.* hole mobility < electrons mobility), M_1 and M_2 aspect ratios of the PMOS version should be larger than the NMOS version (*e.g.* ~ 2 or 3 times). As a consequence, the parasitic capacitances of the PMOS version tends to be a bit larger than the NMOS version.

An advantage of the PMOS version is the improved phase noise performance than compared to the NMOS version (Yoon, 2004). The better phase noise performance of PMOS compared to NMOS version was verified in our designed circuits and it is shown in simulation sections. The improvement is due to the fact that PMOS devices have low flicker noise than NMOS devices. This statement is true for the 45 nm CMOS process used in this thesis, and it may be not true for other CMOS technologies.

Figure 5.12- PMOS cross couple LC-tank oscillator



Source: the author, based on (RAZAVI, 2001)

5.4.3 Integrated Inductor

As discussed in Chapter 3, phase noise is one of the main important performance parameters of oscillators. Based on the phase noise analytical model proposed by (LEESON, 1996) and (HAJIMIRI, 1998), the phase noise is inversely proportional to the inductor quality factor and the power consumption. As a consequence, when very low noise performance is required, the maximum allowable current is burned and off-chip inductors with high quality inductors are employed (DOS ANJOS, 2012).

Some of the reasons why on-chip inductors doe not achieve high Q are the metal and substrate losses. Metal losses include finite conductivity of the metals, current crowding at the edge because the skin effect and proximity effects caused by a nearby metal layer. Substrate losses include the parasitic and eddy currents (YOON, 2004).

Skin effects is the tendency of an alternating electric current to become distributed within a conductor such that the current density is largest near the surface of the conductor, and decreases with greater depths in the conductors. The current flows mainly at the "skin" of the conductor and causes the effective resistance of the conductor to increase at higher frequencies where the skin depth is smaller. This phenomena is caused by the induced

Foucault or Eddy currents generated by the changing of the magnetic field created by the AC current in the conductor (DOS ANJOS, 2012). At DC, there is a constant current density in the conductor what makes its effective resistance to be lower than at AC conditions.

When two conductors are near to each other, as the case of inductors, induced Eddy currents are also generated by the change of the magnetic field caused by neighboring conductors. This phenomena is called proximity effects (DOS ANJOS, 2012) and similarly to the "skin effect", it results in a redistribution of the current densities (*i .e.* high density in the farthest edge from the magnetic field in the conductors that increases the effective resistance).

One could model the silicon substrate as a ground resistor in series with a capacitance between the spiral and the substrate (BUNCH, 2002). This capacitance allows RF currents to interact with the substrate, lowering the inductor value and inserting losses (BUNCH, 2002). Moreover, Eddy currents are also induced in the silicon substrate and due to the ohmic losses, it are also reflected back to the inductor therefore increasing the series resistance of the inductor.

Alternative solutions for achieving high-quality inductors is the use of bonding wires (*e.g.* Q on the order of 50). However, the inductance of a bonding wire suffers large variations since its mechanical fabrication process is not so tightly controlled as photolithographic process. Moreover, monolithic inductors fabricated as planar spirals using GaAs substrate achieves Q on the order of 20 - 40 (BUNCH, 2002). For silicon process, Q is usually lower than 20.

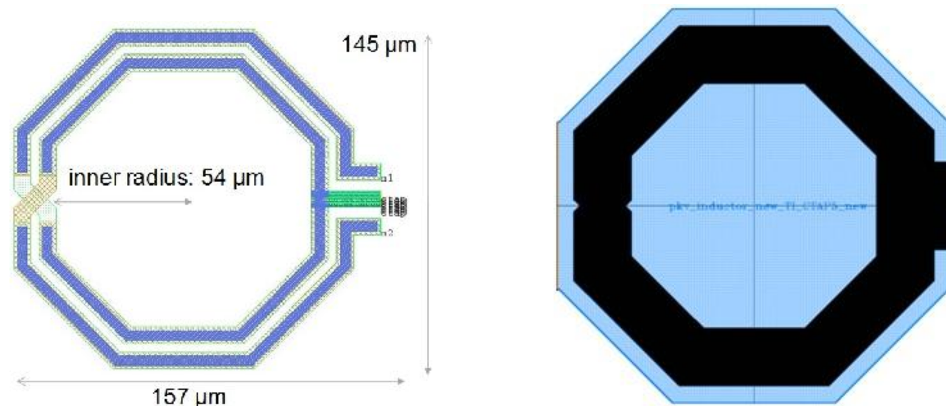
In (HAM, 2001) it is presented a design methodology in order to find the optimum value of L_1 and C_1 for a given oscillation frequency specification. This work suggests the use of minimum inductance value that satisfies both the tank amplitude and startup constraints for the maximum bias current allowed by the design specifications. In this condition, there is no waste of inductance and power, while achieving the best phase noise performance. Moreover, it suggests the operation at the edge of the current-limited operation.

For the design of the integrated inductor we have used the PeakView EMD of Lorentz solution (http://www.lorentzsolution.com/). This software is an electromagnetic simulator for on-chip passive devices synthesis. The designer configures the physical dimensions of the inductor, and by means of an electromagnetic analysis, the tool provides the performance parameters, as for instance, inductance and quality factor. After the design of the inductor, the

physical-based-model utility of PeakView generates a compact circuit equivalent model proper for transient simulation using Spectre. The tool also generates the layout of the inductor.

Figure 5.13 shows the designed center-tap integrated inductor design for an oscillation frequency of 2.5 GHz. The windings are done with two top metals in parallel in order to decrease the series resistance. The center tap connection was implemented using four metals in parallel. Moreover, The largest metal width available in the technology was used and a ~3 µm of spacing between each windings in order to maximize the inductance (YOON, 2004).

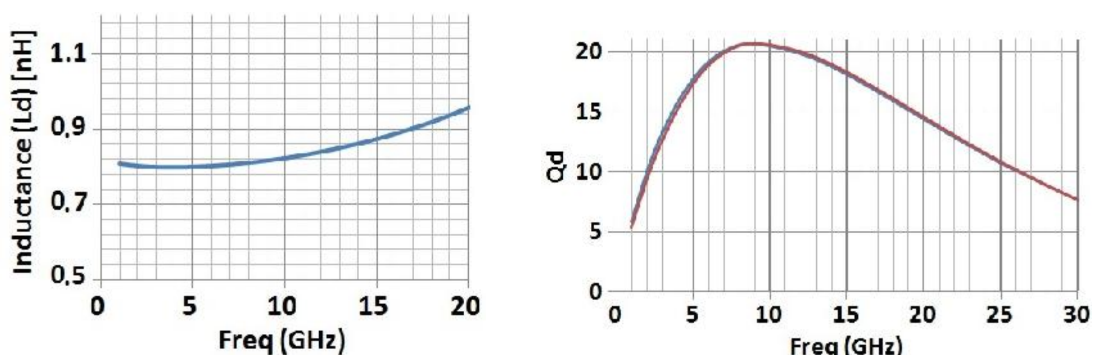
Figure 5.13 - Layout of L_1 before (left) and after metal filling (right)



Source: the author

With 2 turns and 8 sides, an inductance of L_1 = 0.8 nH was achieved. The right part of figure 5.13 shows the designed inductor after metal filling done by the designer. Figure 5.14 shows the simulated L_1 and its quality factor (Qd) as a function of frequency. At 2.5 GHz, Q equal to 11 is achieved for the metal filled inductor.

Figure 5.14 - Simulated inductance (Ld) and quality factor (Qd)



Source: the author

5.4.4 Designed oscillators

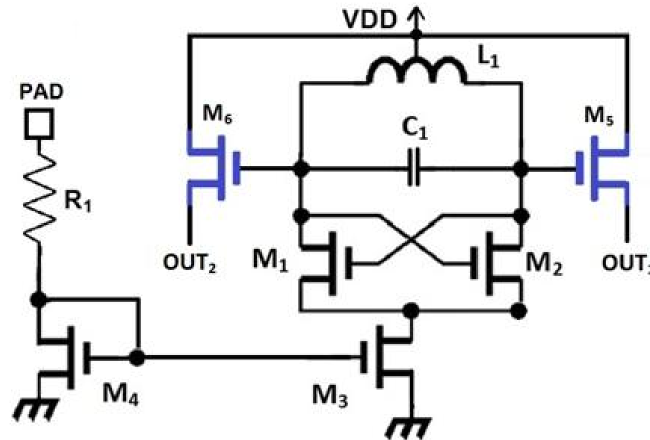
Using the concepts and equations presented in section 5.4, four cross-couple LC-tank oscillators were designed using 45-nm CMOS process. As mentioned early, the objective of this work is not the optimum design of a LC-tank oscillator, but the study of flicker noise under cycle-stationary operation and its electrical simulation using modified electrical simulator.

Three versions (OSC_{N1}, OSC_{N2} and OSC_{N3}) of the NMOS cross-couple LC-tank shown in figure 5.11 were designed . The g_m pairs of OSC_{N1} and OSC_{N2} were implemented using analog-friendly transistors that present better flicker noise performance compared to core (digital) transistors. OSC_{N3} was implemented using core transistors. The forth version, OSC_{P1}, is the PMOS topology shown in figure 5.12 implemented with analog-friendly transistors. Note that the g_m-pair transistors of the PMOS version (OSC_{P1}) have area twice larger than the NMOS version (OSC_{N1}) due to the g_m requirement and lower carrier mobility. The g_m-pair transistors for OSC_{N1}, OSC_{N2} and OSC_{N3} were implemented using triple well devices (figure 5.3) in order to make possible the bulk bias.

The goal of having the same circuit implemented with different devices was the evaluation of flicker noise in different devices. The difference between OSC_{N1} and OSC_{N2} is the size of the g_m-pair transistors. OSC_{N2} were purposely designed with g_m-pair transistors with smaller area than OSC_{N1} in order to have worse flicker noise and phase noise performance. The goal of having an oscillator with not optimized flicker noise performance is to maximize the bulk bias effects - used to decrease flicker noise.

In order to drive a 50- input impedance of the spectrum analyzer during the phase noise measurements, the oscillator outputs were isolated by means a source follower as shown in figure 5.15. Nodes OUT_1 and OUT_2 also provide the DC bias for M_5 and M_6 through a variable resistor (R_{LOAD} - not shown in this figure) connected to ground. The resistor load can be initially set to be 50 , and later, it can be swept in order to verify the impact of the buffer in the phase noise performance. The PMOS version (OSC_{P1}) employs a PMOS source-follower whose source terminal is connected to VDD through R_{LOAD}.

Figure 5.15. NMOS cross-coupled LC tank oscillator with source follower



Source: the author

Table 5.1 shows the dimensions of the key devices of all designed circuits. M stands for multiplicity. The nominal supply voltage is 1.1 V and all of them were designed to operate with fosc ~ 2.4 - 2.5 GHz and I_{BIAS} = 5.5 mA. This range of frequency is inside of WLAN and WiMAX bands. All oscillators were designed using the inductor presented in 5.4.3. The design circuits were planned to measured at wafer level.

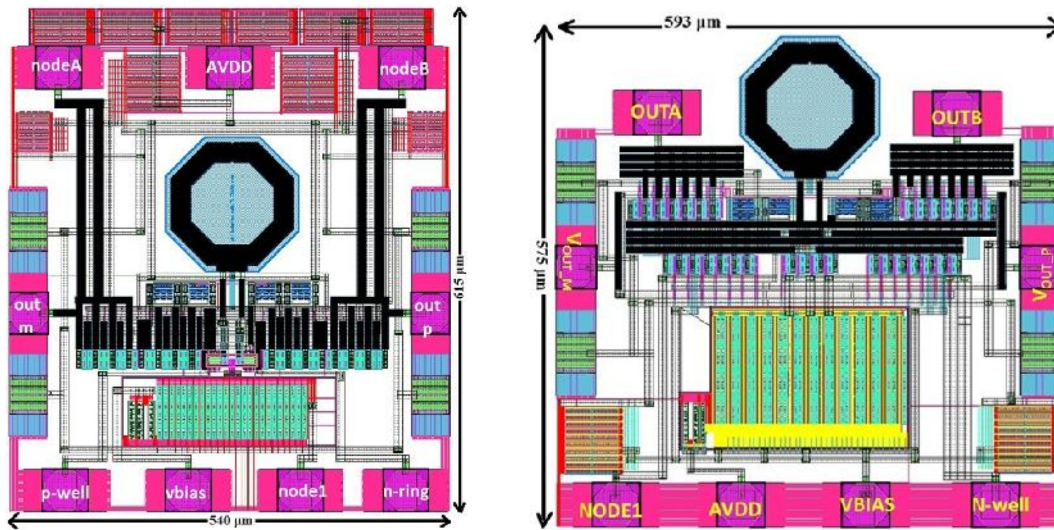
Figure 5.16 shows the layout of OSC_{N3} and OSC_{P1}, whose total area is 540 µm x 615 µm, and 593 µm x 575 µm, respectively. DC pads were used for the supply voltage and I_{BIAS} (node PAD in figure 5.5), while GSG pads were used for OUT_1 and OUT_2. Figure 5.17 shows the layout of the g_m pair for the OSC_{P1}. All the routing were done with two or more metals in parallel in order to reduce the metal resistance.

Table 5.1: Devices Dimensions

Device	circuit	type	width (µm)	M	length (µm)	C_1 (pF)	L_1 (nH)	R_1 ( )	f_{OSC} (GHz)
$M_{1,2}$	OSC_{N1}	analog	90	2	0.08	2.913	0.8	85	2.561
$M_{1,2}$	OSC_{N2}	analog	30	2	0.08	2.913	0.8	85	2.557
$M_{1,2}$	OSC_{N3}	core	96	2	0.08	2.913	0.8	85	2.541
$M_{1,2}$	OSC_{P1}	analog	96	4	0.12	3.399	0.8	87	2.411

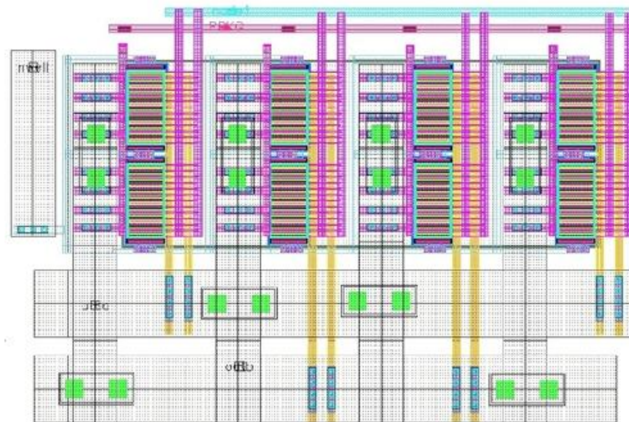
Source: the author

Figure 5.16 - Layout of OSCN3 (left) and OSCP1 (right)



Source: the author

Figure 5.17 - Layout of the gm-pair of OSCP1



Source: the author

5.5 Post-extraction simulation results

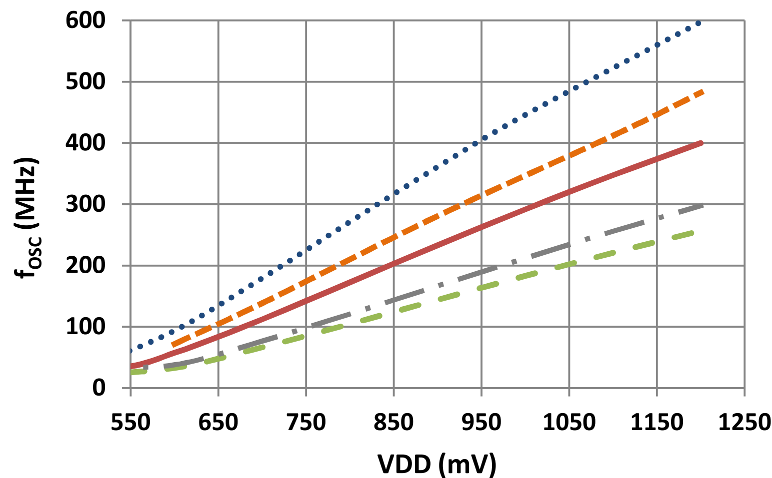
All simulation results presented in this section were carried out using the traditional flicker noise device model (BSIMV4).

5.5.1 Inverter-based ring oscillator (11 stages) using 130 nm CMOS process

Figure 5.18 shows the oscillation frequency (f_{OSC}) as a function of supply voltage using transistor corner models. In this simulation, the supply voltages of ring and output buffer are

connected together. As one can see, f_{OSC} is approximately linear with the supply voltage. It happens because the rise and fall time of a CMOS inverter are inversely proportional to the supply voltage (WESTE, 1993). Note that f_{OSC} is inversely proportional to the inverter-gate delay, as described by equation 1.2.

Figure 5.18 - f_{OSC} vs. VDD using corner models: FF (dots), FS (broken line), TT (line), SF (line and dots), SS (broken line)



Source: the author

Table 5.2 shows f_{OSC} using transistor corner models for following supply voltages: 700 mV, 800 mV, 900 mV and 1000 mV. Using typical models and a supply voltage of 700 mV, the oscillation frequency is 111.2 MHz.

The total frequency variation (Δf_{OSC}) considering a supply voltage variation of 700 mV (1200 mV - 500 mV) is 363.14 MHz at typical conditions, which represents ~ 518 kHz/mV. This large voltage - frequency gain shows how the ring circuit is sensitivity to supply noise.

Figure 5.19 shows the RMS supply current (I_{OSC}) for the ring oscillator as a function of supply voltage. As one can see, I_{OSC} has an exponential dependence of the supply voltage (SEDRA, 1997). For a supply voltage of 700 mV, $I_{OSC} = 61$ µA at typical conditions.

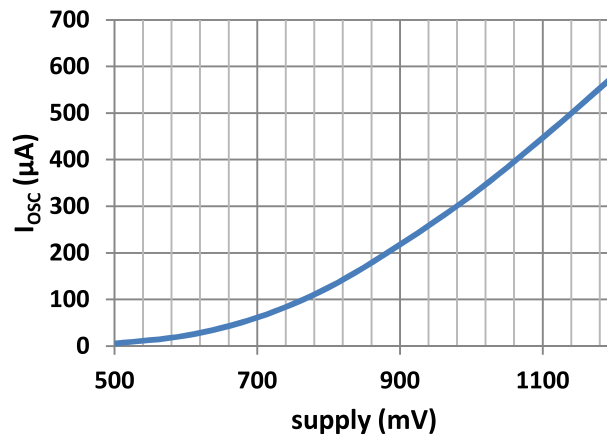
Figure 5.20 shows the simulated power spectrum for the ring oscillator measured at a 50-resistor (modeling the input of the spectrum analyzer) connected at the ring-oscillator output. The supply voltage is 850 mV and the fundamental frequency is 202.8 MHz, while the other harmonics can be seen in this figure. Note that power spectrum shown in figure 5.20 is ideal (similar to that one shown figure 3.6) because the noise sources (*e.g.* thermal, flicker, supply noise) is not taken into account.

Table 5.2: f_{OSC} vs. supply for ring-oscillator designed in 130 nm process

Supply voltage (mV)	f_{OSC} (MHz)				
	TT	SS	FF	SF	FS
700	111.2	66.3	179.3	76.7	138.6
800	172.4	104.4	271.3	120.9	208.7
900	232.9	143.8	361.1	166.6	280.8
1000	291.6	182.8	446	211.9	345.4

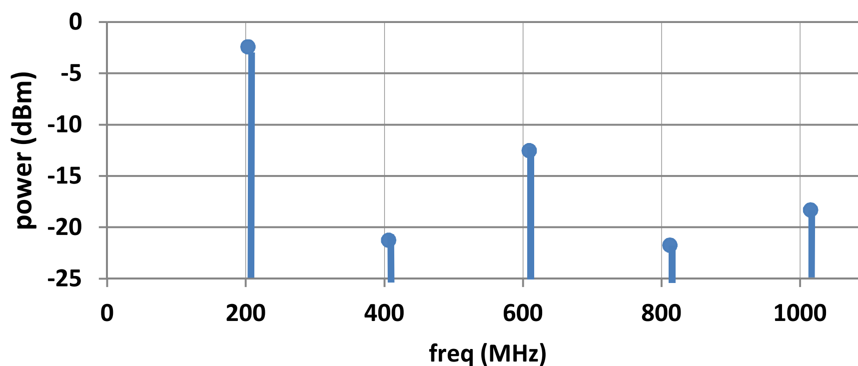
Source: the author

Figure 5.19 - I_{OSC} (µA) vs. supply (mV)



Source: the author

Figure 5.20 - Simulated power spectrum (dBm) for the ring-oscillator



Source: the author

As shown in table 5.2, f_{OSC} is 111.2 MHz when the supply voltage is 700 mV. Figure 5.21 shows the impact of bulk bias on f_{OSC}. The left plot shows f_{OSC} as a function of the NMOS

bulk bias varied from -300 mV (reverse bias) to + 300 mV (forward bias). As the bulk-source voltage (V_{BS}) is increased (forward bias), V_{TH} is decreased and thus, I_{DS} and f_{OSC} are increased. The voltage - frequency gain for the bulk bias is around 81 kHz/mV - more than 6 times smaller than the gain controlled by the supply voltage.

The right plot of figure 5.21 shows the impact of PMOS bulk bias on f_{OSC}. The abscissa axis is the PMOS bulk bias. Since the source of PMOS transistor are connected to the supply voltage (700 mV), for V_B = 900 mV (a reverse bias of V_{BS} = 200 mV is applied); and for V_B = 400 mV (a forward bias of V_{BS} = - 300 mV is applied). The voltage - frequency gain for the bulk bias is ~ 85 kHz/mV - almost the same for the NMOS bulk bias.

Figure 5.21 - Simulated effect of bulk bias on f_{OSC}: NMOS (left) and PMOS (right)

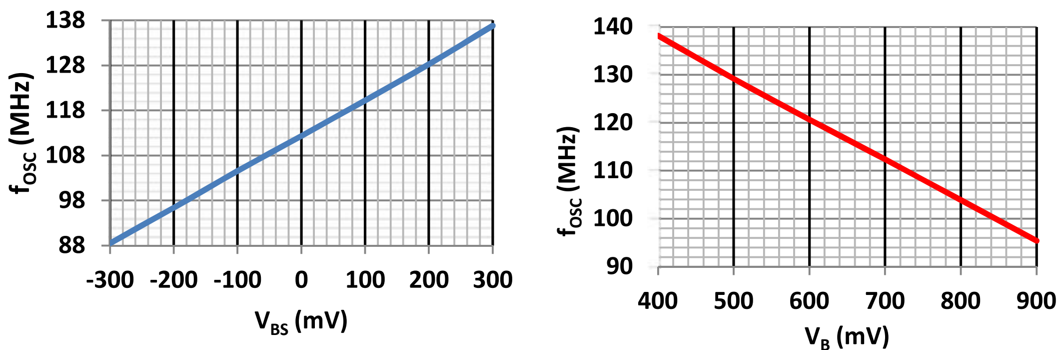


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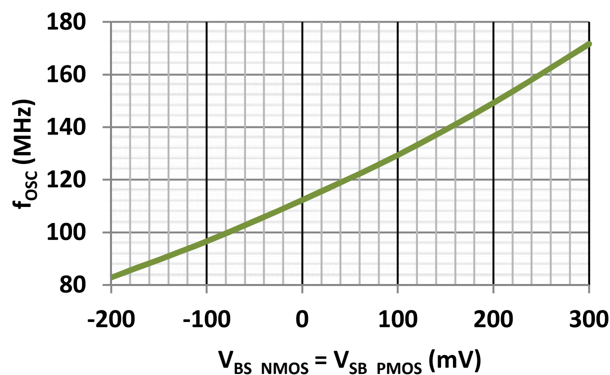
Figure 5.22 - Simulated effect of bulk bias on f_{OSC} for both devices simultaneously

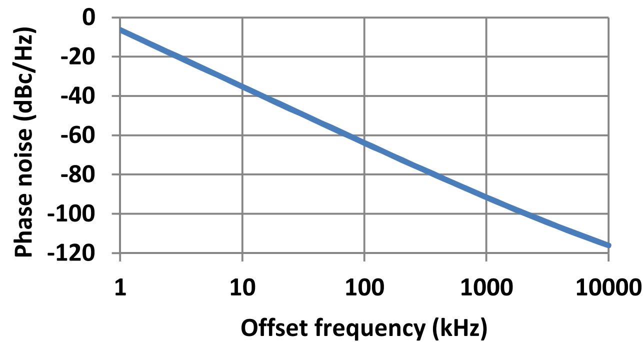


Source: the author

Figure 5.22 shows the impact of bulk bias on NMOS and PMOS devices simultaneously. The bulk bias is swept in the same direction for both devices. The voltage - frequency gain for this case is 177 kHz/mV, approximately the sum of separated voltage-frequency gains for NMOS and PMOS devices.

Figure 5.23 shows the phase noise for the ring-oscillator as a function of offset carrier when both ring and buffer are supplied with 700 mV. The curve crosses the x-axis at ~ 614 Hz. At 1kHz, 10 kHz and 100 kHz of offset frequency, phase noise is -36 dBc/Hz, -64 dBc/Hz and - 92 dBc/Hz, respectively.

Figure 5.23 - Simulated Phase noise vs. offset frequency for 130-nm ring oscillator



Source: the author

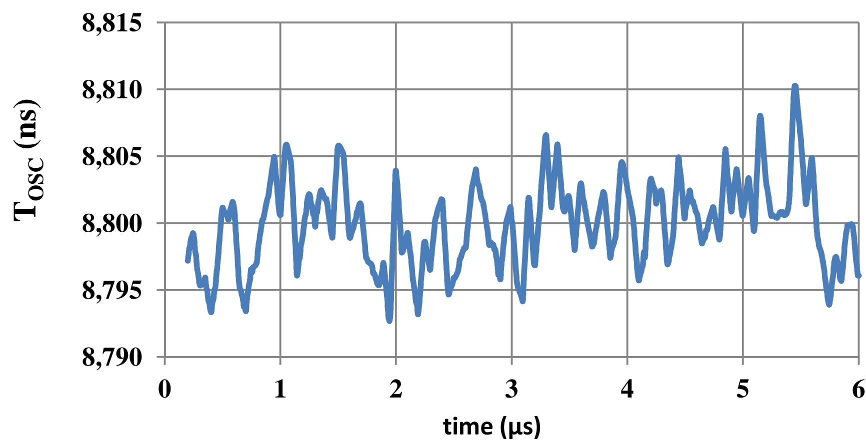
The transient noise simulation, described in section 3.5, was performed in order to estimate the variation of the oscillation period (T_{OSC}) due to the noise sources when both ring and buffer are supplied with 700 mV. At each time step, noise source are evaluated and the output noise is modulated leading to frequency variation as shown in the figure 5.24, where T_{OSC} (inverse of oscillation frequency) is plotted as a function of time.

Figure 5.25 shows the histogram of T_{OSC} for the 100 μs transient noise simulation, where the mean and sigma of T_{OSC} is 8.781 ns and 3.7 ps, respectively. The maximum and minimum values of T_{OSC} are 8.793 ns and 8.768 ns, respectively. A simulation with duration of 100 μs means that all noise sources with frequency higher than 10 kHz can be included in the noise calculation if the analysis is properly configured. For example, in order to include noise sources at 100 Hz, the simulation would have to last 10 ms, at least. The sigma of T_{OSC} is usually referred as Period jitter, as described in section 3.7.

Table 5.3 shows the T_{OSC} as a function of bulk bias for ten conditions. As the ring-oscillator is supplied with 700 mV, V_{BULK} smaller than 700 mV means forward bulk bias. For the NMOS bulk bias, V_{BULK} larger (smaller) than 0 means forward (reverse) bulk bias. As can be seen in table 5.3, the sigma of T_{OSC} decreases when forward bulk bias is applied. When forward bulk bias is applied, there is a reduction of V_{TH} and the transistors of the ring-oscillator tend to operate at higher level of inversion. At 700 mV of power supply, the ring-oscillator transistors operate at the most part of time in moderate and weak inversion.

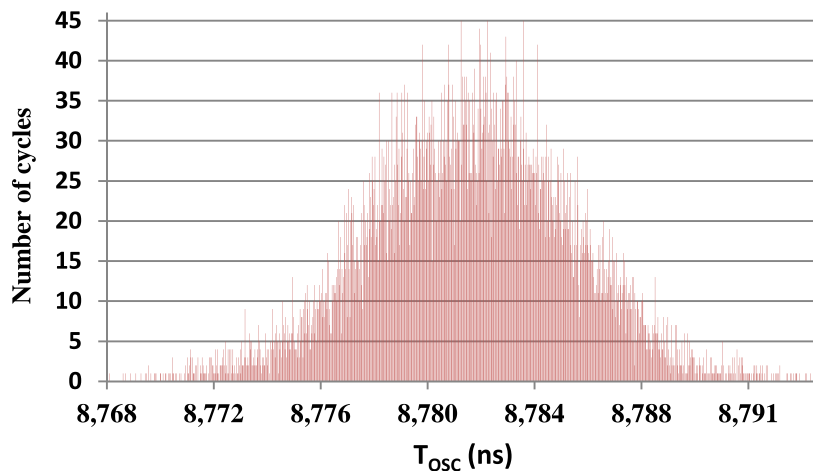
Increasing the transistor inversion level leads to a reduction of transistor gain and g_m/I_{DS}. As a consequence, there is a lower propagation of the transistor flicker noise to the oscillator jitter. A reduction of transistor gain means that fluctuations in the gate voltage terminal (*e.g.* flicker noise) leads to smaller fluctuation of I_{DS}. A second simulation which V_{TH} was swept shows that the sigma of T_{OSC} decreases as V_{TH} decreases.

Figure 5.24 - T_{OSC} (ns) vs. time (µs) using transient noise analysis



Source: the author

Figure 5.25 - T_{OSC} (ns) vs. number of cycles



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Finally, the last line of table 5.3 shows the ratio of sigma/T_{OSC}. Since the jitter is related to the oscillation period, this normalization can be used as a comparison parameter when verifying the jitter under different bias conditions.

Table 5.3: T_{OSC} (ns) and sigma (ps) as a function of bulk bias (V_{BULK})

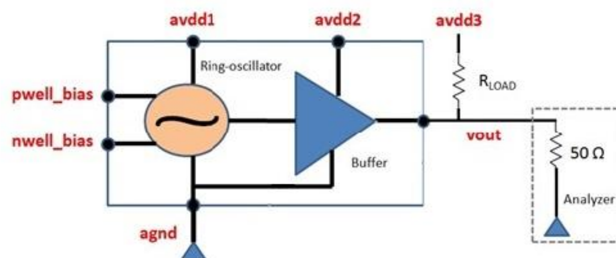
Parameter	V_{BULK} (mV)									
pmos bulk:	700	700	700	700	700	600	500	400	600	500
nmos bulk:	0	-100	100	200	300	0	0	0	100	200
T_{OSC} (ns)	8.781	9.432	8.106	7.694	7.213	8.19	7.658	7.169	7.638	6.636
Max (ns)	8.793	9.447	8.216	7.703	7.221	8.202	7.669	7.181	7.648	6.644
Min (ns)	8.768	9.416	8.195	7.684	7.204	8.178	7.646	7.157	7.627	6.627
Sigma (ps) (Jitter)	3.7	5.1	3.4	2.9	2.5	3.8	3.7	3.3	3.3	2.8
Sigma/T_{OSC} (10^{-4})	4.2	5.4	4.2	3.7	3.5	4.6	4.8	4.6	4.3	4.2

Source: the author

5.5.2 Inverter-based ring oscillator using 45 nm CMOS process

Figure 5.26 shows the test bench used to simulate the ring-oscillator with R_{LOAD} equal to 50 . The oscillation frequency (f_{osc}), output voltage swing and the phase noise were simulated using Spectre simulator. The phase noise simulation was performed using PSS and PNOISE analysis, and the traditional mosfet flicker noise model provided by foundry.

Figure 5.26 - Test bench for the ring-oscillator simulation



Source: the author

Supply voltages avdd1 and avdd2 are nominally equal to 1.1 V; and avdd3 is 1.8 V. The ring-oscillator is implemented by digital transistors and the last stage of the output buffer is a common source amplifier implemented by means of analog transistors that supports 1.8 V.

The RMS supply current at nodes avdd1 and avdd2 are 88 μA and 16.6 mA, respectively at nominal conditions. The nominal values of V_{TH_N} and V_{TH_P} are 417 mV and -458 mV, respectively.

Table 5.4 shows the post-extracted performance parameters using nominal, weak and strong models. At nominal process and with VDD = 1.1 V, f_{osc} is 666.7 MHz. The minimum and maximum frequency oscillation using weak and strong models are 593 MHz and 747 MHz, respectively, what represents a total variation of 153 MHz. Voltage swing is the peak to peak output voltage amplitude. Phase noise at 5 kHz, 10 kHz and 100 kHz away from the carrier (666.7 MHz) is given in table 5.3.

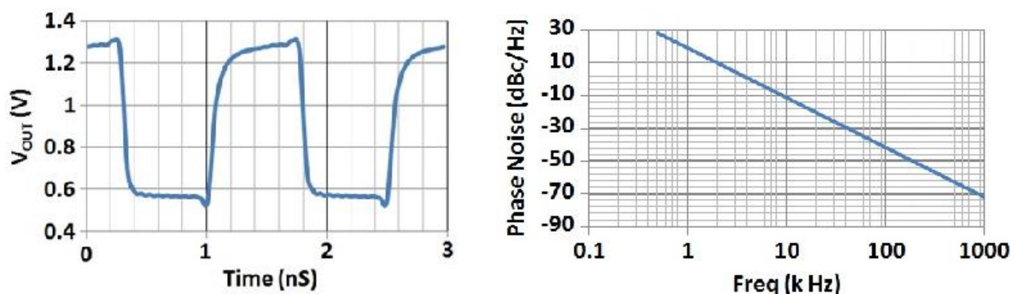
Table 5.4: Post-extracted performance for 45 nm ring at VDD = 1.1 V

Transistor Models	f_{OSC} (MHz)	Voltage Swing (mV)	phase noise at 5 kHz (dBc/Hz)	phase noise at 10 kHz (dBc/Hz)	phase noise at 100 kHz (dBc/Hz)
nominal	666.7	730	-3.3	-12.4	-42.8
weak	593.6	718	-4.0	-13.2	-43.5
strong	747.4	768	-2.5	-11.7	-42

Source: the author

Figure 5.27 shows the transient simulation and the phase noise analysis using nominal process. As can be seen in the phase noise plot, for offset frequencies lower than ~ 5 kHz (close-in phase noise), the simulator predicts a positive value quantity. It would mean that noise power is larger than the carrier power, what naturally there is no physical meaning. This is a known limitation of traditional electrical simulators when simulating phase noise of noisy oscillators.

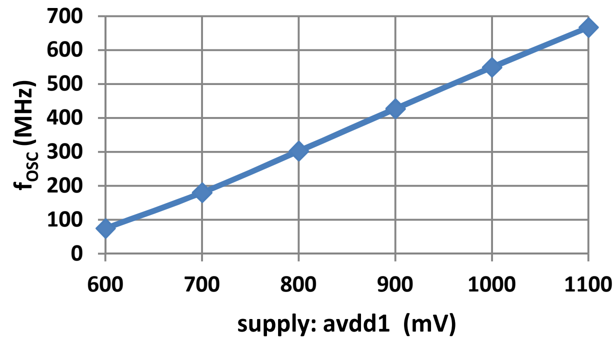
Figure 5.27 - Transient simulation (left) and phase noise analysis (right)



Source: the author

Figure 5.28 shows the oscillation frequency as a function of the ring supply voltage (avdd1). The oscillation frequency is practically linear with the supply voltage. At 500 mV, the ring does not oscillate.

Figure 5.28 - f_{OSC} as a function of VDD for 45-nm ring oscillator



Source: the author

Table 5.5 presents the performance parameters as a function of bulk bias for a supply voltage of 1.1 V. It is applied forward bulk bias simultaneously for the NMOS and PMOS devices. The value of $|V_{BS}|$ was zero, 125 mV, 250 mV and 300 mV. As can be seen, increasing $|V_{BS}|$, the threshold voltage decreases and F_{OSC} increases.

Table 5.5: Post-extracted performance parameters as a function of V_{BS} (mV)

V_{BULK_N} (mV)	V_{BULK_P} (mV)	V_{TH_P} (mV)	V_{TH_N} (mV)	f_{OSC} (MHz)	Voltage swing (mV)	P. noise at 5 kHz (dBc/Hz)	P. noise at 10 kHz (dBc/Hz)	P. noise at 100 kHz (dBc/Hz)
Zero	1100	417	-458	666.7	730	-3.3	-12.4	-42.8
125	975	393	-438	700.8	737	-2.9	-12.1	-42.4
250	850	366	-416	736.4	737	-2.6	-11.8	-42.1
350	750	343	-397	765.4	737	-2.4	-11.6	-41.8

Source: the author

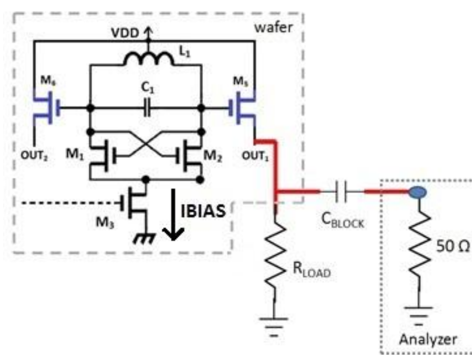
The simulated phase noise tends to get worse when applied the bulk bias due to the increase of the oscillation frequency. Higher the oscillation frequency, the worse is the phase noise, as described by (LEESON, 1996) and (HAJIMIRI, 1998). However, the forward bulk bias tends to decrease the flicker noise as discussed in section 3.3 and this reduction is not properly taken into account by traditional transistor flicker noise models (DA SILVA, 2008).

Therefore, one of the investigations of this Ph.D. thesis is the accuracy of traditional electrical simulators when simulating phase noise of circuits with bulk bias.

5.5.3 Cross-couple LC tank oscillator using 45 nm CMOS process

Figure 5.29 shows the test bench used in order to run the transient and phase noise simulations. A supply voltage of 1.1 V and I_{BIAS} = 5.5 mA were used.

Figure 5.29 - Test bench for transient and phase noise simulation



Source: the author

Table 5.6 shows the post-extracted performance parameters for OSC_{N1}, OSC_{N2}, OSC_{N3} and OSC_{P1} simulated using weak, nominal and strong models. The voltage swing were measured at the output of the source follower, and as a consequence, it is attenuated since the voltage gain of a source follower is lower than unity. Single ended voltage swings are around 100 mV and it can be properly measured by any spectrum analyzer. Phase noise were measured at five different offset frequencies away from the carrier: 0.5 kHz, 1 kHz, 5 kHz, 10 kHz and 100 kHz. The contribution of flicker noise for the phase noise decreases as the offset frequency increases (HAJIMIRI, 1998). At 0.5 kHz, the phase noise is dominated by the flicker noise contribution.

As one can see in table 5.6, the impact of fabrication process effects can result in a total frequency variation (Δf_{OSC}) of about 400 MHz. The major contribution of this frequency variation is the tolerance of capacitor C_1.

One can verify that the phase noise of OSC_{N1} (analog transistors) are better than OSC_{N3} (digital transistors), as for instance, a difference of 11 dBc at 0.5 kHz. Note that both circuits have the same power consumption, LC-tank and silicon area for the g_m-pair devices (table 5.1). The worse phase noise performance of OSC_{N3} is caused by the worse flicker noise of

digital transistors. Note also that as the offset frequency increases, phase noise difference between OSC_{N1} and OSC_{N3} reduces, and it becomes only ~ 1 dBc at 100 kHz of offset. This is also expected because at 100 kHz the flicker noise contribution decreases while the thermal noise contribution increases. The thermal noise of analog and digital transistors are expected to be similar.

Table 5.6: Post-extracted parameters for OSC_{N1}, OSC_{N2}, OSC_{N3} and OSC_{P1}

Models	f_{OSC} (GHz)	Voltage swing (mV)	P. noise at 0.5 kHz (dBc/Hz)	P. noise at 1 kHz (dBc/Hz)	P. noise at 5 kHz (dBc/Hz)	P. noise at 10 kHz (dBc/Hz)	P. noise at 100 kHz (dBc/Hz)
OSC_{N1}							
weak	2.375	70	-41.8	-50.3	-69.1	-76.5	-98.6
nominal	2.561	89	-41.7	-50.3	-69.4	-77	-99.5
strong	2.795	110	-42.7	-51.2	-70.1	-77.7	-100
OSC_{N2}							
nominal	2.557	n.a.	-35.8	-42.1	-56.4	-62.4	-82.4
OSC_{N3}							
weak	2.360	94	-30.50	-39.62	-60.74	-69.78	-98.03
nominal	2.541	110	-30.48	-39.6	-60.75	-69.8	-98.14
strong	2.767	129	-32	-41.12	-62.22	-71.22	-99.07
OSC_{P1}							
weak	2.245	88.1	-44.0	-53.2	-73.4	-81.3	-103.7
nominal	2.426	108	-47.8	-56.7	-76	-83.3	-104.7
strong	2.652	123.7	-47.1	-56.1	-75.5	-82.9	-104.3

Source: the author

Moreover, it is possible to verify that the PMOS version (OSC_{P1}) has better phase noise than the NMOS version (OSC_{N1}). At 500 Hz and 100 kHz of offset, the phase noise difference is 6.4 dBc and 5.2 dBc, respectively. The reasons for that (i) larger silicon area for g_m-pair devices (double), (ii) lower oscillation frequency and (iii) improved flicker noise performance of PMOS devices. The schematic of PMOS version also achieves better phase noise than the

schematic of NMOS version, and thus, the hypothesis that the different performance is solely caused by different parasitic resistances and capacitances in the layout can be excluded.

Finally, regarding the simulation using strong and weak models, one can verify that it does not significantly affect the phase noise performance (variation of ~1 dBc). Table 5.7 presents the simulated parameters as a function of bulk bias (applied only for the g_m-pair devices). The reduction of V_{TH} as a function of V_{BS} is also presented in table 5.7.

Table 5.7: Parameters as a function of V_{BULK} for OSC_{N1}, OSC_{N3} and OSC_{P1}

V_{BULK} (mV)	V_{BS} (mV)	V_{TH} (mV)	f_{OSC} (GHz)	Voltage swing at output (mV)	Voltage swing before buffer (mV)
			OSC_{N1}		
zero	-567	528	2.561	89	334
680	6	414	2.559	90.8	332
825	125	385	2.558	90.5	331
1000	264	349	2.557	89.3	327
			OSC_{N3}		
zero	-505	544	2.541	110	395
600	13	459	2.538	109.2	393
735	128	436	2.536	108.9	393
880	250	410	2.534	108.4	391
1000	350	387	2.532	107.8	389
			OSC_{P1}		
1100	601	-443	2.427	110.4	427
400	-28	-370	2.422	103.2	398
260	-152	-352	2.421	100.9	388
150	-249	-337	2.419	99	379
50	-336	-323	2.418	95	370

Source: the author

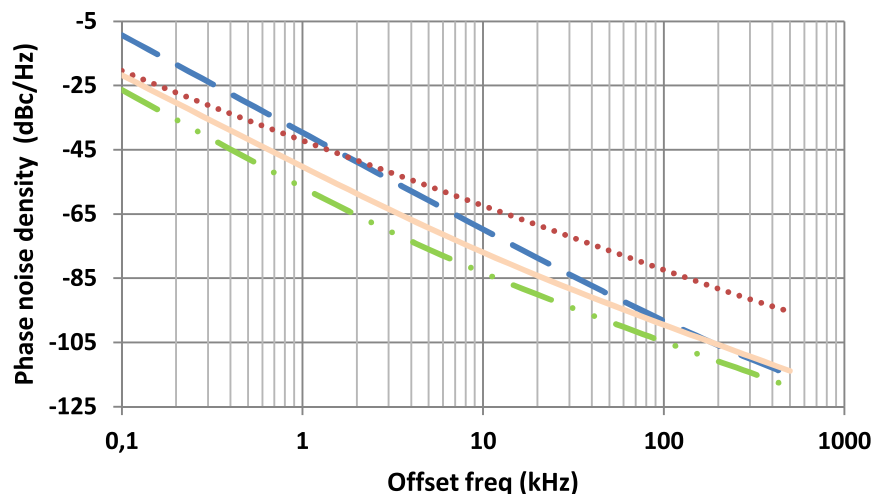
Since the oscillation frequency depends mainly on capacitor C_1 and inductor L_1, f_{OSC} is not significantly affected when bulk bias is applied. Considering a variation of 1 V in the bulk bias voltage, the oscillation frequency varies only ~ 9 MHz or 0.3%. The output voltage swing is not affected by bulk bias as well. The last column of table 5.5 shows the single ended voltage swing at the input of the source follower (before the attenuation).

Table 5.8 presents the phase noise performance as function of the bulk bias. As one can see, there is a significant improvement in the phase noise when the bulk bias is applied. This is especially true for low offset frequencies (close-in phase noise) where the flicker noise performance is more relevant. As for instance, for OSC_{N3}, its phase noise at 0.5 kHz had an improvement of about 4 dB when the bulk voltage is changed to 680 mV.

The first reason for the above improvement is probably the slightly reduction in f_{OSC} (LEESON, 1996). The second reason is probably the g_m reduction due to V_{TH} reduction. Note that flicker noise current depends g_m (RAZAVI, 2001). However, we expect an even better phase noise improvement when bulk bias is employed because the simulator does not take into account the flicker noise reduction caused by the bulk bias.

Figure 5.30 shows the phase noise for OSC_{N1}, OSC_{N2} and OSC_{N3} and OSC_{P1}. Neglecting OSC_{N2}, one can see that the phase noise of OSC_{N1}, OSC_{N3} and $OSCP_1$ at offset frequencies above 500 kHz tends to become approximately equal. Oscillator OSC_{N2} has the lowest area and g_m.

Figure 5.30- Phase noise of OSC_{N1} (line), OSC_{N2} (dots), OSC_{N3} (broken line) and OSC_{P1} (line plus two points)



Source: the author

Table 5.8: Phase noise as function of V_{BULK} for OSC_{N1}, OSC_{N3} and OSC_{P1}

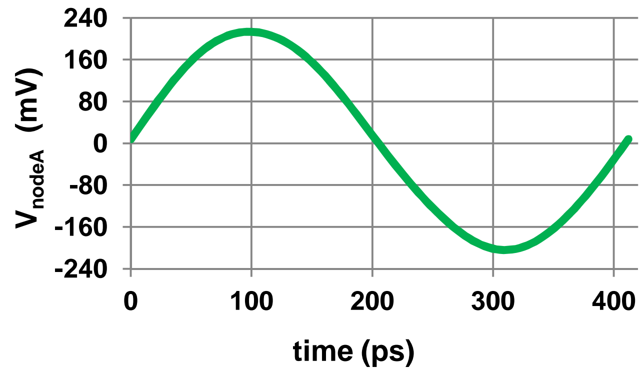
V_{BULK} (mV)	P. noise at 0.5 kHz (dBc/Hz)	P. noise at 1 kHz (dBc/Hz)	P. noise at 5 kHz (dBc/Hz)	P. noise at 10 kHz (dBc/Hz)	P. noise at 100 kHz (dBc/Hz)
OSC_{N1}					
zero	-41.7	-50.3	-69.4	-77.0	-99.5
680	-44.7	-53.0	-71.2	-78.3	-99.8
825	-45.7	-53.9	-71.7	-78.7	-99.8
1000	-47.3	-55.3	-72.3	-78.9	-99.6
OSC_{N3}					
zero	-30.5	-39.6	-60.8	-69.8	-98.1
680	-34.2	-43.3	-64.2	-73.0	-99.8
825	-35.8	-44.8	-65.6	-74.3	-100.3
1000	-38.1	-47.1	-67.6	-76.1	-100.8
OSC_{P1}					
zero	-48.4	-57.3	-76.4	-83.7	-104.9
680	-50.8	-59.3	-77	-83.7	-104.3
825	-50.8	-59.3	-76.8	-83.5	-104.1
1000	-50.6	-59.1	-76.6	-83.3	-103.8

Source: the author

Figure 5.31 and Figure 5.32 show the transient simulation of the input voltage of the source follower and the output voltage for OSC_{P1}, respectively. The peak to peak voltage amplitude at the input and output of the source follower are 427 mV and 110 mV, respectively.

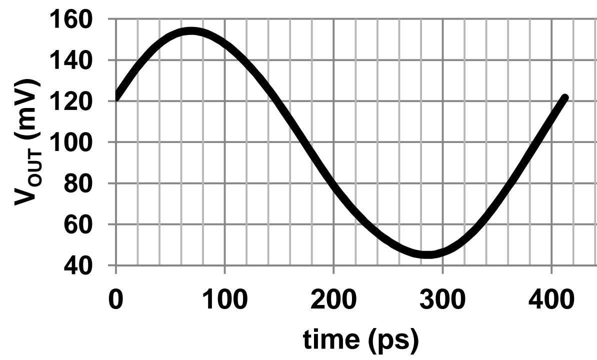
Figure 5.33 and Figure 5.34 show the transient simulation of the input voltage of the source follower and the output voltage for OSC_{N3}, respectively. The peak to peak voltage amplitude at the input and output of the source follower are 395 mV and 110 mV, respectively.

Figure 5.31 - Voltage at the input of source follower OSC_{P1} (transient analysis)



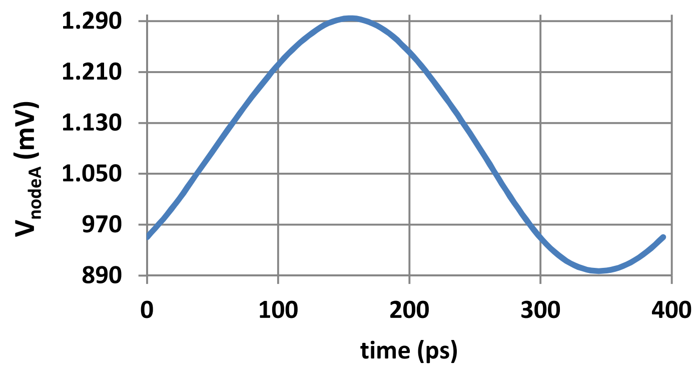
Source: the author

Figure 5.32 - Output voltage of OSC_{P1} (transient analysis)



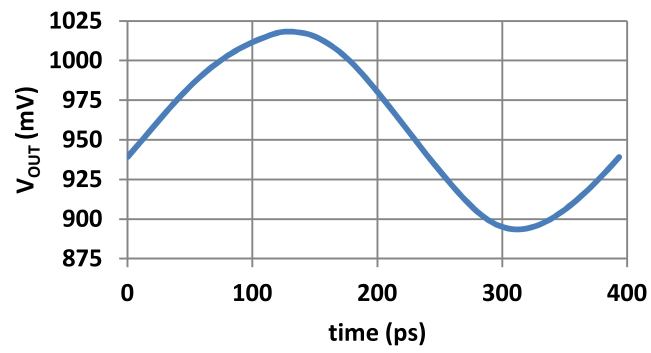
Source: the author

Figure 5.33 - Voltage at the input of source follower for OSC_{N3} (transient analysis)



Source: the author

Figure 5.34 - Output voltage of OSC_{N3} (transient analysis)



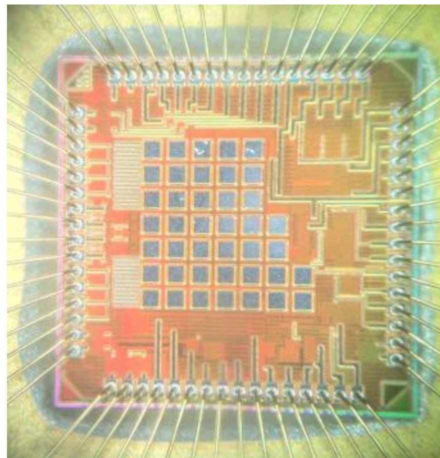
Source: the author

6 SILICON MEASUREMENT - VOLTAGE REFERENCES

6.1 Measurement setup for temp. and VDD dependency characterization

The integrated circuit presented in chapter 4 and shown in figure 4.29 was fabricated through MOSIS silicon brokerage service (https://www.mosis.com/). Figure 6.1 shows a micrograph of the fabricated chip.

Figure 6.1 - Micrograph of chip



Source: the author

In order to perform the characterization of the fabricated samples, a test board shown in figure 6.2 was designed and 10 IC samples were mounted on the test boards. Through the test board, it was possible to measure all voltage references and the ring-oscillator implemented in the 130 nm CMOS process.

All voltage references are connected to discrete output buffers in order to provide its isolation from the measurement equipment. The employed buffer OP4177 presents a low offset voltage lower than 60 μV (ANALOG, 2015) that does not degrade the precise characterization of V_{REF}.

The first measurement was performed to characterize the impact of supply voltage on V_{REF} . By means of the Agilent 4156 semiconductor analyzer, the chip power supply was swept from 0 to 1.2 V (for V_{REF_1} to V_{REF_6}) or 0 to 2.5 (for V_{REF_7} and V_{REF_8}) while the output voltages were recorded.

The second measurement was performed to characterize the impact of temperature on V_{REF} . Still using the semiconductor analyzer to generate the supply voltage and provide the monitoring of V_{REF}, a test chamber was employed to set the temperature of the chip from - 40 to 120 °C. All voltage references of this work were optimized to have the curvature inflection point at approximately 22 °C.

Figure 6.2 - Test board

Source: the author

6.2 I_{REF}: PTAT Current Reference

Ten samples of the PTAT current reference were measured and the values of I_{REF} at 20°C are shown in table 6.1 and figure 6.3. As can be seen in figure 6.3, the average value of I_{REF} at 20°C obtained through Monte Carlo analysis is 497 nA and its difference from the maximum and minimum measured samples (V_{REF_SIM} - V_{REF_MAX}/V_{REF_MIN}) are 120 nA and -46 nA, respectively.

The standard deviation of I_{REF} at 20°C obtained from a Monte Carlo analysis is 53.4 nA. Verifying the measured samples, one can verify that 9 of 10 samples fit within an interval of ± 2 sigma of the Gaussian distribution. Only sample nº 8 fits within an interval of ±3 sigma.

The second parameter show in table 6.1 is the variation of I_{REF} in the temperature range of - 40 to 80 °C (ΔI_{REF_TEMP} = I_{REF} (80 °C) - I_{REF} (-40 °C)). In addition, figure 6.4 shows the temperature behavior for the 10 samples (lines) and the simulation result (dots) in an extended temperature range of -40 to 120 °C.

Considering the reduced temperature range of -40 to 80 ºC, the average value of ΔI_{REF_TEMP} is 323 nA, what represents an average TC of 5188 ppm/°C. Comparing ΔI_{REF_TEMP} of all samples (last line of table 6.1) and its typical simulated value (314 nA), one can verify that the largest difference between silicon and simulation result is lower than 14% (sample 5).

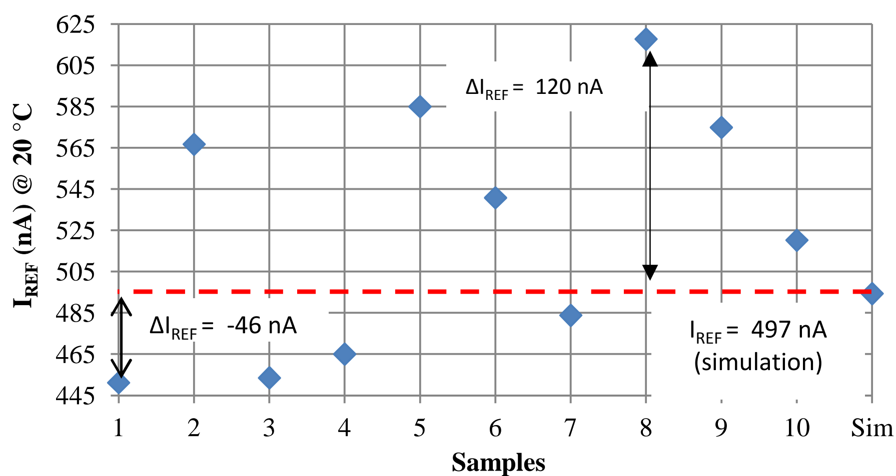
Table 6.1: I_{REF} (nA) at 20°C and I_{REF_TEMP} (nA) for 10 measured samples

Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6	Sample 7	Sample 8	Sample 9	Sample 10
I_{REF} (nA) at 20 °C									
451.2	566.7	453.5	465.1	585.0	540.8	483.8	617.7	574.9	520.3
I_{REF_TEMP} (nA): from - 40 to 80 °C									
292.5	324.7	337.5	343.6	272.0	329.8	347.5	313.9	344.5	323.0

Source: the author

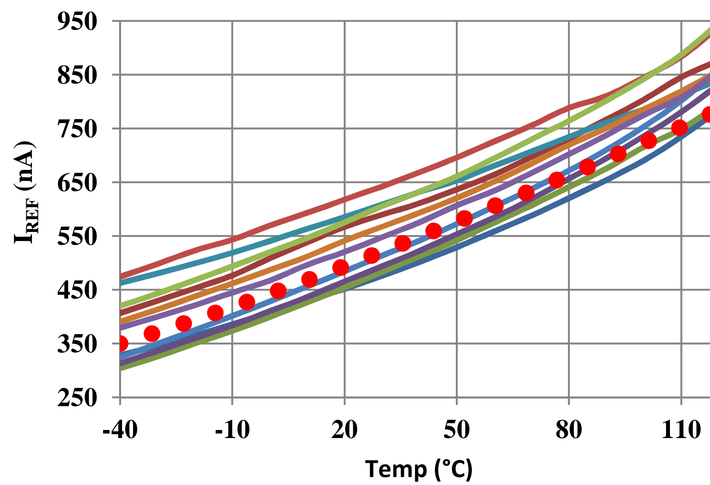
Moreover, the standard deviation of ΔI_{REF_TEMP} obtained from MC analysis is 28.6 nA and thus, 9 from 10 samples fit within an interval of ± 2 sigma of the Gaussian distribution (only sample #5 fits within an interval of +3 sigma).Therefore, either I_{REF} (at 20ºC) as ΔI_{REF_TEMP} were properly estimated by the Monte Carlo analysis.

Figure 6.3 - I_{REF} at 20 °C for 10 samples



Source: the author

Figure 6.4 - I_{REF} vs temp for 10 samples (lines) and simulation (dotted)

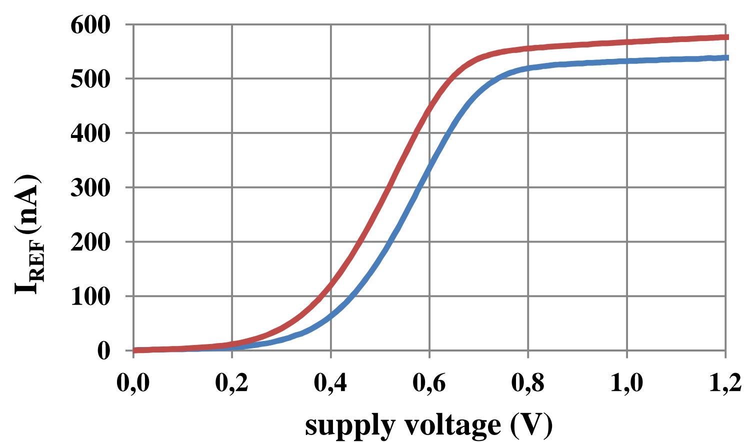


Source: the author

In addition, if a larger temperature range of -40 to 120 ºC is considered, the average values of ΔI_{REF_TEMP} and TC are then equal to 456 nA and 5773 ppm/°C, respectively.

Figure 6.5 shows I_{REF} as a function of supply voltage for two samples. As can be seen, the current reference works for a supply voltage larger than 800 mV. Regarding the supply sensitivity, I_{REF} varies roughly 38 nA/V.

Figure 6.5 - I_{REF} vs supply voltage for 2 measured samples



Source: the author

Table 6.2 summaries all measured performance parameter of the I_{REF} circuit. It shows the average, maximum and minimum values of I_{REF} at 20 ºC and ΔI_{REF_TEMP}. Moreover, it also shows the average value of TC calculated using equation 4.30. Although very few samples were measured, we can consider that operation of I_{REF} was correctly estimated by the Monte Carlo analysis. This result is important because references V_{REF_3}, V_{REF_4}, V_{REF_5}, V_{REF_7} and V_{REF_8} employ this current reference circuit to generate their output voltages.

Table 6.2: Summary of measured performance for 10 samples of I_{REF}

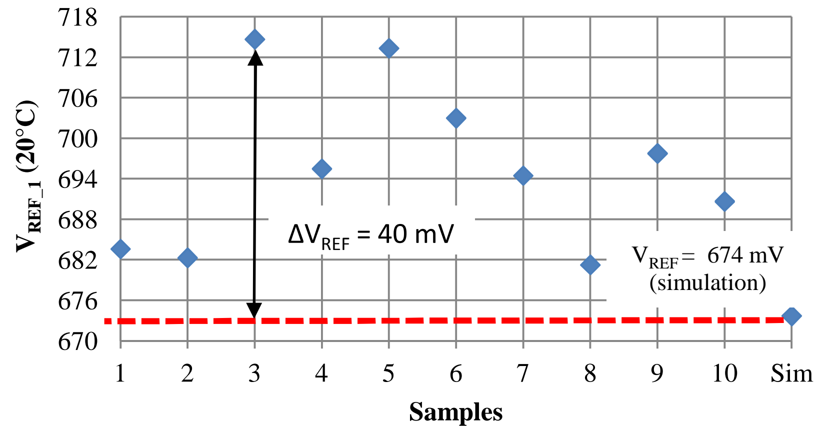
I_{REF} (nA) at room temperature: 20 °C					
MC mean I_{REF} (nA)	**MC sigma I_{REF} (nA)**	**average I_{REF} (nA)**	**max I_{REF} (nA)**	**min I_{REF} (nA)**	**VDD sensitivity (nA/V)**
497	53.4	525.9	617.7	451.2	38
***I_{REF_TEMP} (nA)* for the reduced temperature range: -40 to 80 °C**					
MC mean *I_{REF_TEMP} (nA)*	**MC sigma *I_{REF_TEMP} (nA)***	***average I_{REF_TEMP} (nA)***	***max I_{REF_TEMP} (nA)***	***min I_{REF_TEMP} (nA)***	**average TC (ppm/°C)**
315.7	28.6	323	348	272	5188
***I_{REF_TEMP} (nA)* for the extended temperature range: -40 to 120 °C**					
MC mean *I_{REF_TEMP} (nA)*	**MC sigma *I_{REF_TEMP} (nA)***	***average I_{REF_TEMP} (nA)***	***max I_{REF_TEMP} (nA)***	***min I_{REF_TEMP} (nA)***	**average TC (ppm/°C)**
434.9	39.7	478	531	377	5773

Source: the author

6.3 V_{REF_1}: Bandgap-based reference

The values of V_{REF} (mV) at 20°C and ΔV_{REF_TEMP} (mV) in the temperature range of - 40 to 80 °C for 10 measured samples are shown in table 6.3 and figure 6.6. As can be seen in figure 6.6, all samples have V_{REF} larger than the simulated results and a maximum difference of 40 mV (sample 3) between silicon and the mean value of V_{REF} at 20 °C (obtained from MC analysis) was observed.

Figure 6.6 - V_{REF_1} at 20°C for ten samples



Source: the author

From Chapter 4, the sigma of V_{REF} (mV) at ~ 20°C is 16 mV. Therefore, 8 from 10 samples fit within an interval of ± 2 sigma of the Gaussian distribution. Samples 3 and 5 fit within an interval of ± 3 sigma.

Figure 6.7 shows V_{REF_1} as a function of supply voltage and as one can see, all samples work for a supply voltage larger than 1 V. Regarding the supply voltage sensitivity, an average variation of 12 mV/V was measured.

Figure 6.8 shows V_{REF_1} as a function of temperature. Considering the temperature range of - 40 to 80 °C, the smallest and largest values of ΔV_{REF_TEMP} are 3.3 mV and 16.5 mV, what means a temperature coefficient of 40 and 160 ppm/°C, respectively. The average of ΔV_{REF_TEMP} and TC are 9 mV and 107 ppm/°C, respectively.

Table 6.3: V_{REF_1} (mV) at 20°C and V_{REF_TEMP} (mV) for 10 measured samples

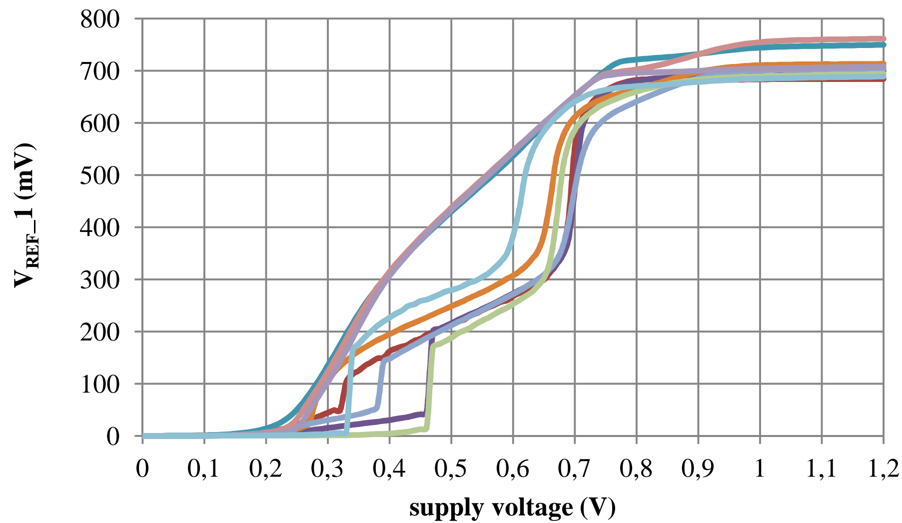
Sample 1	**Sample 2**	**Sample 3**	**Sample 4**	**Sample 5**	**Sample 6**	**Sample 7**	**Sample 8**	**Sample 9**	**Sample 10**
V_{REF} (mV) at 20 °C									
683.6	682.3	714.7	695.5	713.3	703.0	694.5	681.3	697.8	690.7
V_{REF_TEMP} (mV): from - 40 to 80 °C									
7	7.6	9.0	16.5	5.0	3.3	3.5	14.8	8.4	14.3

Source: the author

Regarding the MC analysis, the mean and of ΔV_{REF_TEMP} for the above temp. range is approximately 10.7 mV and 8 mV. Therefore, for our set of samples, there is a good agreement between simulation and silicon; either for V_{REF_1} (20 ° C) as ΔV_{REF_TEMP}.

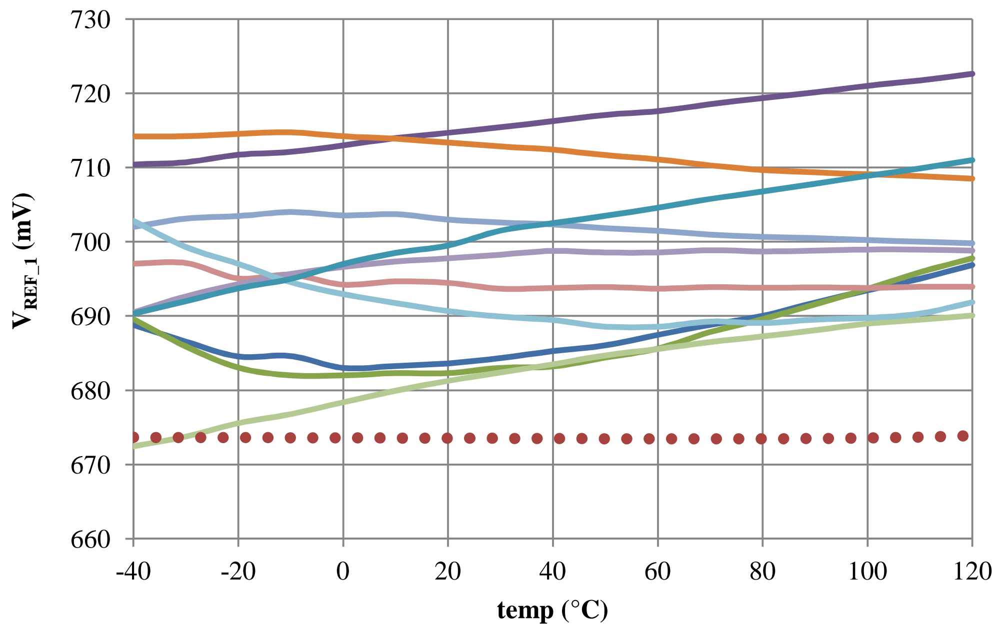
Table 6.4 summaries all measurement data for V_{REF_1}. For the temperature range of -40 to 120 °C, the average TC is 100 ppm/°C.

Figure 6.7 - Measured V_{REF_1} vs supply voltage



Source: the author

Figure 6.8 - V_{REF_1} vs temp. for 10 measured samples (lines) and simulation (dots)



Source: the author

Table 6.4: Summary of measured performance for 10 samples of V_{REF_1}

at room temperature: 20 °C					
MC mean V_{REF} (mV)	**MC sigma V_{REF} (mV)**	**average V_{REF} (mV)**	**max V_{REF} (mV)**	**min V_{REF} (mV)**	**VDD sensitivity (mV/V)**
674	16.1	695.6	714.7	681.3	12
Reduced temperature range: -40 to 80 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
10.7	8	9	16.5	3.3	107
Extended temperature range: -40 to 120 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
29.3	23.4	11	19.6	3.5	100

Source: the author

6.4 V_{REF_2}: Bandgap-based reference using PMOS diode

The values of V_{REF_2} (mV) at 20°C and ΔV_{REF_TEMP} (mV) in the temperature range of - 40 to 80 °C for 9 measured samples are shown in table 6.5 and figure 6.9. As can be seen in figure 6.9, the maximum difference between the measured samples and the simulated mean value of V_{REF_2} is 31 mV.

From the MC analysis shown in Chapter 4, the sigma of V_{REF_2} (mV) at ~ 20°C is 16 mV. The most part of samples fit within an interval of ± 1 sigma of the Gaussian distribution. Only two samples fit within an interval of ± 2 sigma.

Figure 6.10 shows V_{REF_2} as a function of VDD. All samples work for a VDD > 1 V. Regarding the VDD sensitivity, an average variation of 18 mV/V was achieved.

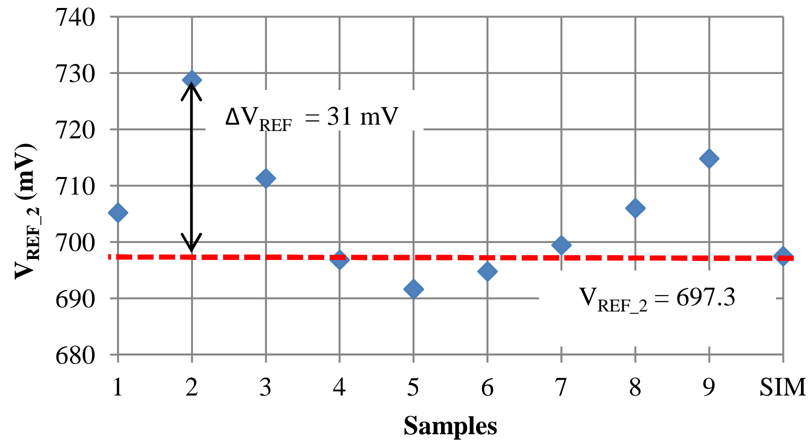
Figure 6.11 shows V_{REF_2} as a function of temperature. Considering the temperature range of -40 to 80 °C, the mean of ΔV_{REF_TEMP} is 9 mV what means TC equal to 107 ppm/ºC - temperature performance predicted by the Monte Carlo analysis.

Table 6.5: V_{REF_2} (mV) at 20°C and V_{REF_TEMP} (mV) for 9 measured samples

Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6	Sample 7	Sample 8	Sample 9
V_{REF} (mV) at 20 °C								
705.2	728.8	711.3	696.8	691.6	694.8	699.5	706.0	714.8
V_{REF_TEMP} (mV): from - 40 to 80 °C								
7	7.6	9.0	16.5	5.0	3.3	3.5	14.8	8.4

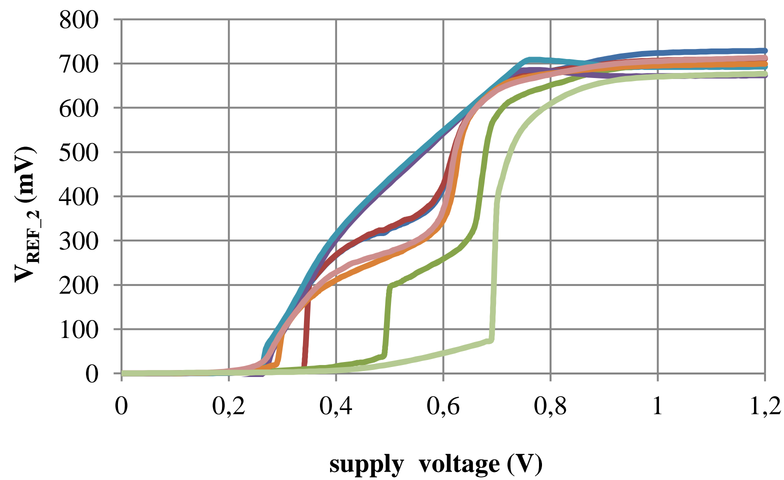
Source: the author

Figure 6.9 - Measured V_{REF_2} at 20°C for 9 samples



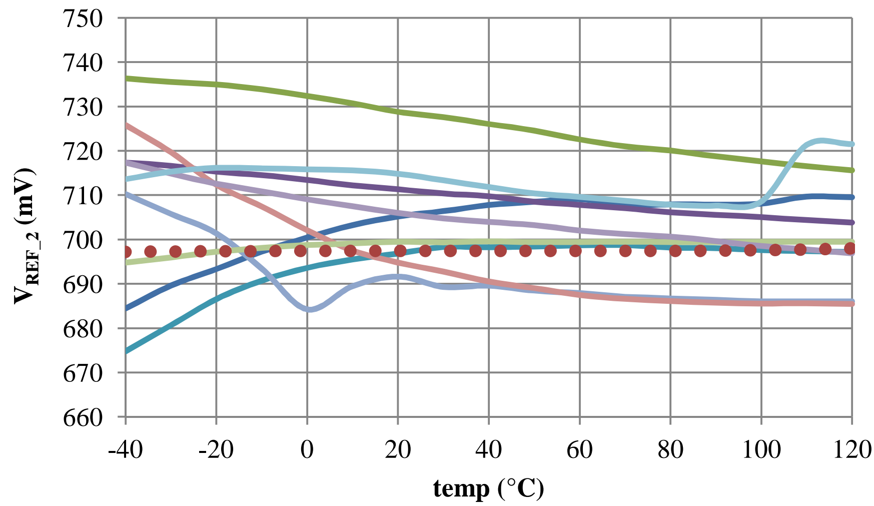
Source: the author

Figure 6.10 - Measured V_{REF_2} vs supply voltage



Source: the author

Figure 6.11 - V_{REF_2} vs temp. for 9 measured samples (lines) and simulation (dots)



Source: the author

Table 6.6 summaries all measurement data for V_{REF_2}.

Table 6.6: Summary of measured performance for 9 samples of V_{REF_2}

at room temperature: 20 °C					
MC mean V_{REF} (mV)	**MC sigma V_{REF} (mV)**	**average V_{REF} (mV)**	**max V_{REF} (mV)**	**min V_{REF} (mV)**	**VDD sensitivity (mV/V)**
697.3	16.1	705.4	728.8	691.6	18
Reduced temperature range: -40 to 80 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
10.8	8.2	19	39.7	4.8	226
Extended temperature range: -40 to 120 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
30	23.5	21	40.4	4.8	187

Source: the author

6.5 V_{REF_3}: Simple V_{TH0}-based reference

The values of V_{REF} (mV) at 20°C and ΔV_{REF_TEMP} (mV) in the temperature range of - 40 to 80 °C for 10 measured samples are shown in table 6.7 and figure 6.12. As can be seen in figure 6.12, the maximum difference between the measured samples and the nominal value of V_{REF_3} is 25.1 mV.

From the Monte Carlo analysis shown in Chapter 4, the sigma of V_{REF_3} (mV) at ~ 20°C is 15.4 mV. All samples fit within an interval of ± 2 sigma of the Gaussian distribution.

Table 6.7: V_{REF_3} (mV) at 20°C and V_{REF_TEMP} (mV) for 10 measured samples

Sample 1	**Sample 2**	**Sample 3**	**Sample 4**	**Sample 5**	**Sample 6**	**Sample 7**	**Sample 8**	**Sample 9**	**Sample 10**
V_{REF} (mV) at 20 °C									
306.7	311.5	301.9	311.8	291.9	301.1	299	307.4	297.0	294.2
V_{REF_TEMP} (mV): from - 40 to 80 °C									
15.2	18.1	12.1	18.6	13.0	11.2	17.7	15.4	8.7	16.2

Source: the author

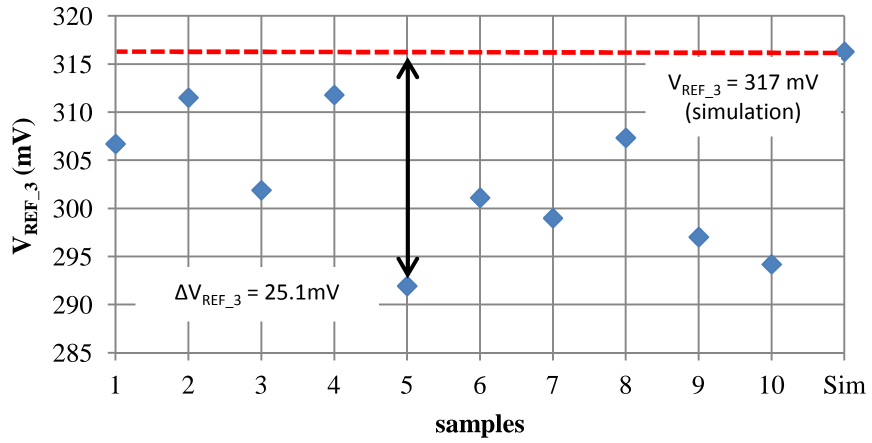
Figure 6.13 shows V_{REF_3} as a function of supply voltage and as can be seen, all samples work for a supply voltage larger than 0.8 V. Regarding the supply voltage sensitivity, an average variation of 6 mV/V was achieved.

Figure 6.14 shows V_{REF_3} as a function of temperature. Considering the reduced temperature range of -40 to 80 °C, the average TC and ΔV_{REF_TEMP} are 412 ppm/ºC and 14.6 mV, respectively.

From Monte Carlo analysis, the mean and sigma value of ΔV_{REF_TEMP} is 7.7 mV and 1.4 mV, respectively. Furthermore, the worst value of ΔV_{REF_TEMP} predicted by MC analysis is 14.9 mV. Since the MC predictions does not account for voltage shifted caused by the packaging process (FRUETT, 2003), (ABESINGHA, 2002) and (GUPTA, 2005), we can consider that there is a reasonable agreement of silicon and simulation results regarding the temperature behavior of V_{REF_3}.

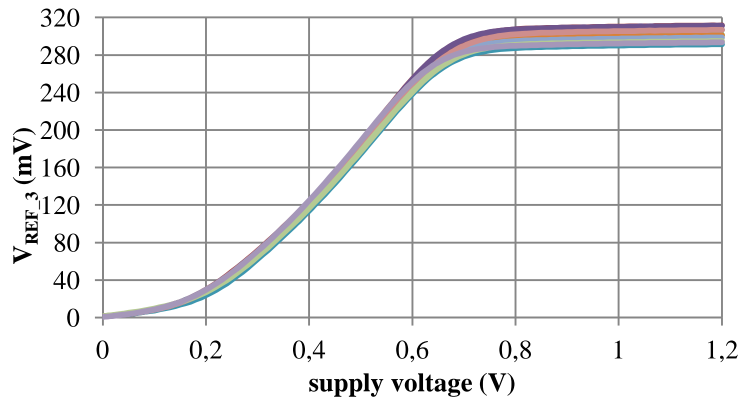
Table 6.8 summarizes all measurement data for V_{REF_3}.

Figure 6.12 - V_{REF_3} at 20°C for 10 samples



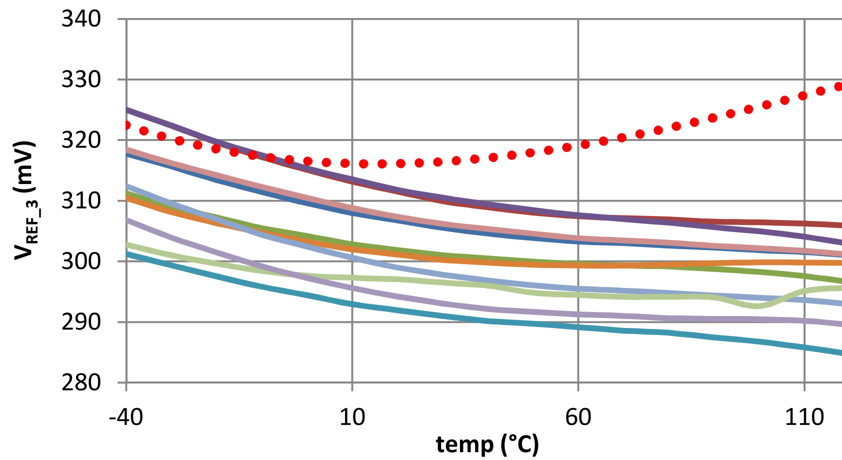
Source: the author

Figure 6.13 - Measured V_{REF_3} vs supply voltage for 10 samples



source: the author

Figure 6.14 - V_{REF_3} vs temp. for 10 measured samples (lines) and simulation (dots)



source: the author

Table 6.8: Summary of measured performance for 10 samples of V_{REF_3}

at room temperature: 20 °C					
MC mean V_{REF} (mV)	**MC sigma V_{REF} (mV)**	**average V_{REF} (mV)**	**max V_{REF} (mV)**	**min V_{REF} (mV)**	**VDD sensitivity (mV/V)**
317	15.4	302.3	311.8	291.9	6
Reduced temperature range: -40 to 80 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
7.7	1.4	14.6	18.6	8.7	402
Extended temperature range: -40 to 120 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
13.5	3.4	16.6	22.1	10.2	340

source: the author

6.6 V_{REF_4}: Alternative V_{TH0}-based reference

As explained in Chapter 4, V_{REF_4} generates the output voltage based on a balanced sum of two voltages with opposite TC. The voltage with positive TC (V_{PTAT}) is proportional to the thermal voltage and it is generated by the difference of two gate-source voltages (equation 4.7). The voltage with negative TC (V_{CTAT}) is proportional to the gate-source voltage of a NMOS transistor. Verifying figure 4.10, V_{PTAT} and V_{CTAT} voltages are at the source terminal of N_4 and the gate terminal of N_6, respectively.

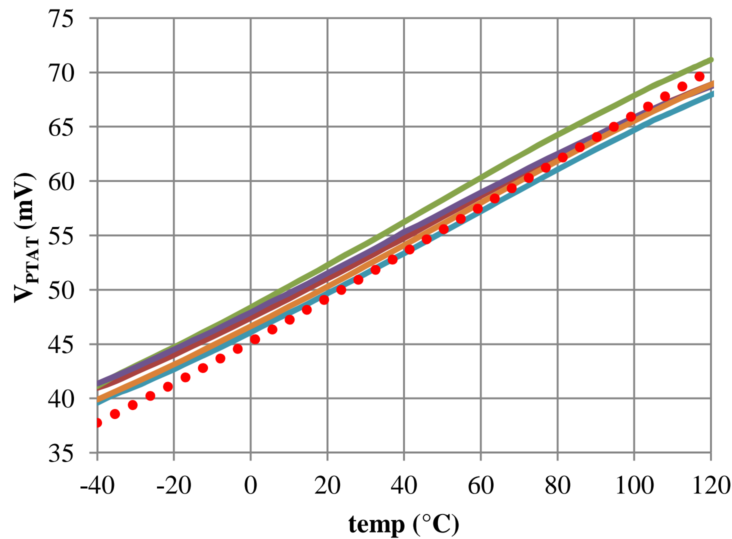
Table 6.9 shows the measured V_{PTAT} and V_{CTAT} (mV) and its temperature variation (V_{PTAT_TEMP} and V_{CTAT_TEMP}) in the temp. range of -40 to 80 °C for 5 samples. V_{PTAT} and V_{CTAT} as a function of temperature can be seen in figures 6.15 and 6.16, respectively.

Table 6.9: Measured V_{PTAT}, V_{CTAT} (mV) at 20 °C, and V_{TEMP} (-40 to 80 °C)

	sample 1	sample 2	sample 3	sample 4	sample 5	average	simulation
V_{PTAT} (mV)	51.0	52.3	51.5	49.7	50.3	51	49.3
V_{PTAT_TEMP} (mV)	21.4	23.1	21.1	21.5	22	21.8	24.1
V_{CTAT} (mV)	109.5	114.4	108.3	112.0	114.3	109.5	122.7
V_{CTAT_TEMP} (mV)	102.7	96.7	99.2	104.2	102.3	101	97.9

source: the author

Figure 6.15 - V_{PTAT} vs temp. for 5 measured samples (lines) and simulation (dots)



source: the author

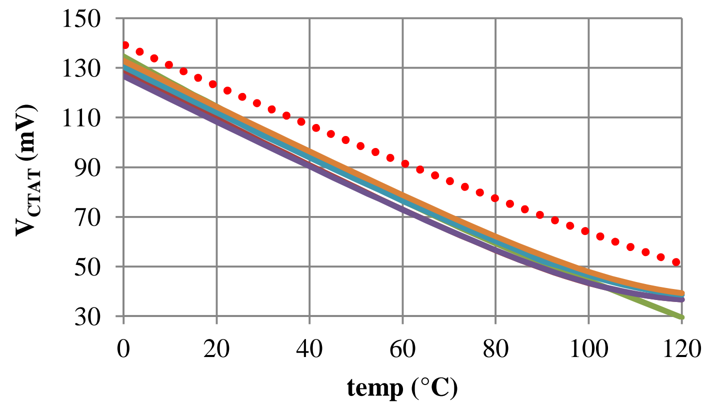
A good agreement between the simulation and silicon results was verified for V_{CTAT} and V_{PTAT}. It is an important result since these voltages are used in the design of several temperature-compensated voltage references.

Regarding V_{CTAT}, one can see that there is a negative shift between measured samples and the simulated result. It happens because the threshold voltage of the fabricated N_6 transistor (figure 4.10) is probably lower than the typical simulated one.

One can observe that for temperature above the room temperature (20 °C), V_{PTAT} is slightly closer to the simulation results and the slope of V_{CTAT} is slightly lower. It happens because for temperatures lower than 20 °C there was not very precise control of the temperature chip (few degrees of uncertainty). For this experiment, thermostream system

(http://www.temptronic.com/) was used to set the chip temperature instead of the temperature chamber. Posteriorly was verified that part of the cold air was escaping during the measurement and thus the chip was not achieving the exact desired temperature.

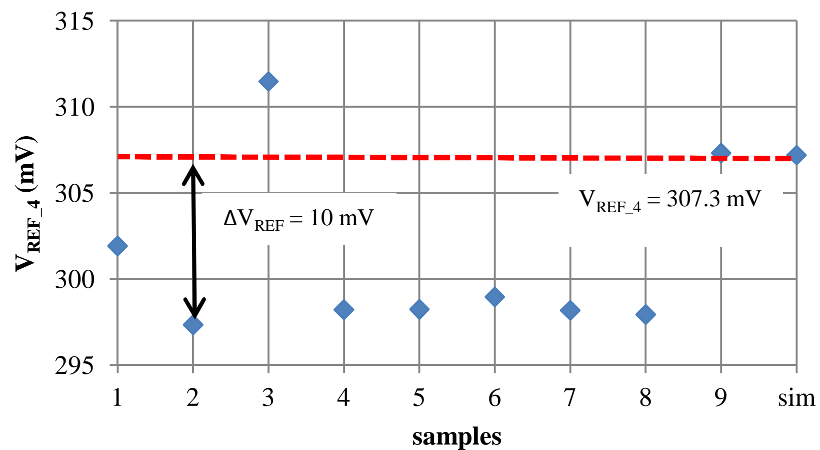
Figure 6.16 - V_{CTAT} vs temp. for 5 measured samples (lines) and simulation (dots)



source: the author

Regarding the V_{REF_4} circuit, its output voltage at 20°C and ΔV_{REF_TEMP} (mV) in the temperature range of - 40 to 80 °C for 9 measured samples are shown in table 6.10 and figure 6.17. Figure 6.17 shows that the maximum difference between the measured samples and the nominal simulated V_{REF_3} is 10 mV.

Figure 6.17- Measured V_{REF_4} at 20°C for 9 samples



Source: the author

Table 6.10: V_{REF_4} (mV) at 20°C and V_{REF_TEMP} (mV) for 9 measured samples

Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6	Sample 7	Sample 8	Sample 9
V_{REF} (mV) at 20 °C								
301.9	297.3	311.5	298.2	298.2	299.0	298.2	297.9	307.3
V_{REF_TEMP} (mV): from - 40 to 80 °C								
10.1	3.2	12.9	13.3	14.8	10.5	11.0	10.8	15.2

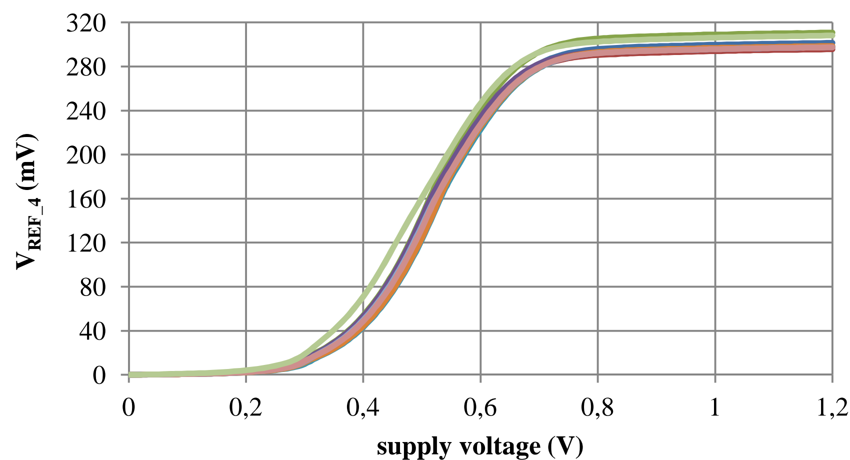
Source: the author

From the Monte Carlo analysis shown in Chapter 4, the sigma of V_{REF_4} (mV) at ~ 20°C is 14.5 mV. All samples fit within an interval of ± 1 sigma of the Gaussian distribution what represents a great agreement between silicon and simulation.

For the most part of samples, V_{REF_4} is lower than the simulated value. Since the output voltage of this type of circuit is proportional to the transistor threshold voltage, this result also suggests that the value of V_{TH} of N_6 is lower than the typical simulated one.

Figure 6.18 shows V_{REF_4} as a function of supply voltage and as can be seen, all samples work for a supply voltage larger than 0.8 V. Regarding the supply voltage sensitivity, an average variation of 7.3 mV/V was observed.

Figure 6.18 - Measured V_{REF_4} vs supply voltage for 9 samples

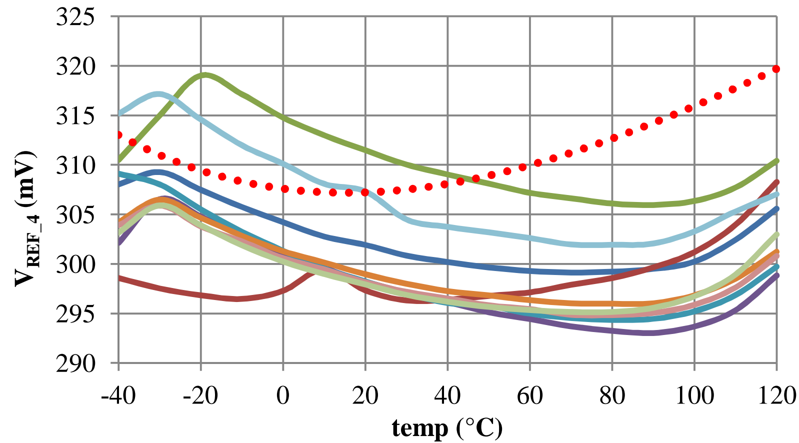


Source: the author

Figure 6.19 shows V_{REF_4} as a function of temperature. Considering the reduced temperature range of -40 to 80 °C, the average TC is 313 ppm/ºC. It means an average value of ΔV_{REF_TEMP} equal to 11.3 mV. The mean and sigma values of ΔV_{REF_TEMP} predicted by

Monte Carlo simulation are 7.2 mV and 1.4 mV, respectively. Thus, one can consider that there is reasonable agreement between silicon and simulation results. Finally, table 6.7 summarizes all measurement data for V_{REF_4}

Figure 6.19 - V_{REF_4} vs temp. for 9 measured samples (lines) and simulation (dots)



Source: the author

Table 6.11: Summary of measured performance for 9 samples of V_{REF_4}

at room temperature: 20 °C					
MC mean V_{REF} (mV)	**MC sigma V_{REF} (mV)**	**average V_{REF} (mV)**	**max V_{REF} (mV)**	**min V_{REF} (mV)**	**VDD sensitivity (mV/V)**
307.8	14.5	301.1	311.5	297.3	7.3
Reduced temperature range: -40 to 80 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
7.2	1.4	11.3	15.2	3.16	313
Extended temperature range: -40 to 120 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
13.7	3.2	12.3	15.2	10.1	256

Source: the author

6.7 V_{REF_5}: V_{TH0}-based reference using composite transistors

The values of V_{REF} (mV) at 20°C and ΔV_{REF_TEMP} (mV) in the temp. range of - 40 to 80 °C for 10 measured samples are shown in table 6.12 and figure 6.20. As can be seen in figure 6.20, the maximum difference between the measured samples and the nominal V_{REF_5} is 53.8 mV.

From the MC analysis shown in Chapter 4, the sigma of V_{REF_5} (mV) at 20°C is 28.7 mV. All samples fit within an interval of ± 2 sigma of the Gaussian distribution.

Figure 6.19 shows V_{REF_5} as a function of supply voltage and as one can see, all samples work for a supply voltage larger than 0.8 V. Regarding the supply voltage sensitivity, an average variation of 2.7 mV/V was observed.

Figure 6.22 shows V_{REF_5} as a function of temperature. Considering the reduced temperature range of -40 to 80 °C, the average TC is 396 ppm/ºC while the average ΔV_{REF_TEMP} is 41.6 mV. The mean and sigma values of ΔV_{REF_TEMP} predicted by the MC analysis are equal to 4.6 mV and 2.6 mV, respectively.

Comparing silicon and simulation results, it is possible to verify that the temperature performance of the fabricated samples was not properly predicted by the Monte Carlo and corners simulations. It is an interesting result since the value of V_{REF_5} at 20 °C was properly estimated by the simulations (the discrepancy is only related to the temperature behavior).

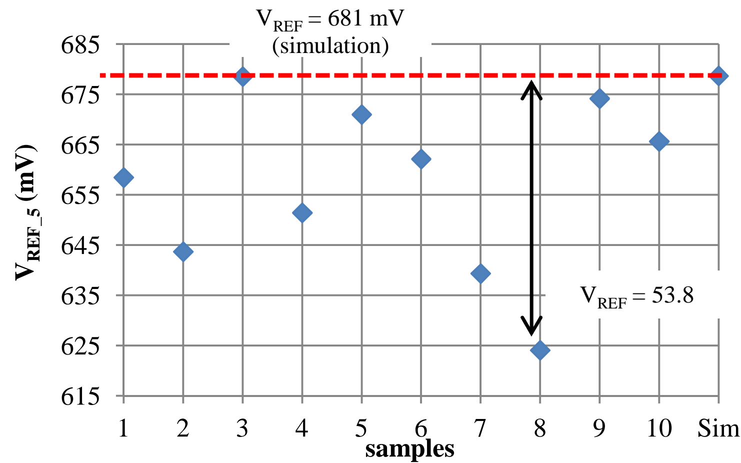
Although there is not an enough number of samples in order to make possible the development of statistical-based statements, one can clearly verify that all samples have PTAT behavior.

Table 6.12: V_{REF_5} (mV) at 20°C and V_{REF_TEMP} (mV) for 10 measured samples

Sample 1	**Sample 2**	**Sample 3**	**Sample 4**	**Sample 5**	**Sample 6**	**Sample 7**	**Sample 8**	**Sample 9**	**Sample 10**
V_{REF} (mV) at 20 °C									
658.5	643.7	678.6	651.5	671.0	662.2	639.4	624.1	674.2	665.7
V_{REF_TEMP} (mV): from - 40 to 80 °C									
37.5	36.3	38.8	38.9	35.2	33.8	44.8	45.2	50.5	55.3

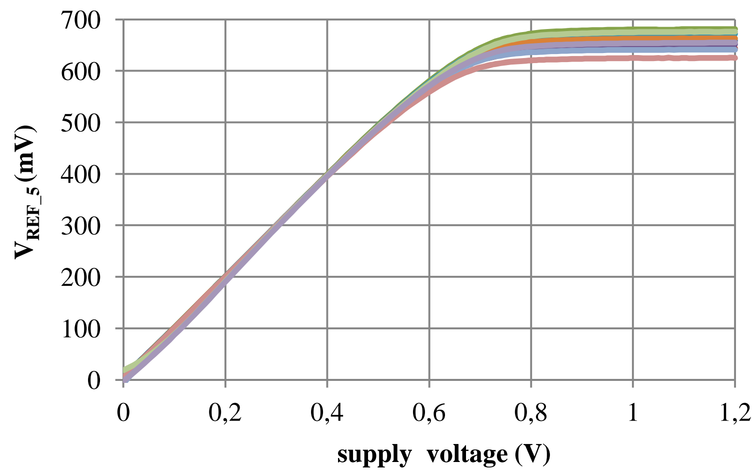
Source: the author

Figure 6.20 - V_{REF_5} at 20°C for 10 samples



Source: the author

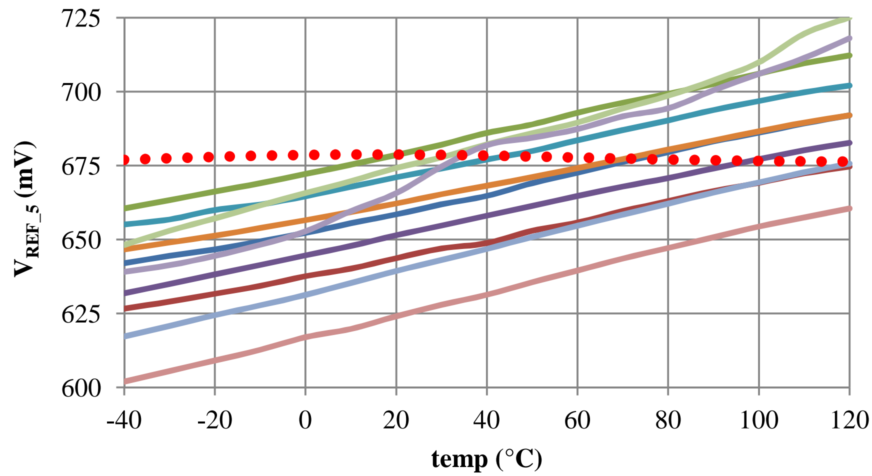
Figure 6.21- Measured V_{REF_5} vs supply voltage for 10 samples



source: the author

V_{REF_5} circuit is composed by a I_{REF} bias circuit, two self-composite transistors and a diode-connected NMOS transistor. Based on the results of section 6.2, it is possible to consider that the current reference is properly operating as designed and its temperature behavior was well predicted by the Monte Carlo analysis. Moreover, based on the V_{CTAT} measurements (section 6.6), it was possible to verify that the CTAT behavior of the V_{GS} voltage of NMOS transistor working in weak inversion is properly estimated in the simulations. Our hypothesis is that the temperature behavior of self-composite cascode transistor implemented using transistors with the minimum length is not well modeled by the BSIM model. It seems that the voltage generated by self-composite cascode transistors have a larger TC (more PTAT) than the predicted by simulations.

Figure 6.22 - V_{REF_5} vs temp. for 10 measured samples (lines) and simulation (dots)



source: the author

Finally, table 6.13 summaries all measured performance of V_{REF_5}.

Table 6.13: Summary of measured performance for 10 samples of V_{REF_5}

at room temperature: 20 °C					
MC mean V_{REF} (mV)	**MC sigma V_{REF} (mV)**	**average V_{REF} (mV)**	**max V_{REF} (mV)**	**min V_{REF} (mV)**	**VDD sensitivity (mV/V)**
681	28.7	656.9	678.6	624.1	2.7
Reduced temperature range: -40 to 80 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
4.6	2.6	41.6	55.3	33.8	396.5
Extended temperature range: -40 to 120 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
5.9	3.4	56.6	79.0	45.4	538.2

Source: the author

6.8 V_{REF_6}: Resistorless V_{TH0}-based reference using composite transistors

The values of V_{REF} (mV) at 20°C and ΔV_{REF_TEMP} (mV) in the temperature range of - 40 to 80 °C for 10 measured samples are shown in table 6.14 and figure 6.23. As can be seen in figure 6.20, the maximum difference between the measured samples and the nominal value of V_{REF_6} is 54 mV.

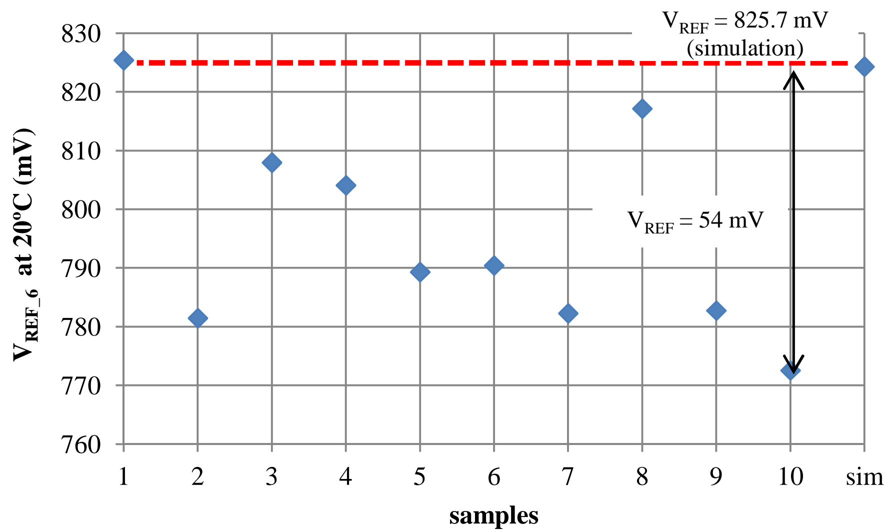
From the Monte Carlo analysis shown in Chapter 4, the sigma of V_{REF_6} (mV) at 20°C is 27.3 mV. All samples fit within an interval of ± 2 sigma of the Gaussian distribution.

Table 6.14: V_{REF_6} (mV) at 20°C and V_{REF_TEMP} (mV) for 10 measured samples

Sample 1	**Sample 2**	**Sample 3**	**Sample 4**	**Sample 5**	**Sample 6**	**Sample 7**	**Sample 8**	**Sample 9**	**Sample 10**
V_{REF} (mV) at 20 °C									
825.4	781.5	808.0	804.1	789.3	790.4	782.3	817.1	782.7	772.5
V_{REF_TEMP} (mV): from - 40 to 80 °C									
25.4	32.6	29.5	29.1	30.7	22.4	29.1	29.2	23.9	30.7

source: the author

Figure 6.23 - V_{REF_6} at 20°C for 10 samples



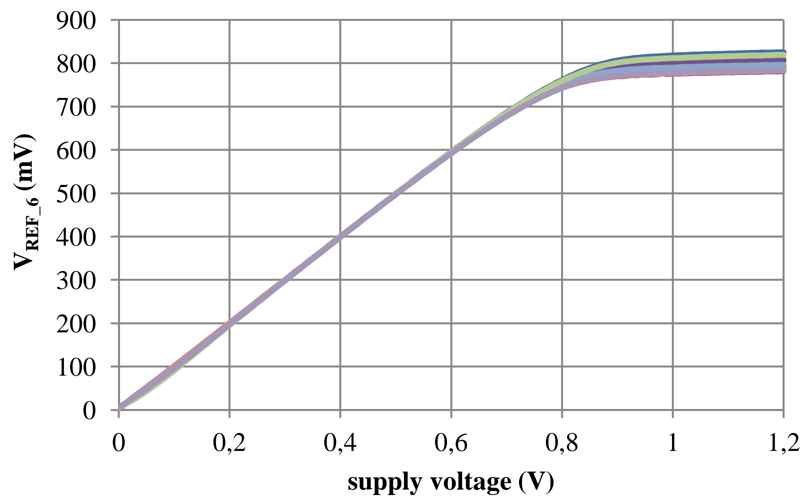
source: the author

Figure 6.24 shows V_{REF_6} as a function of supply voltage and as one can see, all samples work for a supply voltage larger than 0.8 V. Regarding the supply voltage sensitivity, an

average variation of 29 mV/V was observed. The line regulation performance of V_{REF_6} is ten times worse than V_{REF_5} because the former does not use cascode devices in order to mitigate the effect of supply voltage variation on the current mirror.

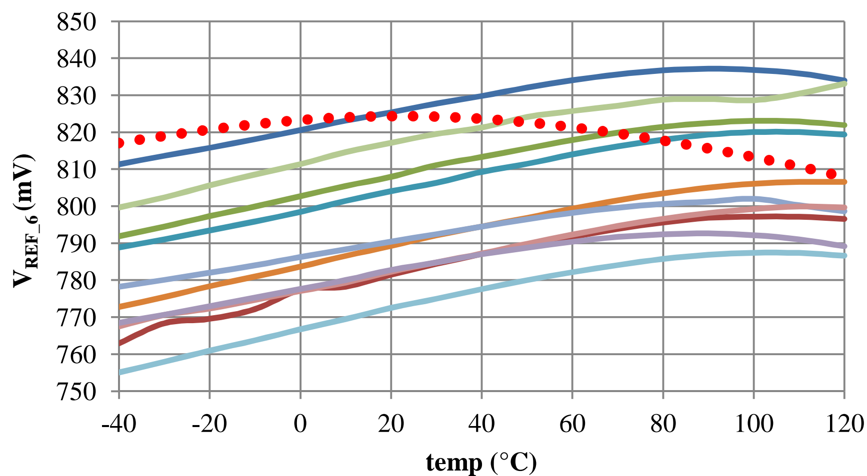
Figure 6.25 shows the temperature performance of V_{REF_6}. Considering the temperature range of -40 to 80 °C, the average value of ΔV_{REF_TEMP} and TC are 28 mV and 220 ppm/°C, respectively. The mean and sigma of ΔV_{REF_TEMP} are 9.1 mV and 1.8 mV, respectively.

Figure 6.24 - Measured V_{REF_6} vs supply voltage for 10 samples



source: the author

Figure 6.25 - V_{REF_6} vs temp. for 10 measured samples (lines) and simulation (dots)



source: the author

Similarly to the V_{REF_5} circuit, the temperature variation of V_{REF_6} is worse than the predictions done by the Monte Carlo and corners simulations. The formulated hypothesis done in section 6.7 for the unexpected temperature performance of V_{REF_5} is also assigned to V_{REF_6} as well.

Table 6.15 summarizes all measured data of V_{REF_6}.

Table 6.15: Summary of measured performance for 10 samples of V_{REF_6}

at room temperature: 20 °C					
MC mean V_{REF} (mV)	**MC sigma V_{REF} (mV)**	**average V_{REF} (mV)**	**max V_{REF} (mV)**	**min V_{REF} (mV)**	**VDD sensitivity (mV/V)**
825.7	27.3	795.3	825.4	772.5	29
Reduced temperature range: -40 to 80 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
9.1	1.8	28	32.6	22.4	219
Extended temperature range: -40 to 120 °C					
MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***max* V_{REF_TEMP} (mV)**	***min* V_{REF_TEMP} (mV)**	**average TC (ppm/°C)**
17.6	3.7	30	34.2	23.8	235

Source: the author

6.9 V_{REF_7} and V_{REF_8}: Bandgap reference using 2.5-V transistors

As presented in Chapter 4, the output voltages of V_{REF_7} and V_{REF_8} is generated by a balanced sum of PTAT voltage implemented by means of self-cascode transistors, and a CTAT voltage implemented by means of diodes.

Table 6.16 presents the measured diode voltages employed by V_{REF_7} and V_{REF_8} for five samples. The output pin is located at the source of M_7 transistor (figure 4.15). For V_{REF_7} and

V_{REF_8}, the diode voltages were implemented by means of PMOS transistor (fig. 4.6) (V_{PMOS}) and a PNP bipolar (V_{PNP}), respectively.

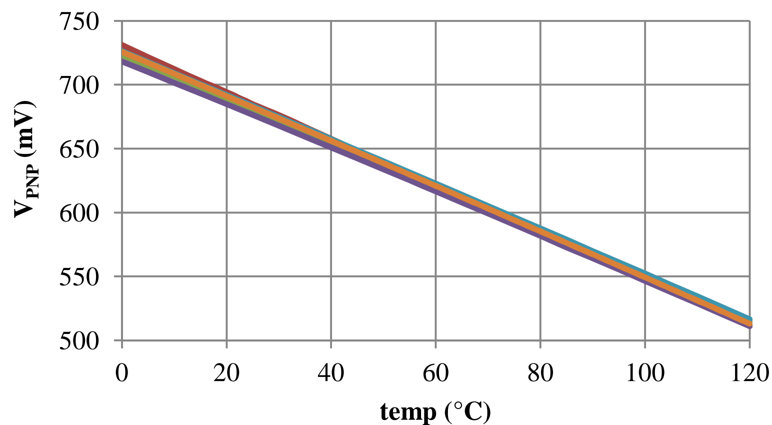
Table 6.16: Measured V_{PNP}, V_{PMOS} (mV) at 20 °C and V_{TEMP} (0 to 120 °C)

	sample 1	sample 2	sample 3	sample 4	sample 5	average	simulation
V_{PNP} (mV)	692.5	694.2	689.4	684.7	699.0	690.6	691.1
V_{PNP_TEMP} (mV)	213.6	219.6	208.5	207.1	209.6	211.7	212.8
$TC_{_PMOS}$ (ppm/°C)	-2571	-2636	-2521	-2521	-2524	-2554	- 2566
V_{PMOS} (mV)	795.5	792.2	791.8	785.1	795.2	792.0	749.1
V_{PMOS_TEMP} (mV)	171.9	172.5	165.2	156.7	166.3	166.5	202
$TC_{_PMOS}$ (ppm/°C)	-1748	-1748	-1709	-1677	-1709	-1718	- 2301

source: the author

Figure 6.28 shows V_{PNP} as a function of temp. As can be seen for V_{PNP}, there is a very good agreement between the silicon and simulation, either the value at 20 ºC as the temperature coefficient.

Figure 6.28 - V_{DIODE} as a function of temp. for 5 samples and simulation (dotted)

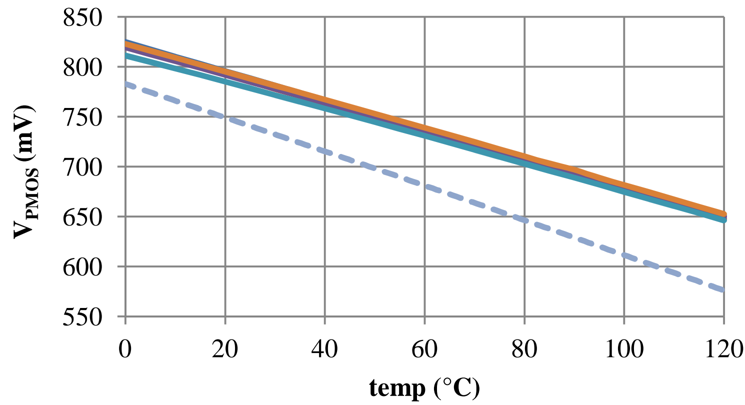


Source: the author

Figure 6.29 shows V_{PMOS} as a function of temperature. The first verification is that the measured data is shifted by about +40 mV. Apart from this discrepancy, the measured temperature coefficient is about ~25% difference from the simulation results. The worse predictability of V_{PMOS} compared to V_{PNP} is expected since the electronic model for the former one are not well calibrated and intended to be used for voltage reference design.

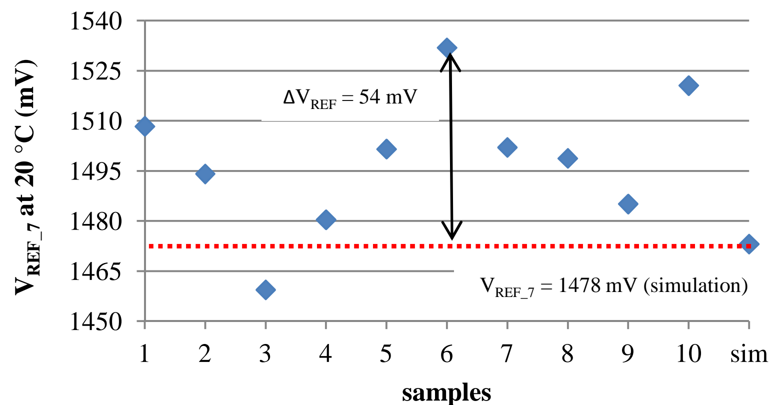
V_{PMOS} voltage could be used in an application that requires a very low area but tolerant to the diode variability.

Figure 6.27 - V_{PMOS} as a function of temp. for 5 samples and simulation (dotted)



source: the author

Figure 6.28 - V_{REF_7} at 20°C for 10 samples

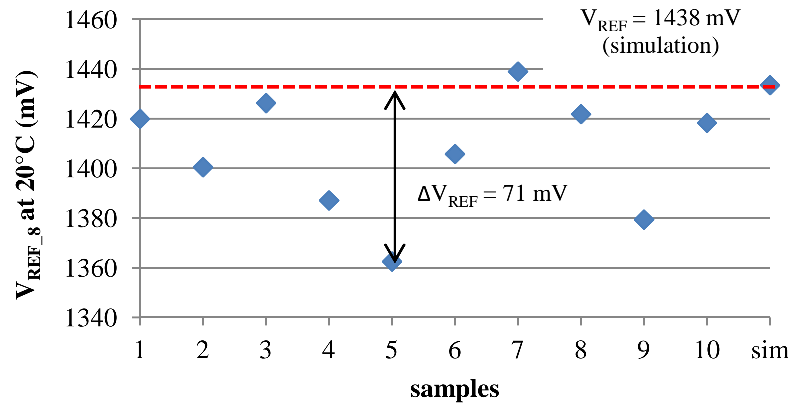


Source: the author

Ten samples of V_{REF_7} and V_{REF_8} were measured and its values at 20°C and temperature performance are given in table 6.17. Figures 6.28 and 6.29 show the values of V_{REF_7} and V_{REF_8} at 20°C. The maximum difference between the measured samples and the nominal simulated value is 54 mV and 71 mV for V_{REF_7} and V_{REF_8}, respectively.

From the Monte Carlo analysis shown in Chapter 4, the sigma of both V_{REF_7} (mV) and V_{REF_8} at 20°C is 25 mV. For V_{REF_7} 9 of 10 samples fit inside within an interval of ± 2 sigma of the Gaussian distribution. For V_{REF_8}, 8 of 10 samples inside within an interval of ± 2 sigma.

Figure 6.29 - V_{REF_8} at 20°C for 10 samples



Source: the author

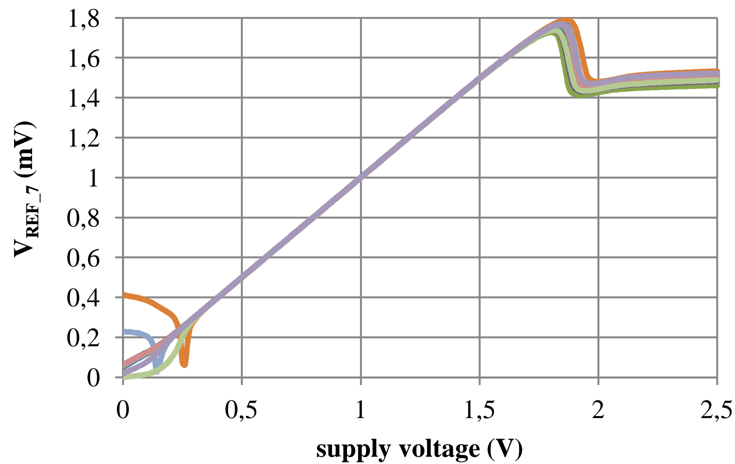
Table 6.17: V_{REF_7} and V_{REF_8} at 20°C and V_{REF_TEMP} for 10 measured samples

Sample 1	**Sample 2**	**Sample 3**	**Sample 4**	**Sample 5**	**Sample 6**	**Sample 7**	**Sample 8**	**Sample 9**	**Sample 10**
V_{REF_7} (mV) at 20 °C									
1508.3	1494.1	1459.4	1480.4	1501.5	1531.9	1502.0	1498.8	1485.1	1520.6
$V_{REF_TEMP_7}$ (mV): from - 40 to 80 °C									
63.8	57.1	63.7	67.6	59.6	65.4	67.0	65.2	40.7	53.4
V_{REF_8} (mV) at 20 °C									
1420.0	1400.5	1426.4	1387.1	1362.5	1405.8	1439.0	1421.9	1379.4	1418.4
$V_{REF_TEMP_8}$ (mV): from - 40 to 80 °C									
37.4	49.7	31.2	47.4	64.6	27.3	10.9	37.3	47.5	29.8

Source: the author

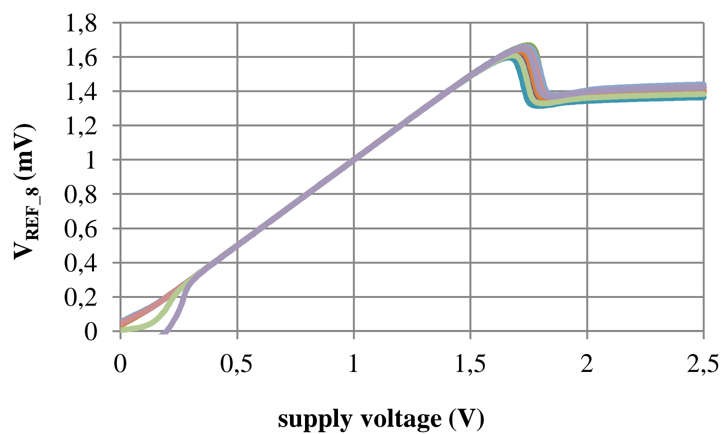
Figures 6.30 and 6.31 show V_{REF_7} and V_{REF_8} as a function of supply voltage and as one can see, all samples work for a supply voltage larger than 2.0 V. Regarding the supply voltage sensitivity, an average variation of 43 and 36 mV/V were observed for V_{REF_7} and V_{REF_8}, respectively.

Figure 6.30 - Measured V_{REF_7} vs supply voltage for 10 samples



source: the author

Figure 6.31- Measured V_{REF_8} vs supply voltage for 10 samples



source: the author

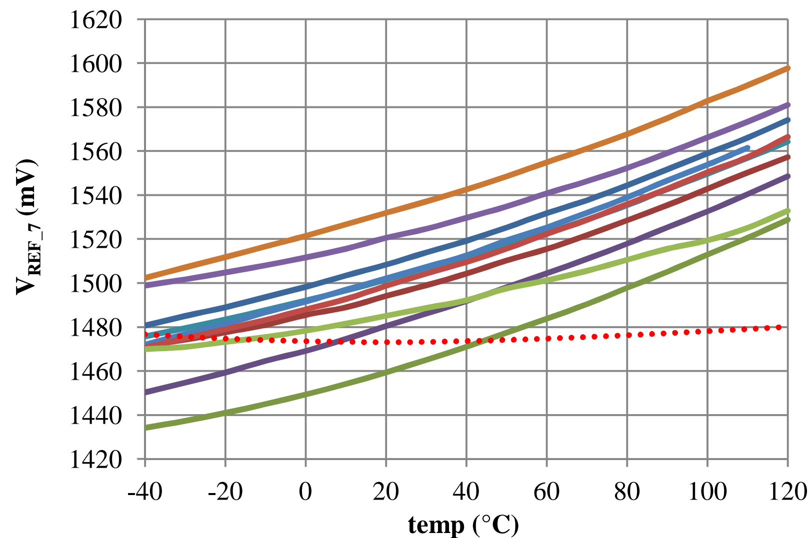
Figures 6.32 shows V_{REF_7} as a function of temperature. The average, worst and best values of ΔV_{REF_TEMP} are 60.3 mV, 67.6 mV and 40.7 mV, respectively; while the average TC is 336 ppm/°C. All samples clearly have a PTAT behavior and a larger slope if compared to the simulated temperature performance (figure 4.27 from Chapter 4).

The temperature behavior of V_{REF_7} estimated by the Monte Carlo analysis from Chapter 4 was much more optimistic: the mean and sigma value of ΔV_{REF_TEMP} are 9.7 mV and 5.4 mV, respectively, while the simulated average TC is 54 ppm/°C.

As early discussed in this chapter, all measured samples of current source (also employed in the design of V_{REF_7} and V_{REF_8}) present a temperature behavior that agrees with Monte

Carlo and corners analysis predictions. Moreover, although the measured values of V_{PMOS} present some difference when compared to the simulation results, it is not enough to cause such discrepancy in the temperature behavior of V_{REF_7}. Consequently, the non-expected TC of V_{REF_7} may not be assigned to I_{BIAS} and CTAT voltage (V_{PMOS}).

Figure 6.32 - V_{REF_7} vs temp. for 10 measured samples (lines) and simulation (dots)



source: the author

Figure 6.33 show V_{REF_8} as a function of temperature. The average, worst and best values of ΔV_{REF_TEMP} are 31.3 mV, 64.6 mV and 10.9 mV, respectively; while the average TC is 228 ppm/°C. The mean and sigma values of ΔV_{REF_TEMP} obtained from MC analysis are: 9.6 mV and 5.3 mV. The worst simulated ΔV_{REF_TEMP} is 41.2 mV. The first conclusion for V_{REF_8} is that the TC of the fabricated samples is also worse than the simulation predictions - as similar happen to V_{REF_7}.

The second finding is that V_{REF_8} presents a better agreement between silicon and simulation data than V_{REF_7}. It is certainly caused by the use of PNP device in order to implement the CTAT voltage. Note that the diode voltage (V_{PNP}) used in this design presents a very good agreement between simulation and silicon as discussed early.

Therefore, based on:

(i) V_{REF_5}, V_{REF_6}, V_{REF_7} and V_{REF_8} have larger TC (more PTAT) then the simulation results, and all of them use self-cascode transistors;

(ii) Their internal nodes (*e.g.* I_{BIAS} and V_{CTAT}) shows a good agreement between silicon and measured data,

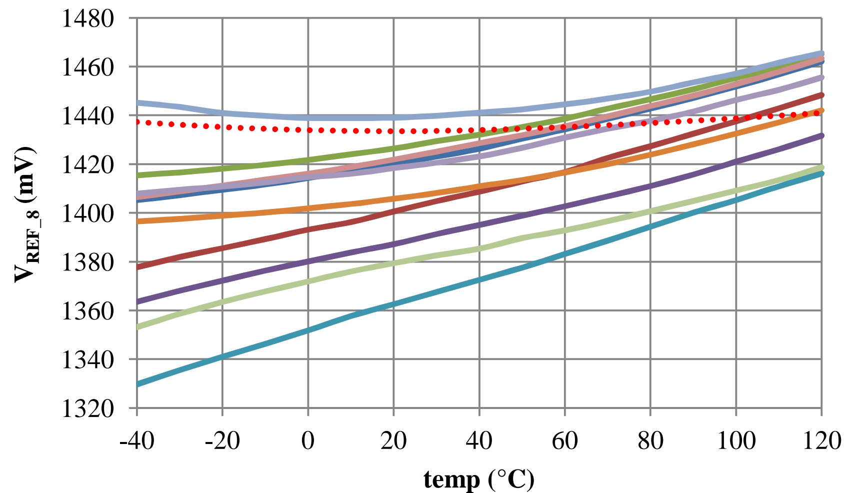
our hypothesis is that the PTAT voltage generated by our implementation (using minimum transistor length) of self-composite cascode transistor have a larger TC (more PTAT) than that shown in simulations.

Table 6.18 summaries all measured data of V_{REF_7} and V_{REF_8}.

Table 6.18: Measured performance for 10 samples of V_{REF_7} and V_{REF_8}

at room temperature: 20 °C						
	MC mean V_{REF} (mV)	**MC sigma V_{REF} (mV)**	**average V_{REF} (mV)**	**max V_{REF} (mV)**	**min V_{REF} (mV)**	**VDD sensitivity (mV/V)**
V_{REF_7}	1473	25.3	1498.2	1531.9	1459.4	43
V_{REF_8}	1438	25	1406.1	1439.0	1362.5	36
Reduced temperature range: -40 to 80 °C						
	MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**Average V_{REF_TEMP} (mV)**	***Max* V_{REF_TEMP} (mV)**	***Min* V_{REF_TEMP} (mV)**	**Average TC (ppm/°C)**
V_{REF_7}	9.7	5.4	60.3	67.6	40.7	336
V_{REF_8}	9.6	5.3	38.3	64.6	10.9	228
Extended temperature range: -40 to 120 °C						
	MC mean V_{REF_TEMP} (mV)	**MC sigma V_{REF_TEMP} (mV)**	**average V_{REF_TEMP} (mV)**	***Max* V_{REF_TEMP} (mV)**	***Min* V_{REF_TEMP} (mV)**	**Average TC (ppm/°C)**
V_{REF_7}	13.7	8.1	88.7	98.3	63	370
V_{REF_8}	13.6	7.8	57.4	86.54	26.7	256

Figure 6.33 - V_{REF_8} vs temp. for 10 measured samples (lines) and simulation (dots)



source: the author

6.10 V_{REF_9}: Low dropout (LDO) regulator

Seven samples of V_{REF_9} were measured and its value at 20°C and the temperature performance are presented in table 6.19. Figure 6.34 shows V_{REF_9} (mV) at 20°C.

For the data measured, the maximum difference between silicon and simulation is 58 mV. The output voltage is approximately equal to 1.33*V_{REF_1}. Since the mean value and sigma of V_{REF_9} are 927.3 mV and 21.3 mV, respectively and then, the most part of samples fits inside an interval of ± 2 sigma of the Gaussian distribution.

Figure 6.35 shows V_{REF_9} as a function of supply voltage. As can be seen, the minimum supply voltage for operation is 1 V, which agrees with the simulation results. The minimum required supply voltage is given by V_{OUT} (~900 mV) + V_{DSAT_M1} (~ 100 mV). Regarding supply voltage sensitivity, the output voltage achieves an average variation of 16 mV/V.

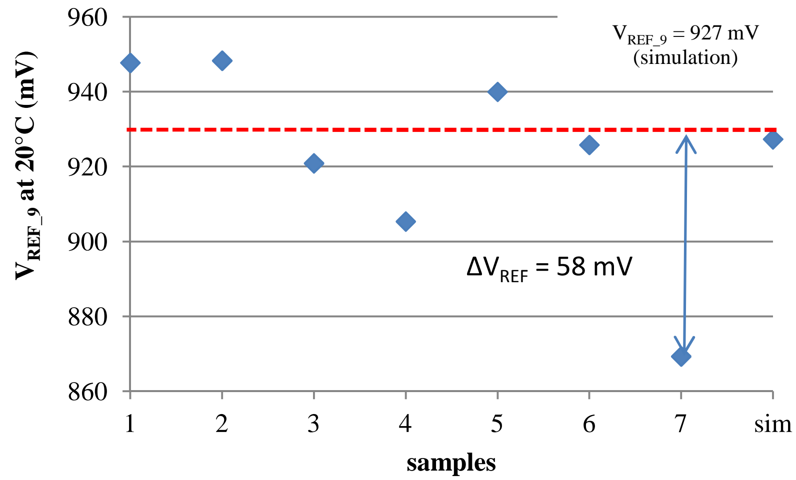
Figure 6.36 shows the temperature performance of V_{REF_9} for seven samples. The average value of ΔV_{REF_TEMP} is 11.7 mV what means an average TC of 99 ppm/°C in the temperature range of -40 to 80°C.

Table 6.19: V_{REF_9} (mV) at 20°C and V_{REF_TEMP} (mV) for 7 measured samples

Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6	Sample 7	Average
V_{REF} (mV) at 20 °C							
947.7	948.3	920.9	905.3	940	925.8	869.3	922.5
V_{REF_TEMP} (mV): from - 40 to 80 °C							
5.2	7.9	3.3	24	4.9	17.2	11.7	10.6

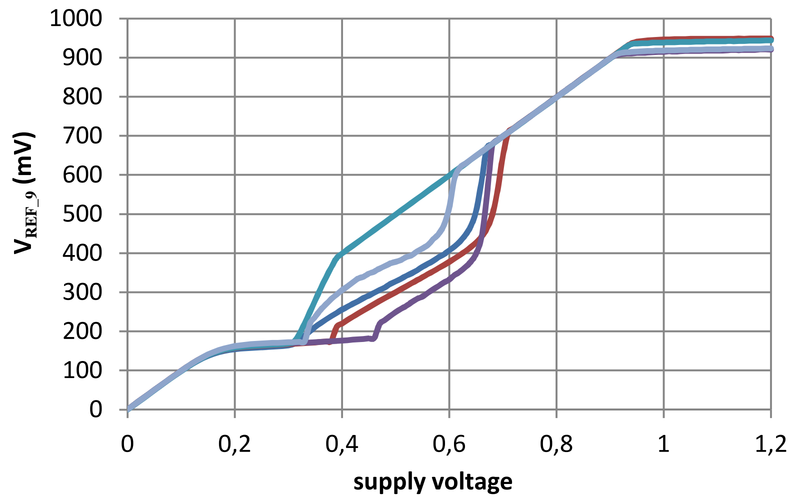
source: the author

Figure 6.34 - V_{REF_9} at 20°C for 7 samples



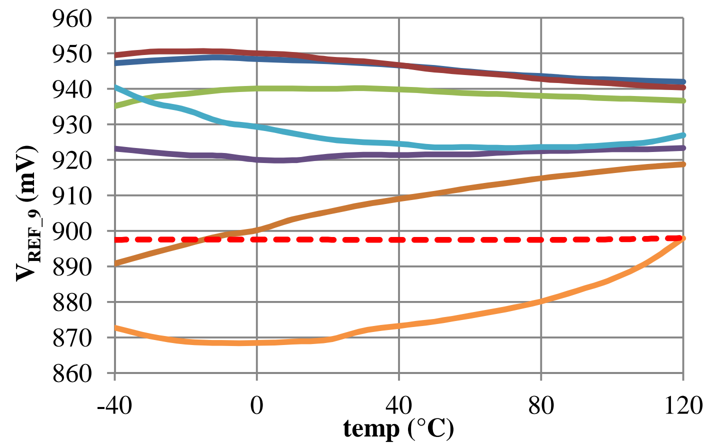
source: the author

Figure 6.35 - V_{REF_9} vs supply voltage for 5 samples



Source: the author

Figure 6.36 - V_{REF_9} vs temp. for 7 measured and simulation (dotted)



Source: the author

6.11 TID effects

The radiation experiment was carried out in Laboratório de Radiação Ionizante (LRI) of the Instituto de Estudos Avançados (IEAv) - Departamento de Ciência e Tecnologia Aeroespacial (DCTA), in São José dos Campos, São Paulo/Brazil.

The chip was irradiated through -ray of a Cobalt source (^{60}Co) shown in the figure 6.37.

Figure 6.37 - ^{60}Co source and test circuit inside LRI/IEAv laboratory

Source: Alan Rossetto

The chip was irradiated continually during about 320 hours with a deposition rate of 1535 rad/h. Therefore, the total accumulated dose irradiated in our case-study circuits was 490 krad. The room temperature was kept constant and equal to 23 °C (with about ± 1 °C of variation) during the irradiation experiment.

The chip was supplied with the nominal operation voltage (1.2 and 2.5 V) through of PXI-4110 and PXI-4130 from National Instruments. The data acquisition was done every 5 minutes using PXIe 6259 and PXI 4072 for the voltages and current measurements, respectively. These measurement modules were controlled by the NI-PXIe 8135 controller.

The PXI-4072 (6 1/2 digit multimeter) was programmed to operated in the 20 mA range in order to achieve the best available resolution of 10 nA. Since the designed current reference (I_{REF}) is about 525 nA (nominal) at the room temperature, a measurement uncertainty of ~ 2% is expected due to the equipment resolution. For the voltage measurements, the absolute accuracy of PXIe 6259 is less than 1 mV, and then a precise characterization is achieved.

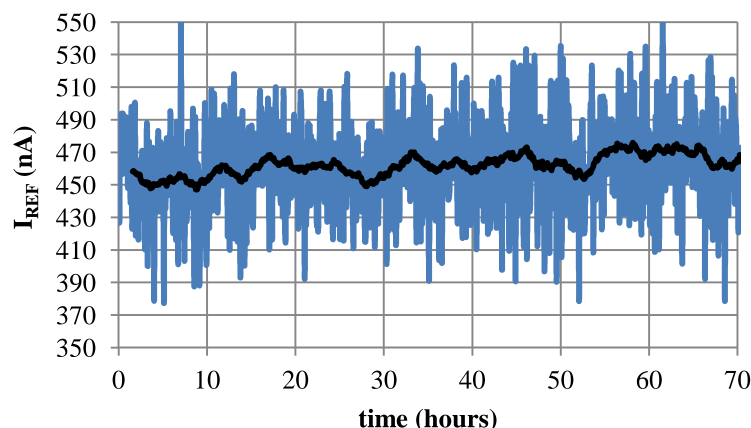
Unfortunately, due to the limited availability of resources allocation (human and equipments), only one sample of the fabricated IC was irradiated.

6.11.1 TID Measurement setup test

Initially, in order to validate our setup measurement, the chip was powered, and the output voltages and current were monitored during 70 hours without any radiation source applied.

Figure 6.38 shows the current source (I_{REF} - section 4.2) as a function of time. The raw data is the blue line and the moving average is the red line. The first observation is the noise presented in the raw data; peaks of more than ± 50 nA can be seen. The noise is generated by all equipments connected in the setup measurement.

Figure 6.38 - I_{REF} vs time (hours): moving average (black) and raw data (blue)

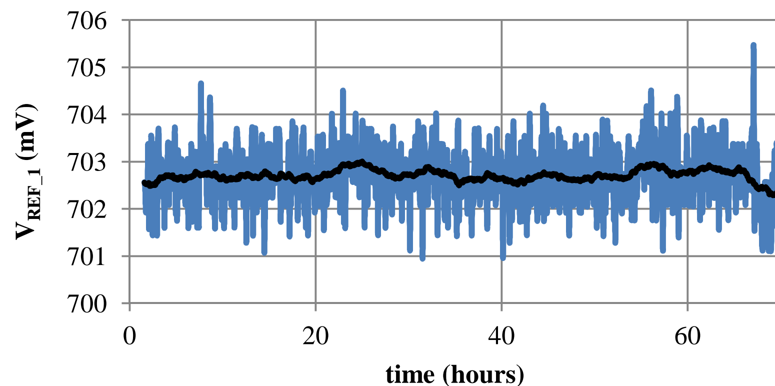


Source: the author

The second observation is regarding the moving average data. There was about 28 nA peak-to-peak of I_{REF} variation during the 70 hours. One cause of this variation is the limited accuracy of the current monitor (PXI-4072) of 10 nA. Other error source is the temperature variation (roughly ± 1 ºC) during the experiment. Since the implemented I_{REF} has TC of ~ 5200 ppm/ ºC, a current variation of at least 5 nA is expected to occur during the measurement.

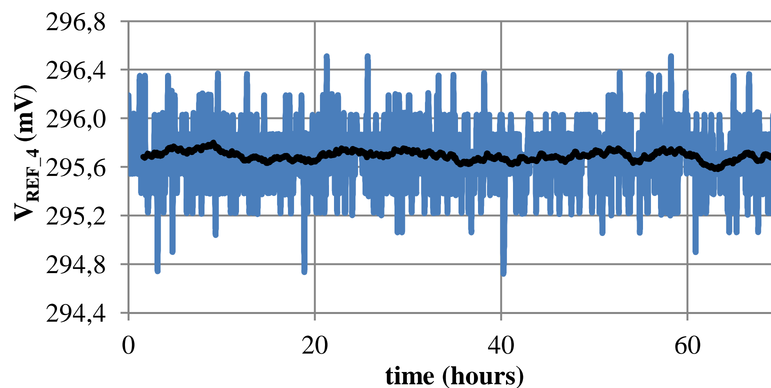
Figure 6.39 and 6.40 shows V_{REF_1} and V_{REF_4} as a function of time, respectively. As can be seen, the voltage measurement has better accuracy (lower variation) than the current measurement. Analyzing the moving average curves, one can verify that the voltage variation for both circuits during 70 hours of operation is lower than 1 mV peak to peak - what means that the setup is adequate for the TID experiment. Next sections present the output voltages and current during the irradiation process.

Figure 6.39 - V_{REF_1} vs time (hours): moving average (black) and raw data (blue)



Source: the author

Figure 6.40 - V_{REF_4} vs time (hours): moving average (black) and raw data (blue)



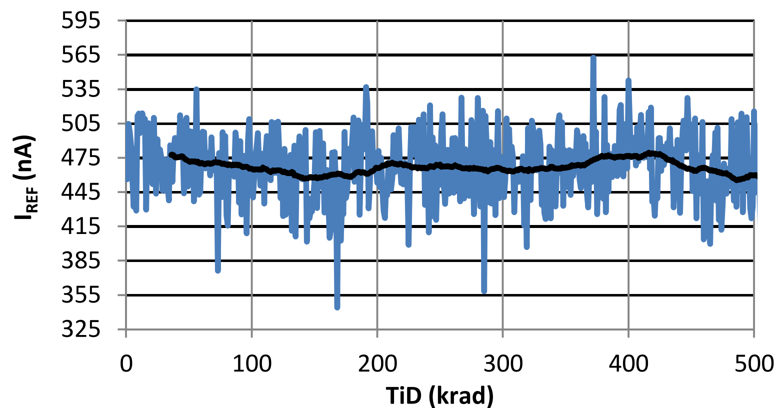
Source: the author

6.11.2 Current reference (I_{REF})

Figure 6.41 shows I_{REF} as a function of the total ionization dose TID (krad) for the moving average (red) and raw data (blue). The x-axis starts with 0 rad that means the value of I_{REF} before irradiation starts.

There is not a clear tendency of I_{REF} and TID in this figure. The mean value of I_{REF} during the irradiation process is about 460 nA with variations of about ± 22 nA. Taking into account the inaccuracy of the current measurement setup discussed before, it is not possible to accurately estimate the impact of TID on I_{REF}. However, it is possible to consider that the impact of TID of up to 490 krad on this single sample is lower than 10%.

Figure 6.41 - I_{REF} vs TID (krad)



Source: the author

6.11.3 V_{REF_1}: Bandgap-based reference

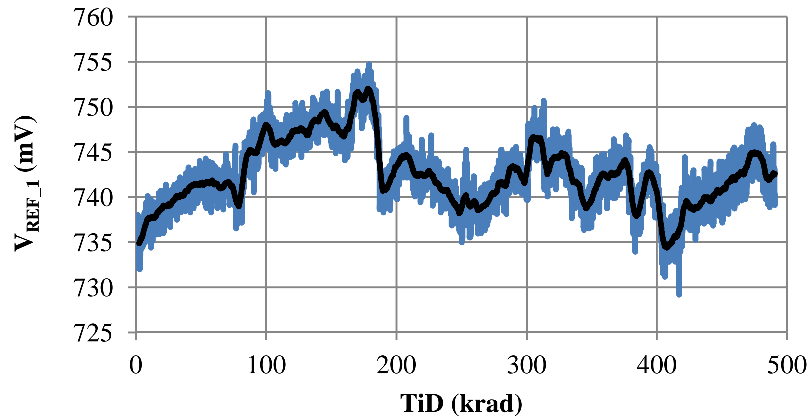
Figures 6.42 shows V_{REF_1} as a function of TID. The value of V_{REF_1} pre-radiation is 734 mV, while its maximum irradiated value is 752 mV when TID dose is 175 krad. It means a worst case variation ($\Delta V_{REF_TID} = V_{REF_PRE} - V_{REF_TID}$) of 18 mV.

Figure 6.43 shows V_{REF_1} as a function of TID through the output pin presented inside the voltage regulator (V_{REF_9} of figure 4.17). The layout of V_{REF_1} was instantiated in the design of voltage regulator using the same horizontal orientation.

Differently from what happens for the isolated V_{REF_1} circuit, this case shows an initial addition of + 39 mV in the value of the output voltage for TID in the beginning of the

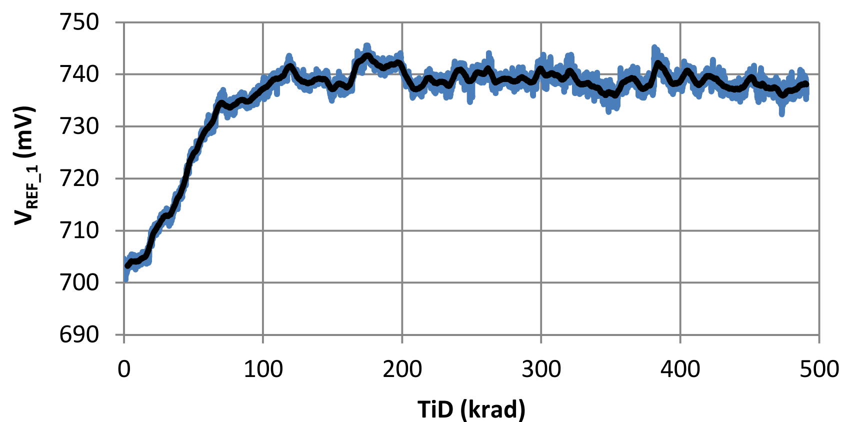
irradiation process (around 100 krad). After that, V_{REF_1} becomes nearly 739 mV with ± 4 mV of variation.

Figure 6.42 - V_{REF_1} vs TID (krad)



Source: the author

Figure 6.43 - V_{REF_1} (obtained from V_{REF_9} circuit) vs TID (krad)



Source: the author

Comparing the pre-irradiation and the worst case irradiated values in figure 6.43, ΔV_{REF_TID} is about 39 mV. The degradation of the BJT current gain ($_F$) and the op-amp offset voltage (V_{OS}) are possible causes of this variation of the output voltage.

Comparing figures 6.42 and 6.43, and knowing that both of them refer to the same circuit with the same layout (only placed in a different part of the chip), we miss more irradiated samples in order to make a more precise conclusion about the discrepancy between these two data. However, the initial and fast increase of the bandgap output voltage (figure 6.43) for

this type of circuit topology is expected, and it is in agreement to (CARDOSO, 2014) and (Cao, 2013).

As discussed in section 2.8, STI field oxide is usually placed surrounding the p+ diffusion region, which it is the emitter of the PNP transistor. Irradiation induced holes get trapped in the body of the field oxide therefore increasing the base leakage current and degrading the current beta gain ( ) (PIEN, 2010) and (PEACE, 2003).

The increase on the base leakage ($\Delta I_B > 0$) is different for the two branches of the Bandgap circuit (see figure 4.3). Since diode D_2 has 8 devices in parallel, there is a large increase on the base leakage current than compared to D_1, that it is only one device.

The increase on the base leakage (degradation of) results in a reduction of the collector current (ΔI_C). Through equation (5.1) (SEDRA, 1997), one can see that a reduction in I_C leads to a reduction in V_{EB}.

$$V_{EB} = U_T \cdot \ln(I_C/I_S) \tag{5.1}$$

Since $|\Delta V_{EB_D2}| > |\Delta V_{EB_D2}|$ due to the several devices connected in parallel (and greater leakage), the resulting $\Delta V_D = V_{D1} - V_{D2}$ (please, see equation 4.13) tends to increase with TID. The increase of ΔV_D (and the decrease of V_{EB}) were verified experimentally in (CARDOSO, 2014) and (Cao, 2013).

Due to the increase of ΔV_D, there is an increase of the BGR bias current ($I_{1b} = I_{2b}$) described by equation (4.11). Finally, V_{REF_1} increases because its bias current increase - result also verified experimentally in (CARDOSO, 2014) and (CAO, 2013).

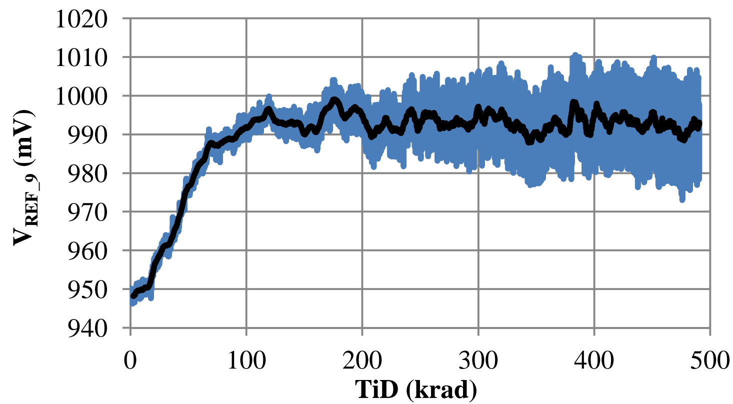
6.11.4 V_{REF_9}: Low dropout regulator

Extending the above discussion about V_{REF_1}, this section shows V_{REF_9} (voltage regulator) as a function of TID in figure 6.44. As expected, the output voltage, given by (V_{REF_1}*gain), has the same tendency than V_{REF_1}. Moreover, the obtained ΔV_{REF_9} is approximated equal to ΔV_{REF_1} * gain, where ΔV_{REF_9} is about ~ 49 mV, ΔV_{REF_1} is 39 mV and the voltage gain is 1.34.

In addition, figure 6.45 shows the gain of the voltage regulator. The gain would be only affected by the op-amp offset voltage and the ratio of the resistance (R_1 and R_2). As can be seen, the voltage gain is practically not affected by the TID effects. This is expected since the

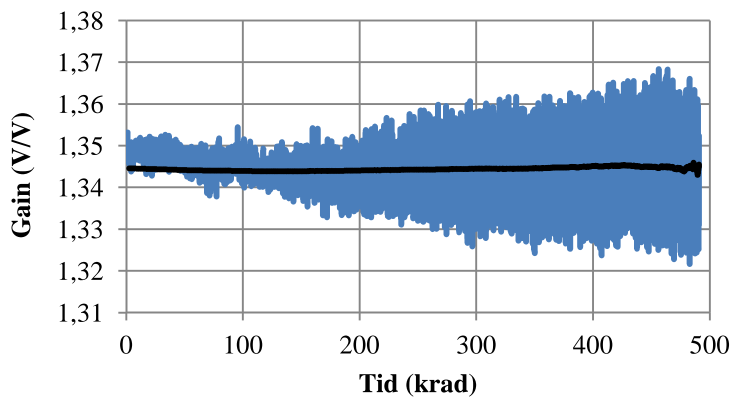
resistance is weakly affected by TID, and the offset voltage is probably low (and also weakly affected by TID) because the op-amp has wide and long channels transistors.

Figure 6.44 - V_{REF_9} vs TID (krad)



source: the author

Figure 6.45 - Voltage regulator gain vs TID (krad)



source: the author

6.11.5 V_{REF_4}: Alternative V_{TH0}-based reference

6.11.5.1 V_{PTAT} voltage

Figures 6.46 show the impact of radiation on V_{PTAT} voltage (at source terminal of N_4 in figure 4.10). It clearly shows an increase of the V_{PTAT} with the increase of TID. The value of V_{PTAT} before irradiation is 51.2 mV, and it increases about 4.5 mV (~ 9%) for a total dose of 490 krad.

From equation (4.7) and figure 4.10 (Chapter 4), V_{PTAT} is given by the difference of gate source voltages of N_3 and N_4 devices, and it is approximately described by equation (5.2):

$$V_{PTAT} = n \cdot U_T \cdot \ln\left(S_{N4} \cdot I_{DS_N3}\right)/\left(S_{N3} \cdot I_{D_N4}\right)] + (V_{TH_N3} - V_{TH_N4}) \qquad (5.2)$$

Note that the only difference among (5.2) and (4.7) is that the former one considers the threshold voltages of N_3 and N_4 are different. Both N_3 and N_4 devices have W/L = 3 µm/8 µm, but N_4 has ten devices in parallel while N_3 has only two.

Verifying equation (5.2), it is possible to conclude that there are three possible conditions caused by the TID that would result in the increase of $V_{PTAT:}$

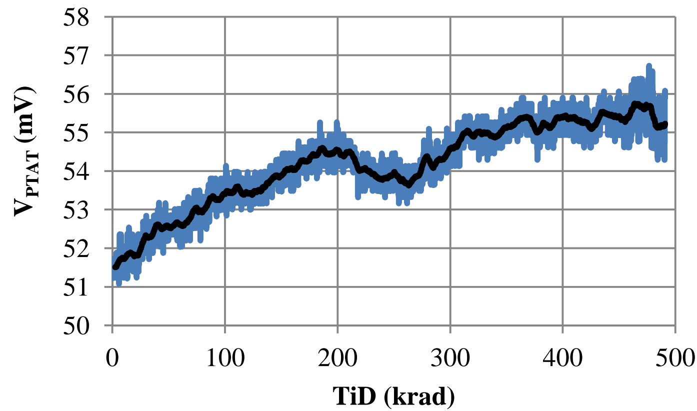
(i) $(S_{N4}/S_{N3})_{Prerad} < (S_{N4}/S_{N3})_{TiD}$ (Devices size ratio mismatch).

(ii) $\left(I_{DS_N3}/I_{DS_N4}\right)_{Prerad} < \left(I_{DS_N3}/I_{DS_N4}\right)_{TiD}$ (Current mirror mismatch),

(iii) $(V_{T_N3} - V_{T_N4})_{Prerad} < (V_{TH_N3} - V_{TH_N4})_{TiD}$ (Threshold voltage mismatch),

Indexes "Prerad" and "TID" mean pre-radiation and under TID effects, respectively.

Figure 6.46 - V_{PTAT} vs TID (krad)



source: the author

In Section 2.5, it was discussed that the shallow trench structures (STI) of MOS devices are the most radiation sensitive regions in CMOS modern circuits. Due to the positive charges trapped in the STI structures, parasitic paths between source and drain terminals are induced. These parasitic paths results in an increase of the leakage current, meanly important for (V_{GS} - V_{TH}) < 0 (weak inversion operation), as shown in figure 2.13.

Devices N_3 and N_4 operates in subthreshold mode and our main hypothesis is that the parasitic paths created by STI structures for N_4 (multiplicity = 10) are larger than that of N_3

transistor (multiplicity = 2) because there are more transistors and consequently, 5 times more available silicon area for parasitic paths. This scenario can be understood as an increase in the devices size ratio - condition named as (i).

In addition, also from figure 2.12 (please, see the arrow direction), greater TID greater is transistor conduction and probably more parasitic paths are created. This is in agreement with the increase of V_{PTAT} with TID.

Conditions (ii) and (iii) are also possible reasons of the increase of the V_{PTAT}. Considering N_3 and N_4 devices, threshold voltage shift caused by TID may have been different for these devices (*i.e.* $\Delta V_{TH_N4} < \Delta V_{TH_N3}$). Although N_3 and N_4 were designed in a common centroid layout configuration, this technique may have no effect in mitigating the TID effects.

The same effect can be expected for the PMOS devices of the current mirror, therefore resulting in an increase of the ratio (I_{DS_N3}/I_{DS_N4}) after irradiation. Moreover, the carrier mobility degradation caused by TID may also have been different for N_3 and N_4 ($\Delta\mu_{0_N3} > \Delta\mu_{0_N4}$).

The about 9% of variation of V_{PTAT} is also in agreement with the variation of I_{REF} due to TID presented in section 6.11.2. Since the I_{REF} is given by V_{PTAT}/R_{PTAT}, one could expect a variation around 11% if the impact of TID on integrated resistors can be neglected (or with maximum variation of 2% up to 2 Mrad as discussed in section 2.6).

Moreover, from the irradiated data of 130 nm CMOS transistors presented in section 2.6 and table 2.1, one could expect V_{TH_TID} lower than - 6 mV for the long and wide n-channel N_3 and N_4 devices. Therefore, we do not expect large variations due to TID on the V_{PTAT} voltage.

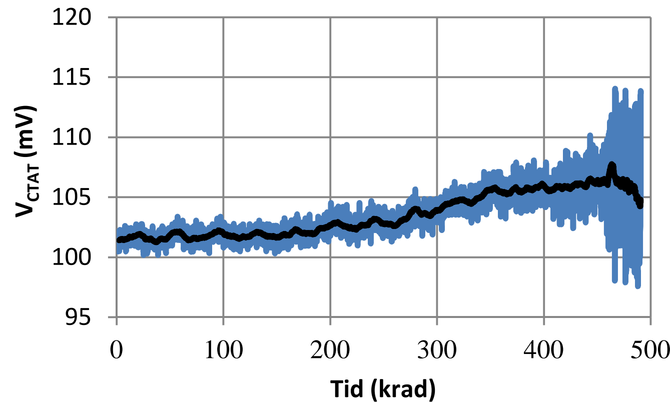
6.11.5.2 V_{CTAT} voltage

Figure 6.47 shows V_{CTAT} (the gate terminal of N_6 in figure 4.10) as a function of TID. It seems that V_{CTAT} increases with TID, as similarly observed by V_{PTAT}. The value of V_{CTAT} pre-irradiation was 101.4 mV and a maximum increase of 107.7 mV was observed during the irradiation process. It means a worst case ΔV_{CTAT_TID} of ~ 6.3 mV (about 6% of increase).

V_{CTAT} is the gate source voltage of N_6 that is biased with I_{PTAT} through a current mirror. Therefore, an increase on V_{PTAT} results in an increase of V_{CTAT} voltage. In addition, a current

mirror mismatch between devices P_3 and P_2 (figure 4.10) would also result in an increase of V_{CTAT}. However, as the gate source voltage is a natural logarithm function of I_{DS}, ΔV_{CTAT} is lower than ΔV_{PTAT}. Therefore, the observed variation of V_{CTAT} is consistent with our prediction.

Figure 6.47 - V_{CTAT} vs TID (krad)



Source: the author

Since N_6 device is a long and wide n-channel transistor, the expected V_{TH_TID} (mV) is lower than - 5 mV (for TID up to 500 krad) as discussed in section 2.6 and table 2.1. Therefore, we would not expect a significant reduction of V_{CTAT} (caused by the reduction of V_{TH}).

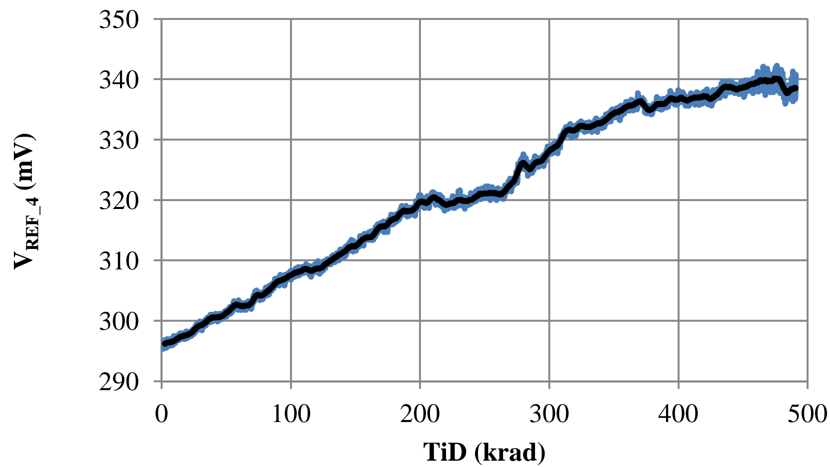
6.11.5.3 V_{REF_4} voltage

Figure 6.48 shows V_{REF_4} as a function of TID. As can be seen, the output voltage increases with TID. This is expected because V_{PTAT} and V_{CTAT} increases with TID as discussed above; and V_{REF_4} is generated by a sum of V_{CTAT} and V_{PTAT} (multiplied by a gain).

There was an increase of 44 mV or about 15% in V_{REF_4} for TID up to 490 krad. Considering an increase of $\Delta V_{PTAT} \sim 4.5$ mV and its nominal voltage gain of about 3.9 (ratio S_7/S_2, please see figure 4.10), and also $\Delta V_{CTAT} \sim 6.3$ mV, ΔV_{REF_TID} should be at least ~ 24 mV.

Therefore, besides the increase on V_{PTAT} and V_{CTAT}, other effect of TID may be also contributing to the increase of V_{REF_4} , as for instance, a mismatch in the p-channel current mirror or a slight reduction of R_3.

Figure 6.48 - V_{REF_4} vs TID (krad)

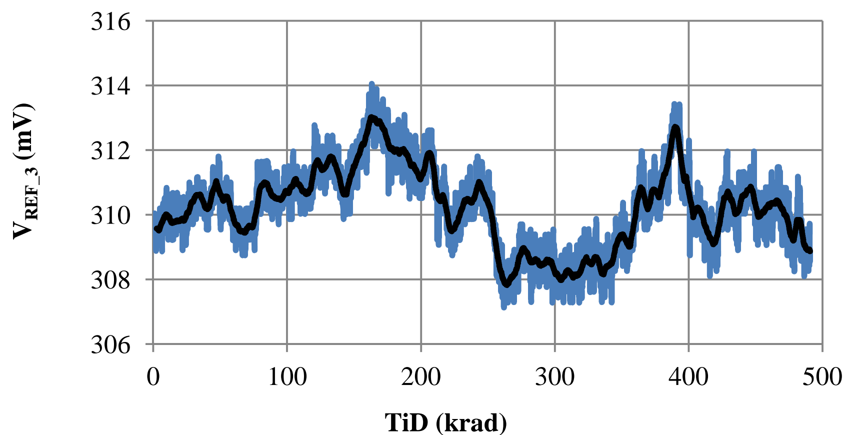


source: the author

6.11.6 V_{REF_3}: Simple V_{TH0}-based reference

Figure 6.49 shows V_{REF_3} as a function of TID. The value of V_{REF_3} pre-radiation is 310 mV, while the maximum and minimum values during irradiation are 313 mV and 308 mV, respectively. It means a worst case of ΔV_{REF_TID} equal to + 3 mV (± 1 %). Such variation means a good robustness against the impact of TID, if one considers that no radiation hardening technique was used.

Figure 6.49 - V_{REF_3} vs TID (krad)



Source: the author

Since all transistors of V_{REF_3} have wide and long channel, their electrical behavior is not severely affected by TID as shown in section 2.6. The lower number of devices of V_{REF_3}

compared to V_{REF_4}, may be one of the reasons why V_{REF_3} seems to be more robust against TID than V_{REF_4}.

6.11.7 V_{REF_7} and V_{REF_8}: Bandgap reference using 2.5-V transistors

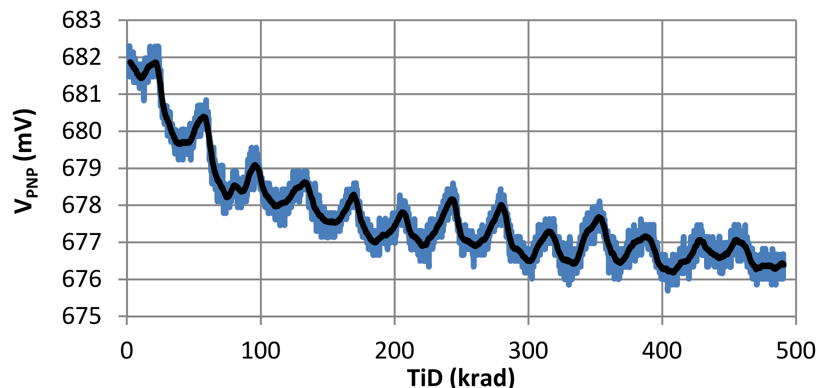
V_{REF_7} and V_{REF_8} circuit are shown in figure 4.15. As explained anteriorly, an output pin was placed in the drain of M_3 device in order to make possible the measurement of the diode voltage (V_{CTAT}). This section starts showing the impact of TID on the diode voltage.

6.11.7.1 V_{CTAT} voltage implemented by means of PNP device

Figure 6.50 shows V_{CTAT} implemented by means of PNP BJT as a function of TID (employed in the V_{REF_8} design). The first observation is the periodic variation of this voltage during the irradiation process. This variation also happens during the test measurement without radiation source, and it is caused by temperature variations during the experiment. The peaks are equally spaced in time and its quantity is the same of the number of days which the experiment was carried out.

The second verification is the reduction of about 6 mV (ΔV_{CTAT}) in V_{PNP} due to TID effects. This result is in agreement with our discussion regarding the reduction of the diode voltage in section 6.11.3. It is related to the increase of the base leakage current and the beta degradation.

Figure 6.50 - V_{CTAT} (V_{PNP}) vs TID (krad)



source: the author

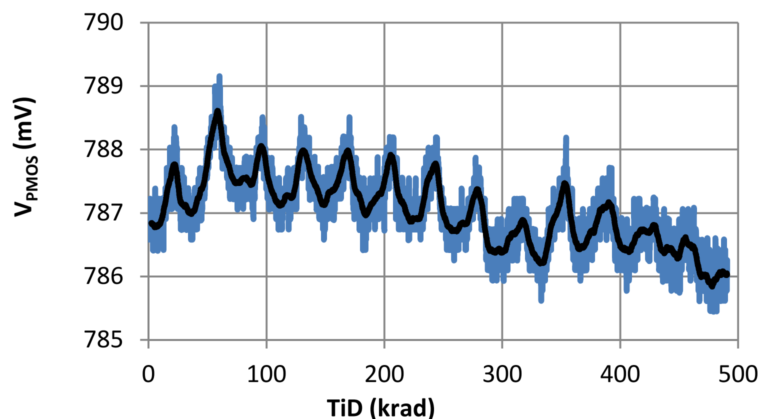
We also expect an increase on the PTAT bias current of the PNP device due to the increase of the V_{PTAT} (as discussed in section 6.11.4.1). However, the effect of the increase of the PTAT bias current (it would increases V_{CTAT}) was overlapped by the effect of the increase on the base leakage current.

6.11.7.2 V_{CTAT} voltage implemented by means of p-channel transistor

Figure 6.51 shows V_{CTAT} implemented by means of p-channel transistor as a function of TID (used in V_{REF_7} design). V_{PMOS} was more robust against TID than V_{PNP} and it varies about ± 1 mV during the irradiation process up to 490 krad.

Based on our discussions of sections 2.10 and 4.4 (PMOS diode), we would expect an increased robustness against the TID effects when using this implementation due to the longer distance of the diode and the STI oxide. It would be needed more irradiated samples in order to have a more scathing conclusion. The lower area of this device compared to the PNP device may also be the reason of the improved robustness.

Figure 6.51 - V_{CTAT} (V_{PMOS}) vs TID (krad)

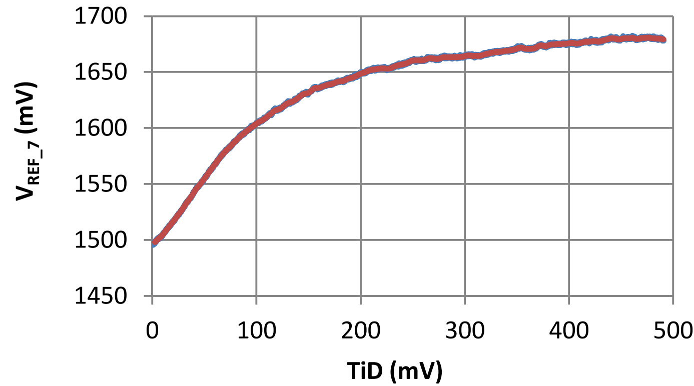


Source: the author

6.11.7.3 V_{REF_7} and V_{REF_8} voltages

Figures 6.52 and 6.53 shows V_{REF_7} and V_{REF_8} as a function of TID. Both circuits have a fast increase of the output voltage at the beginning of the radiation, and then smoothed increase after that.

Figure 6.52 - V_{REF_7} vs TID (krad)



Source: the author

For V_{REF_7}, there was an increase of 184 mV (~ 12%) for TID up to 490 krad. Since V_{CTAT} implemented in this design varies only ± 1 mV during the radiation process, other source of variation is dominating the circuit response under TID effects.

From section 4.9, the output voltage of V_{REF_7} and V_{REF_8} are given by the balanced sum of V_{PTAT} and V_{CTAT} voltages. The V_{PTAT} voltage is generated by means of self-cascode transistors, and it is given by (5.3) if devices M_8 and M_7 are considered.

$$V_{PTAT} = n \cdot U_T \cdot \ln \left(S_{M8} \cdot I_{DS_M7}\right)/\left(S_{M7} \cdot I_{D_M8}\right)] + (V_{TH_M7} - V_{TH_M8}) \qquad (5.3)$$

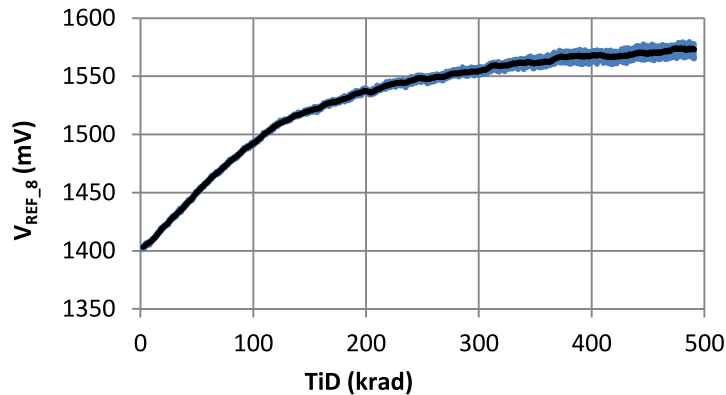
The same discussion about V_{PTAT} voltage of section 6.11.4.1 is also applicable here. Devices M_8 and M_7 have the same W and L, but the former one has 291 devices in parallel, while the last one does not have any one. As a consequence, there are much more parasitic devices in parallel with M_8 device, therefore increasing V_{PTAT} voltage. This effect could be modeled as an increase of the ratio (S_{M8}/S_{M7}).

In addition, the above effect was probably increased because the self-cascode devices were implemented using the minimum channel transistor length (250 nm) allowed to thick oxide devices. From section 2.6 and table 2.1, TID effects are much severe for minimum W and L dimensions.

A small and less significant contribution caused by the mismatch in the current mirror implemented by PMOS devices can also leads to some increase of the output voltage.

For V_{REF_8}, there was the same increase of about + 12% (172 mV) for TID up to 490 krad. Although V_{PNP} was slightly more affected than V_{PMOS}, this effect is small compared to the effect of parasitic MOS devices (increase of the ratio S_{M8}/S_{M7}).

Figure 6.53 - V_{REF_8} vs TID (krad)



Source: the author

Circuits V_{REF_2}, V_{REF_5} and V_{REF_6} were damaged during transportation and handling before irradiation procedure. Moreover, after the irradiation process, the bond-wire detaches from the chip and then, it was not possible to make the temperature characterization of the irradiated circuits.

6.11.8 Radiation Hardening By Design (RHBD)

The circuits implemented in this thesis did not use any radiation hardening technique. As discussed in Chapter 2, one of these efficient techniques is the enclosed layout transistor (ELT), that must be used when the applications require robustness against TID effects.

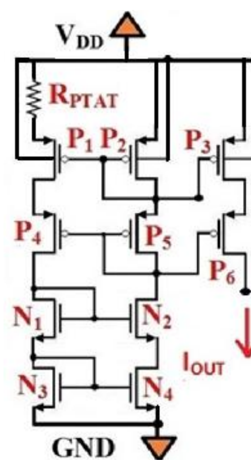
Based on the radiation theory discussed in Chapter 2 and the TID effects observed in our circuits, some design recommendations of how improving the robustness of the voltage references against TID are listed below. The first three recommendations are the traditional guidelines for mitigation of the fabrication process mismatch.

(i) Use the maximum overdrive voltage (V_{GS}-V_{TH}) allowed by the minimum supply voltage of operation. It means that strong inversion operations is preferred than weak inversion operation. As can be seen in figure 2.13, the impact of TID on V_{TH} is greater for weak inversion operation. This happen because the impact of parasitic channel (leakage current) through STI structure is more relevant for low values of current (*i.e.* low values of V_{GS}).

(ii) Use wide and long channel devices whenever possible. From section 2.6, the impact of TID effects decreases as W and L increases.

(iii) Employ p-channel transistors instead of n-channel transistor in key parts of the circuit because they are less sensitive to the TID than n-channel; at least for the CMOS process used in this work, as discussed in (BOCHENEK, 2012) and presented in table 2.1. As for instance, the I_{BIAS} circuit of figure 4.2 could be modified as shown in figure 6.54 without any significant impact on its performance parameters.

Figure 6.54 - Modification of the PTAT current source



source: the author

(iv) Decrease the design variable "N" used in the V_{PTAT} voltage generation (equation 4.7). This variable is the (W/L) ratio of two devices operating in weak inversion. The same temperature compensation can be achieved adjusting the resistors (silicon area penalty) or current mirror ratio (current consumption penalty). As discussed early, our hypothesis is that more parasitic transistors are formed for the device with larger multiplicity during the irradiation process, and as a consequence, V_{PTAT} increases with TID.

(v) Decrease the design variable "x" used in the Bandgap references design. Similarly to variable "N", "x" is used in the V_{PTAT} generation and it is the ratio of two diodes with different sizes. As discussed in section 6.11.3, this parameters tends to increase the bandgap output voltage under TID effects due to the base leakage current.

A suggestion of future work would be the implementation of few versions of the same circuit (for example, V_{REF_1} and V_{REF_7}) with different values of "N" and "x". This would check the validity of our above hypothesis.

A second suggestion is the measurement of the irradiated V_{CTAT} voltage implemented by the PNP device and PMOS diode using the device itself (without the circuit). This experiment would check the hypothesis regarding the improved robustness of PMOS diode.

6.12 Final conclusions

Table 6.20 summarizes the TID effects (up to 490 krad), the average of temperature performance (V_{REF_TEMP} in the range of -40 to 80°C) and the output voltage variation caused by the impact of fabrication process. The average, V_{REF_MAX} and V_{REF_MIN} were obtained from the 10 measured samples and measured at 20 ºC. The value of V_{REF_TID} is the difference between the pre-irradiation values and the worst case variation during the irradiation process up to 490 krad.

6.12.1.1 TID and fabrication process effects

As can be seen in table 6.20, the impact of radiation was similar or more severe than the fabrication process effects (*i.e.* considering 10 samples) for most of the case-study circuits. Only for I_{PTAT} and V_{REF_3}, the TID effects were lower than the fabrication process.

For the bandgap reference (V_{REF_1}), TID effects result in a variation of the output voltage of 5.5 %, while the total variation caused by the fabrication process was 4.8%. If we consider these two error sources are uncorrelated, the total error of V_{REF_1} considering fabrication process and TID effects is 7.3 %. For this circuit, the PNP BJT device was probably the main responsible for the voltage reference variation during irradiation process.

For the V_{TH}-based V_{REF_4} circuit, the TID effects were about 3 times worse than the impact of fabrication process. Regarding V_{REF_3}, it presents the best robustness against the fabrication processes probably because: (i) only wide and long channel transistors are used, (ii) low voltage and current gain between its branches are needed, and (iii) its lowest number of transistors.

The worst impact of TID was for V_{REF_7} and V_{REF_8} circuits (about 12 %). We expected this behavior because these circuits were implemented using thick-oxide transistors (more susceptible to TID than thin-oxide transistors). For these topologies, the self-cascode

transistors using the minimum channel length were probably the mean responsible for the output variation.

For V_{REF_1} and V_{REF_4}, TID effects were worse than 2-sigma variation caused by fabrication process effects. For V_{REF_7} and V_{REF_8}, TID effects were worse than 3-sigma variation.

Table 6.20: TID and measured performance of V_{REF} and I_{REF}

Circuit	MC mean (mV) or (nA)	$V_{REF_AVERAGE}$ (mV) or (nA) At 20ºC	V_{REF}_max (mV) or (nA) At 20ºC	V_{REF}_min (mV) or (nA) At 20ºC	$\Delta V_{REF_PROCESS}$: V_{REF_MAX} - V_{REF_MIN} At 20ºC		ΔV_{REF_TID} (mV) or (nA)		ΔV_{REF_TEMP} (mV) and (%)	
					(mV) or (nA)	(%)	(mV) or (nA)	(%)	(mV) or (nA)	(%)
V_{REF_1}	674	695.6	714.7	681.3	33.4	4.8	39	5.5	9	1.3
V_{REF_2}	697.3	705.4	728.8	691.6	37.2	5.3	n/a	n/a	19	2.7
V_{REF_3}	317	302.3	311.8	291.9	19.9	6.6	6	2	14.6	4.8
V_{REF_4}	307.8	301.1	311.5	297.3	14.2	4.7	44	15	11.3	3.8
V_{REF_5}	681	656.9	678.6	624.1	54.5	8.3	n/a	n/a	41.6	6.3
V_{REF_6}	825.7	795.3	825.4	772.5	52.9	6.7	n/a	n/a	28	3.5
V_{REF_7}	1473	1498.2	1531.9	1459.4	72.5	4.8	184	12	60.3	4.0
V_{REF_8}	1438	1406.1	1439.0	1362.5	76.5	5.4	172	12	38.3	2.7
I_{PTAT}	497	525.9	617.7	451.2	166.5	32	22	5	323	61.5

Source: the author

As shown in this section, TID severely degrades the accuracy of the voltage references circuits, and thus, it should be considered when estimating the total tolerance of voltage references when the application is susceptible to TID effects.

6.12.1.2 Temperature performance and impact of fabrication process

Comparing the mean value of V_{REF} at 20 ºC obtained from MC analysis and the average value of the measured samples ($V_{REF_AVERAGE}$), we can see that the all designed circuit performed as expected and predicted in our simulations. Moreover, verifying the standard

deviation of V_{REF} also obtained from MC analysis, the most part of samples fits inside within an interval of ± 2 sigma of the Gaussian distribution. Only few samples fit inside within an interval of ± 3 sigma as shown throughout this Chapter.

Regarding the temperature coefficient of the measured circuits, references I_{PTAT}, V_{REF_1}, V_{REF_2}, V_{REF_3} and V_{REF_4} performed as predicted in our Monte Carlo analysis. All of them have a variation of less than 5% in the temperature range of - 40 to 80 ºC. From those circuits, the V_{G0}-based V_{REF_1} presented the best performance.

Considering V_{REF_5}, V_{REF_6}, V_{REF_7} and V_{REF_8} references, all of them had presented a temperature coefficient a little more positive than predicted by our corner and MC simulations. Although the circuit stress caused by the packaging process is not taken into account in our simulations, it is certainly not the cause of this small discrepancy between silicon and simulations. These circuits have in common the use of self-cascode transistors using the minimum length channel in order to generate the V_{PTAT} voltage. Our hypothesis is that the temperature behavior of this V_{PTAT} voltage was not accurately predicted by the simulation due to some limited modeling of second order effects of these structures. However, this discrepancy certainly can be corrected with some adjust in the temperature compensation, as for instance, decreasing the gain of the V_{PTAT} voltage. This correction can be done, as for instance, through an adjust in the current mirror gain (I_{PTAT} current gain) of these circuits. Finally, although the TC was a slightly worse than predicted by our simulations, the temperature performance is still proper for many applications. The temp. variation was less than 6.5% and 3% for V_{REF_5} and V_{REF_8}, respectively.

In addition, although there are not enough number of samples in order to make a consistent statistical analysis, V_{REF_1} and V_{REF_2} (the V_{G0}-based) had $V_{REF_PROCESS}$ little lower (*i.e.* at least - 1.4%) than the V_{REF_5} and V_{REF_6} (V_{TH0}-based) voltage references. These circuits were designed to have about the same output voltage. This increase variability of V_{TH0}-based voltage references is expected and it is caused by the high dispersion of V_{TH}. The transistor V_{TH} is a strong function of process parameter which are hard to control in the fabrication of downscaled technologies, such as the doping at the transistor channel region.

7 SILICON MEASUREMENT - OSCILLATORS

7.1 Oscillators implemented in 130 nm CMOS process

The measurement of the ring-oscillator implemented in 130 nm was done using the same test board used for the voltage references shown in figure 6.2. The output buffer of the ring-oscillator was connected to 47- resistor plus a DC blocking capacitor, and then, to a SMA connector. The resistor is used to allow an impedance matching between the circuit and the measurement equipments. The output impedance of the ring output buffer is less than 10 due to the very large transistors.

Moreover, a large copper plate tied to ground was placed under the test board in order to improve our ground plane. Although our test board already had a ground plane, we observed a significant increase of the noise when the copper plate is removed.

7.1.1 Oscillation frequency (f_{OSC})

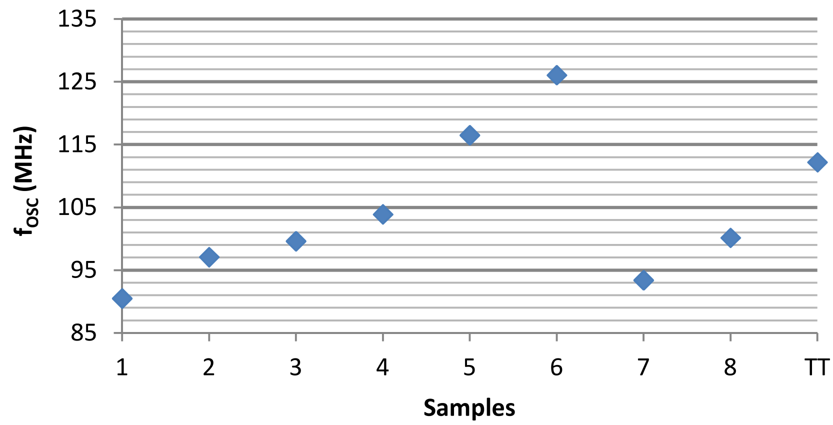
Eight samples of the fabricated ring-oscillator were measured. The oscillation frequency was measured by means of the Agilent 53131A Universal Counter. Figures 7.1 and 7.2 show f_{OSC} for all samples when the ring-oscillator is supplied with 700 mV and 800 mV, respectively. The buffer supply voltage was fixed with 750 mV during both measurements.

The measured results are in agreement to the simulations. For VDD_{RING} = 700 mV, the simulated f_{OSC} at nominal conditions (temperature and process model) is 112.2 MHz. The average, maximum and minimum measured values are 103.4 MHz, 126.1 MHz and 90.5 MHz, respectively.

For VDD_{RING} = 800 mV, the simulated f_{OSC} at nominal conditions (temperature and process model) is 172.4 MHz. The average, maximum and minimum measured values are 155.8 MHz, 180.3 MHz and 141.0 MHz, respectively. The measured average of f_{OSC} and the simulations differ by less than 10% for both supply voltages.

Figure 7.3 shows f_{OSC} as a function of VDD_{RING}. Considering a supply voltage variation from 550 mV to 900 mV, the average variation of f_{OSC} is 495 MHz/V or 495 kHz/mV. This result agrees with the simulated variation of 518 kHz/mV (chapter 5).

Figure 7.1 - Measured f_{OSC} (MHz) for 8 samples with VDD_{RING} = 700 mV



source: the author

Figure 7.2- Measured f_{OSC} (MHz) for 8 samples with VDD_{RING} = 800 mV

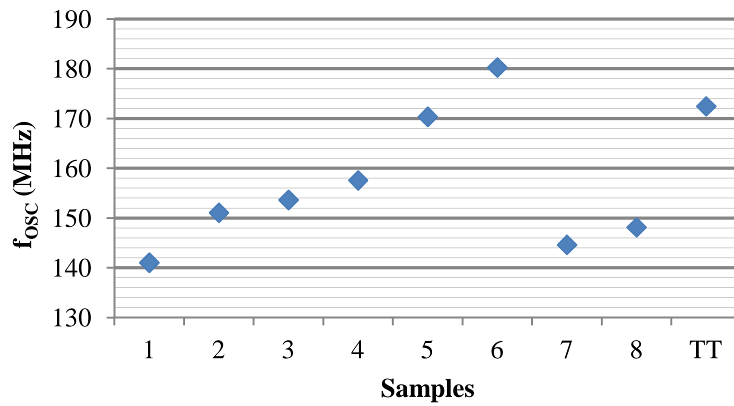


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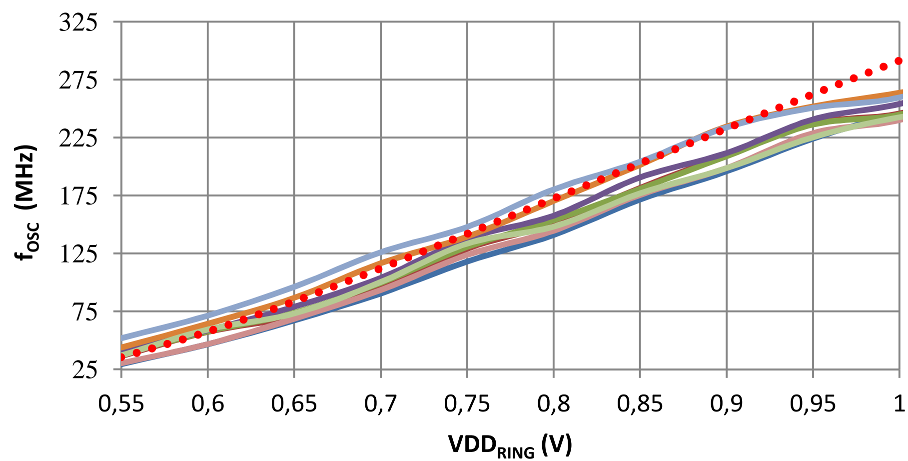
Figure 7.3 - Measured f_{OSC} vs VDD_{RING} for 8 oscillator samples and simulation (dots)



source: the author

7.1.2 Output voltage waveform

Figures 7.4 and 7.5 show the measured output voltage as a function of time for VDD_{RING} = 1.2 V and 0.85 V, respectively. The supply of the output buffer was kept equal to 750 mV. The peak to peak output voltage is about 400 mV. The measured f_{OSC} are equal to 333.4 MHz and 170 MHz for figures 7.4 and 7.5, respectively.

Figure 7.4 - Measured output voltage vs time for VDD_{RING} = 1.2 V (sample # 1)

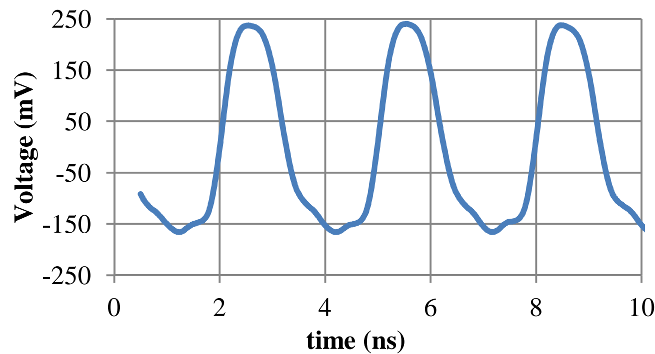


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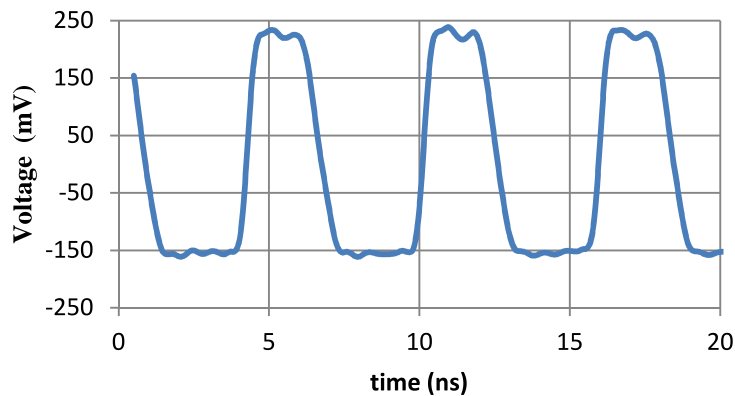
Figure 7.5 - Measured output voltage vs time for VDD_{RING} = 0.8 V (sample # 1)



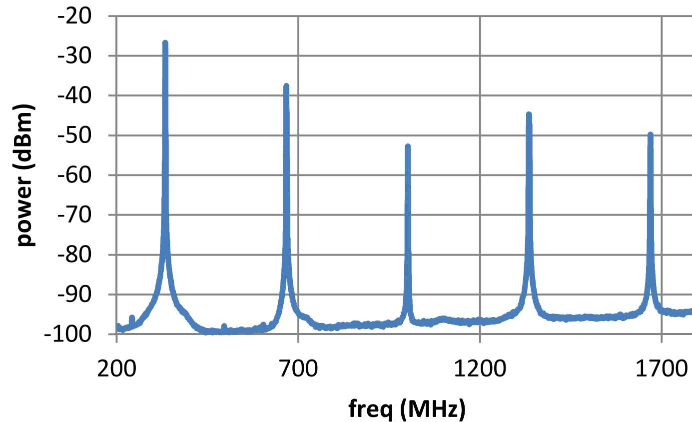
source: the author

7.1.3 Power spectrum

Figure 7.6 shows the power spectrum of the ring using VDD_{RING} = 1.2 V. It is possible to see the fundamental at 333 MHz and the other four harmonics. Figure 7.7 shows the power spectrum using VDD_{RING} = 0.85 V. Comparing these both figures with the ideal (noiseless)

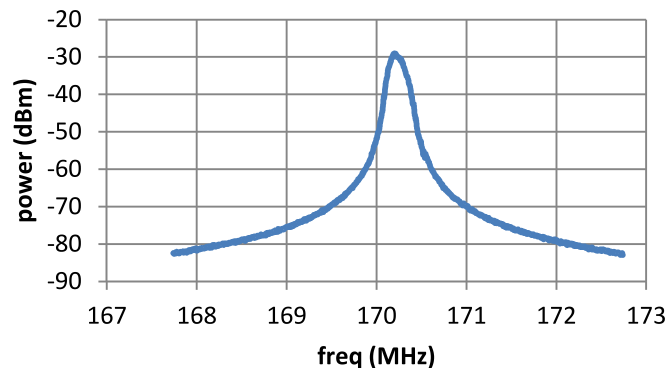
simulated power spectrum of figure 5.20, it is possible to see presence of the phase noise in the real spectrum (*i.e.* the broadening of the output power) .These measurements were done during the investigation of the correct operation of the ring-oscillator.

Figure 7.6 - Power spectrum for VDD_{RING} = 1.2 V (sample # 1)



Source: the author

Figure 7.7 - Power spectrum for VDD_{RING} = 0.85 V (sample # 1)



Source: the author

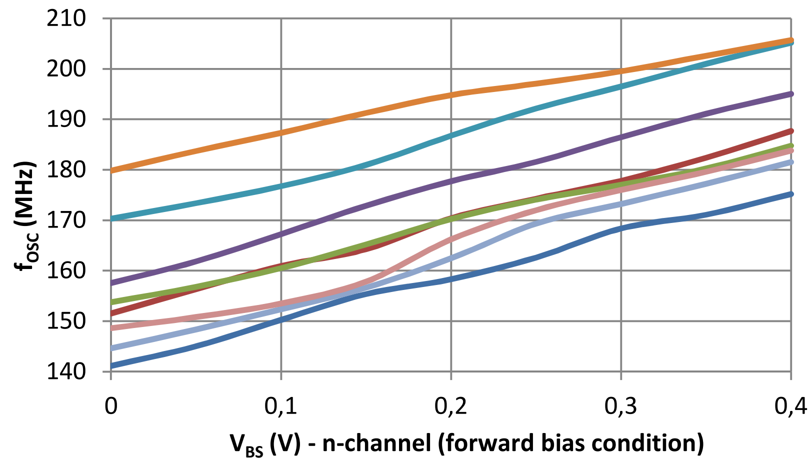
7.1.4 f_{OSC} as a function of bulk bias

Figure 7.8 shows f_{OSC} as a function of the base source voltage for the n-channel devices of the ring oscillator. In this experiment, VDD_{RING} = 800 mV and VDD_{BUFFER} = 750 mV. As can be seen, f_{OSC} practically increases linearly with V_{BS} voltage due to the V_{TH} reduction. The forward bias is applied up to 400 mV and we consider that for this bias condition, there is not significant current flow across the forward PN junction (source and isolated p-well).

F_{OSC} has a average variation of 33.9 MHz for the 400 mV of V_{BS} variation. It means an average variation of 85 kHz/mV. This result is in agreement with the simulated variation *(i.e.* 81 kHz/mV).

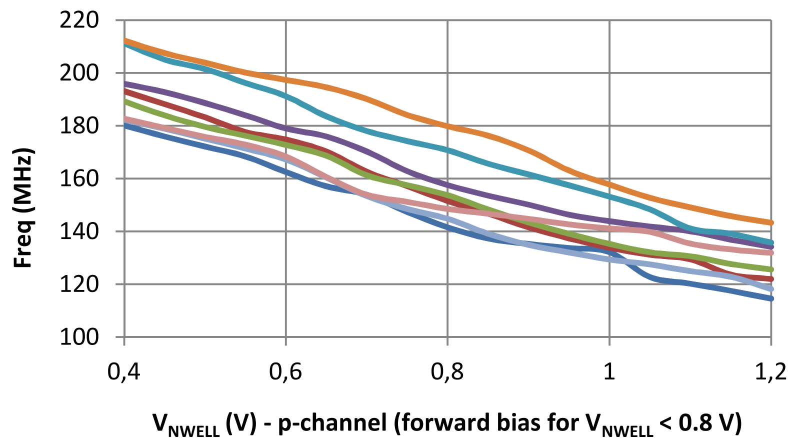
Similarly, figure 7.9 shows f_{OSC} as a function of the nwell voltage (V_{NWELL}) for the p-channel devices of the ring oscillator. Since the supply voltage is 800 mV, V_{NWELL} equal to 800 mV means $V_{BS} = 0$. For $V_{NWELL} = 1.2$ V, a reverse bias of $V_{BS} = +400$ mV is applied for the p-channel devices. For $V_{NWELL} = 0.4$ V, a forward bias of $V_{BS} = -400$ mV is employed. There was an average variation of 65.1 MHz for 800 mV of V_{BS} variation. It means about 81 kHz/mV of variation, also in agreement to the simulation result (85 kHz/mV).

Figure 7.8 - Measured f_{OSC} vs V_{BS} (n-channel) for 8 samples. $VDD_{RING} = 0.8$ V



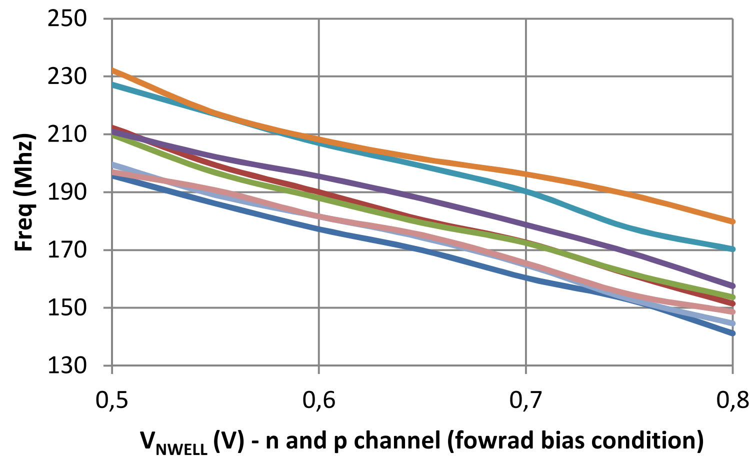
Source: the author

Figure 7.9 - Measured f_{OSC} vs V_{NWELL} (p-channel) for 8 samples ($VDD_{RING} = 0.8$ V)



Source: the author

Figure 7.10 - Measured f_{OSC} vs V_{NWELL} (both bias) for 8 samples (VDD_{RING} = 0.8 V)



Source: the author

Figure 7.10 shows the measured f_{OSC} as a function of V_{NWELL}, but for bulk bias applied for both n- and p-channel devices simultaneously. For instance, for V_{NWELL} = 800 mV and V_{BS} = 0 for both devices. For V_{NWELL} = 500 mV, V_{BS} are equal to + 300 mV and - 300 mV for n-channel and p-channel devices, respectively (both devices are in forward bias condition). There was an average variation of 54.6 MHz for $|\Delta V_{BS}|$ of 300 mV. It means a measured variation of 182 kHz/mV, result in agreement to the simulation (*i.e.* 177 kHz/mV).

All results shown in the above sub-sections show the correct operation of the ring-oscillator and also a good agreement between simulation and measured result, either for the oscillation frequency, as the impact of bulk bias on the ring performance.

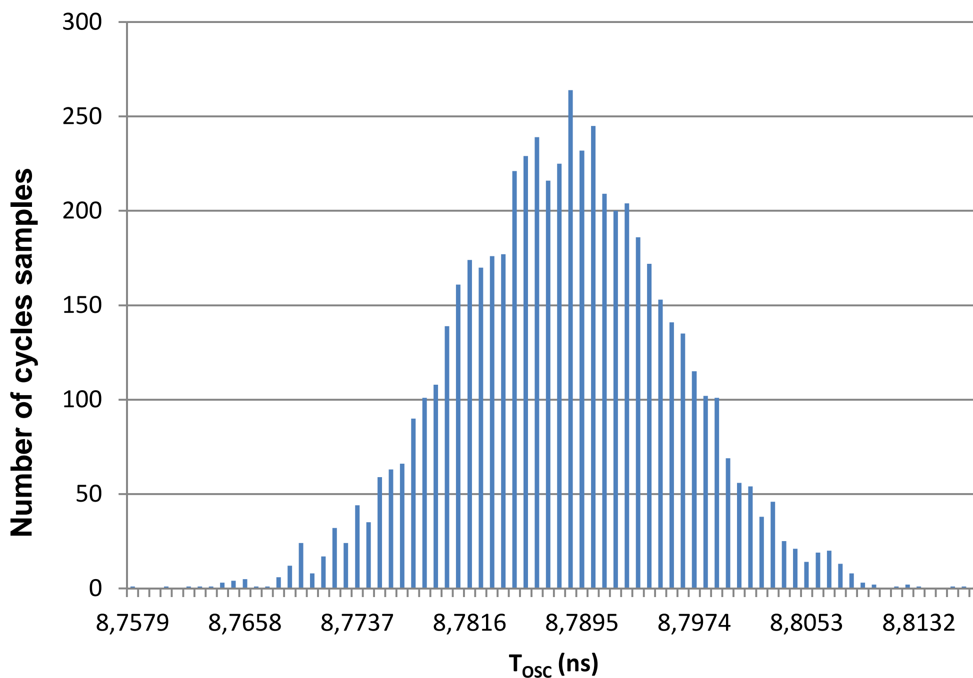
7.1.5 Period Jitter

In order to measure the Period jitter we have used the DSO80304B Infiniium High Performance Oscilloscope (Keysight) that allows the recording of sample values over a time window large enough, as for instance, 50 μs. Measuring a signal with a frequency of about 93 MHz (for VDD_{RING} of 700 mV), more than 4500 cycles will be measured at each save operation. Eventually, we can save data sometimes consecutively and have a large quantity of data. This large amount of data is important because we are interested in the variation of the signal over time. In addition, we need a high sampling rate because the jitter we are going to measure is in the order of ps. This oscilloscope has up to 40 GSa/s sampling rate and it saves time data each 6.25 ps.

Our circuit was supplied by Agilent E3631A Triple output DC power supply. Since its RMS output noise voltage is less than 350 µV accordingly to its manual (from 20 Hz to 20 MHz), the setup seems to be adequate for the jitter measurement.

Figure 7.11 shows the histogram of oscillation period (T_{OSC}) for the ring oscillator sample #5 recorded during 50 µs when it is supplied with 700 mV. In the x-axis is represented the oscillation period while in the y-axis is its frequency of occurrence. An average and (sigma) of T_{OSC} are 8.788 ns and 7.6 ps, respectively. From Chapter 5, note that the standard deviation of T_{OSC} is the Period jitter. The maximum and minimum measured T_{OSC} are 8.817 and 8.761 ns, respectively. It means a total variation ΔT_{OSC} of 55.8 ps (or Δf_{OSC} = 722 kHz). The histogram seems to have a Gaussian distribution and this is expected due to the random nature of device noise.

Figure 7.11 - Measured histogram of T_{OSC} for sample #5 ring (VDD_{RING} = 0.7 V)



source: the author

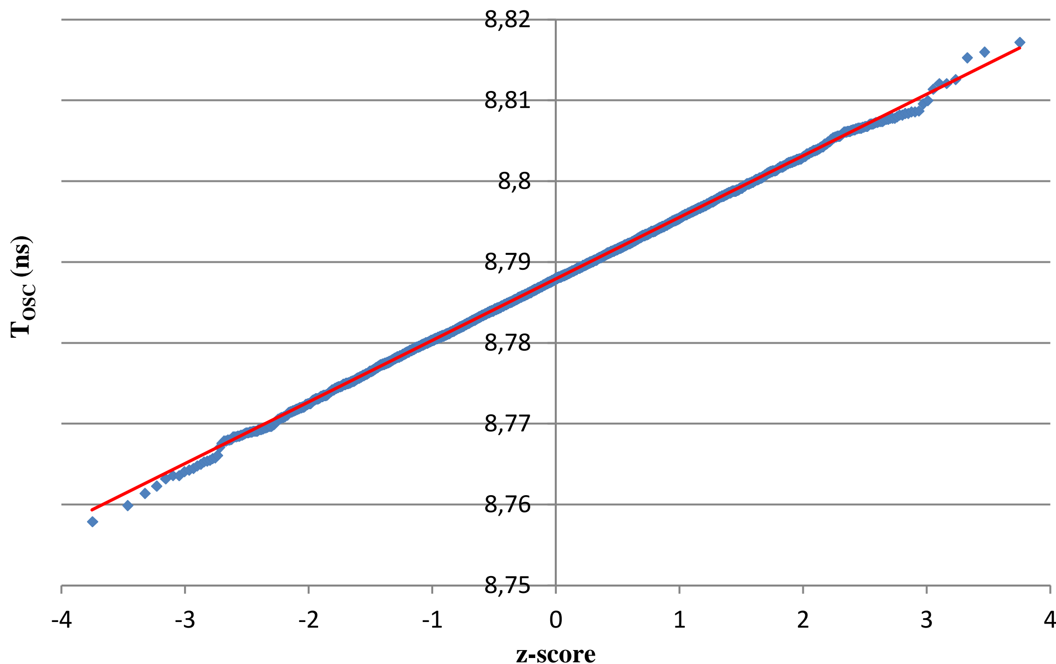
Another way to verify the nature of the data distribution is by means of the Normal Probability Plot shown in figure 7.12. This plot is found by means of the z-score given by equation (7.1.) - when the number of samples is much higher than 10 (LAMOTHE, 2015).

$$z_i = \phi^{-1}\left(\frac{i-0.5}{n}\right) \tag{7.1}$$

Variable "n" is the number of samples, and "i" is 1, 2, 3, ... n. Function ϕ^{-1} returns the inverse of the standard normal cumulative distribution with a mean of zero and a standard deviation of one (*e.g.* "NORM.S.INV" excel function). Data are close to a straight line (red) if they are normally distributed.

As can be seen in figure 7.12, very few data points (at the ends of the curve) depart from the normality, what it is an indication of the variation of T_{OSC} is caused by random noise sources (*e.g.* flicker).

Figure 7.12 - Normal Probability Plot (T_{OSC}) for sample #5 ring (VDD_{RING} = 0.7 V)



Source: the author

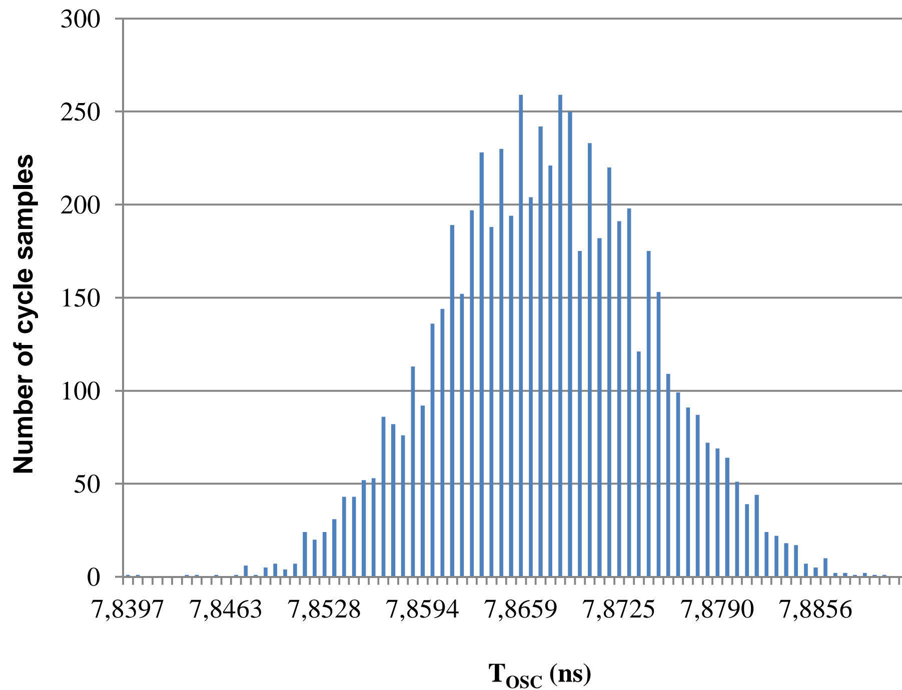
From Chapter 5, the simulated mean and of T_{OSC} are 8.781 ns and 3.7 ps, respectively. This result was obtained through a TRAN noise simulation that considered all noise sources with frequencies higher than 10 kHz. As can be seen, measured T_{OSC} are really near to the simulation results - agreement already shown in figures 7.1 - 7.3.

Figure 7.13 and 7.14 shows the histogram and the normal probability plot for sample #6, respectively. An average and of T_{OSC} are 7.867 ns (~ 127.1 MHz) and 6.9 ps, respectively. The maximum and minimum measured T_{OSC} are 7.892 and 8.843 ns, respectively. It means a total variation (ΔT_{OSC}) of 49 ps (or Δf_{OSC} = 784 kHz).

Similarly to sample #5, most recorded data for sample #6 follows a normal distribution. Only few samples at the ends of this curve depart from the normality.

Regarding the standard deviation (also referred as Period Jitter here), the measured values (7.6 ps and 6.9 ps for samples #5 and #6, respectively) are about twice the simulated one (3.7 ps) - what represents a reasonable agreement between silicon and simulation. We expected that the measured jitter would be greater than the simulated one due the additional noise sources presented in the real circuit.

Figure 7.13 - Measured histogram of T_{OSC} for sample #6 ring (VDD_{RING} = 0.7 V)



Source: the author

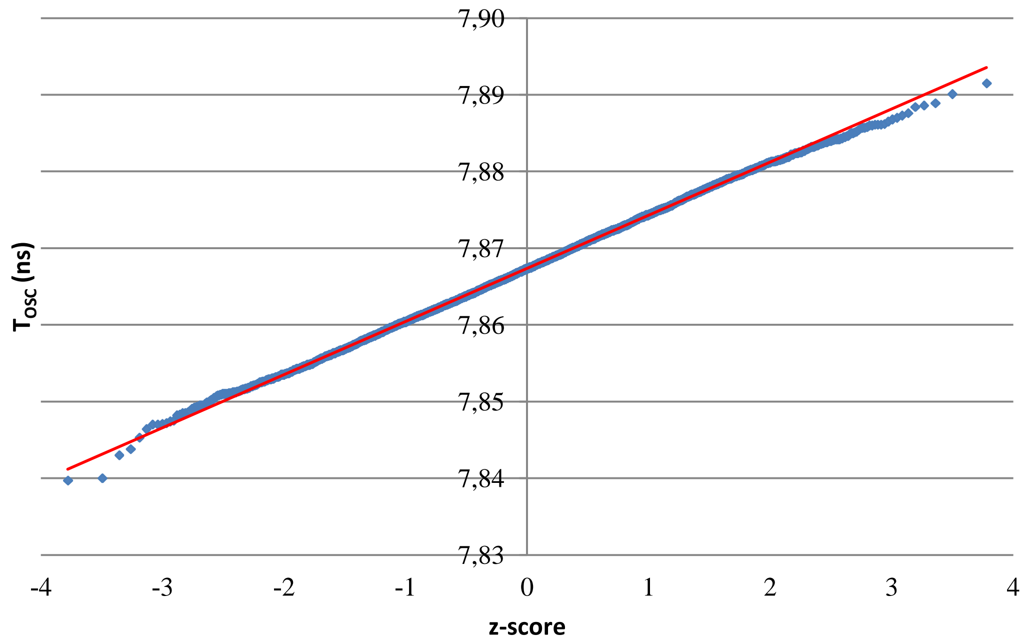
The first additional noise source in our circuit is the supply voltage fluctuation. Although decoupling capacitors (inside the CI) were placed near the ring-oscillator layout, and an external off-chip capacitor was placed next to the integrated circuit, we observed a few milivolts variation of the supply line. From chapter 5, we expected a f_{OSC} variation of 518 kHz for each mV of variation on the supply line. This high sensitivity of F_{OSC} on VDD_{RING} fluctuations increases the measured jitter.

Those few measured samples of T_{OSC} that depart from the normal distribution shown in figures 7.12 and 7.14, may be understood as a result of addition noise sources presented in our circuit (not thermal or flicker noise from our ring-oscillator).

Although figures 7.11 and 7.13 show the histogram of T_{OSC} over a time window of 50 µs, we repeated these measurements many times and compared the mean and sigma of T_{OSC} in order to verify the normal distribution of our data. For instance, the measurement of sample

#5 was done eight times consecutively (*i.e.* total time windows of 400 μs) and the total average and of T_{OSC} are 8.795 ns and 7.5 ps, respectively. The maximum and minimum values of T_{OSC} are 8.829 ns and 8.758 ns.

Figure 7.14 - Normal Probability Plot (T_{OSC}) for sample # 6 ring (VDD_{RING} = 0.7 V)



Source: the author

Table 7.1: Measured Period jitter ( ) for 4 samples

Samples:	**#2**	**#5**	**#6**	**#7**
T_{OSC}: mean (ns)	10.236	8.795	7.875	10.751
T_{OSC}: (ps)	7.8	7.5	6.8	8.4
T_{OSC}: max (ns)	10.305	8.829	7.915	10.792
T_{OSC}: min (ns)	10.163	8.758	7.833	10.699
(f_{OSC_MAX} - f_{OSC_MIN}) (kHz)	1356	918	1323	805
f_{OSC}: mean (MHz)	97.69	113.70	126.98	93.02
/mean (10^{-3})	0.761	0.855	0.866	0.778

Source: the author

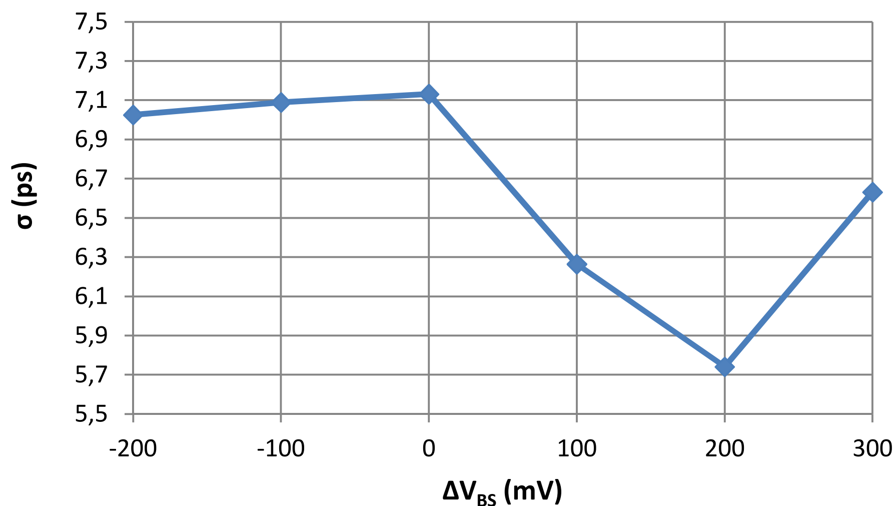
Table 7.1 summarizes the measured Period jitter for 4 samples of the ring-oscillator. As can be seen, these samples have similar jitter performance. Last line of table 7.1 is the ratio of the and the mean values, and it can be understood as comparison parameter because takes into account the oscillation frequency.

7.1.6 Ring-Oscillator Period Jitter as a function of bulk bias

This section shows the measured Period jitter as a function of bulk bias for the ring-oscillator devices. The bulk bias was applied for three bias conditions: (i) solely for the n-channel devices, (ii) solely for the p-channel devices, and (iii) for both devices simultaneously while the $VDD_{RING} = VDD_{BUFFER}$ was 700 mV.

Figure 7.15 shows of T_{OSC} vs ΔV_{BS} when bulk bias is applied only for the n-channel devices. Positive (negative) values of ΔV_{BS} mean forward (reverse) bias condition. V_{TH} decreases in the n-channel transistor with forward bulk bias.

Figure 7.15 - Sigma of T_{OSC} for sample # 5 vs bulk bias for n-channel devices



source: the author

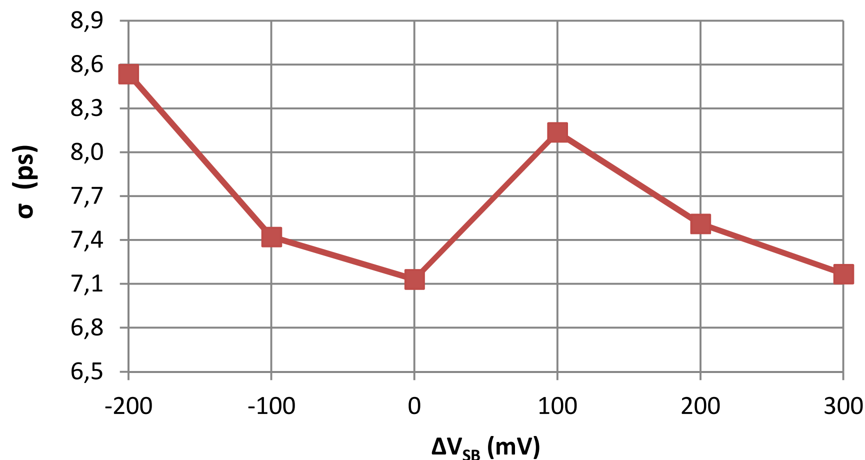
As can be seen, there is a reduction of when forward bulk bias is employed and it is in agreement with the simulation results of section 5.5.1. For $\Delta V_{BS} > 200$ mV, there was an increase of although still lower than the nominal bias condition ($\Delta V_{BS} = 0$). A hypothesis for the increase of for $\Delta V_{BS} = -300$ mV can be generated by some small noise injected in the forward bias PN junction (coming from the source region connected to ground terminal).

For reverse bias conditions,   does not practically change (although it was expected to increase).

Figure 7.16 shows the   of T_{OSC} vs ΔV_{BS} when bulk bias is applied only for the p-channel devices. For positive (negative) values of ΔV_{SB} mean forward (reverse) bias condition. As can be seen ΔV_{SB} slight increases for ΔV_{SB} = 100 mV and then decreases for ΔV_{SB} = 200 mV and ΔV_{SB} = 300 mV. This result qualitatively agrees to the simulated one (using the traditional device flicker noise model) shown in table 5.3.

For the case in which bulk biases are applied for n-channel and p-channel devices simultaneously, there was a significant reduction of the measured . For instance, for ΔV_{BS_NMOS} = ΔV_{SB_PMOS} = 100 mV and 300 mV, the measured   was 6.7 and 4.5 ps, respectively. The largest reduction of simulated   also happens for both bulk bias applied (table 5.3).

Figure 7.16 - Measured   of T_{OSC} for sample # 5 vs bulk bias for p-channel devices



Source: the author

Table 7.2 summarizes all measured data for sample #5 when bulk bias is applied. The Column called "delta (ps)" refers to the difference between the maximum and minimum values of T_{OSC}.

Table 7.2: Measured Period jitter ( ) for sample #5 as a function of bulk bias

NMOS Bulk bias V_{BS}	PMOS Bulk bias V_{SB}	T_{OSC}: mean (ns)	T_{OSC}: (ps)	Delta (ps)	f_{OSC}: mean (MHz)	$/T_{OSC}$ (10-4)
0	0	8.718	7.132	49.8	114.71	8.2
-200	0	10.128	7.026	56.6	98.73	6.9
-100	0	9.488	7.089	55.2	105.40	7.5
100	0	8.224	6.265	43.5	121.601	7.6
200	0	7.756	5.741	42.6	128.939	7.4
300	0	7.481	6.632	48.2	133.667	8.9
0	-200	10.453	8.535	61.8	95.664	8.2
0	-100	9.617	7.422	57.1	103.988	7.7
0	100	8.137	6.018	43.9	122.903	7.4
0	200	7.5108	7.845	63.1	133.142	10.7
0	300	7.168	7.954	61.6	139.517	11.1
100	100	7.626	6.705	46.3	131.129	8.8
300	300	6.013	4.535	33.8	166.298	7.5

Source: the author

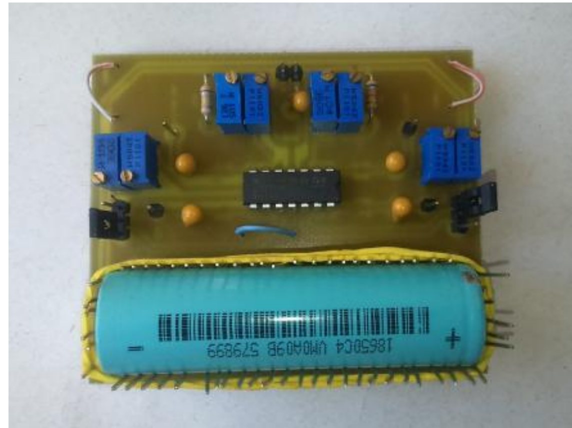
7.1.7 Measured Period Jitter for battery supplied ring oscillator

In order to verify how much the measured jitter was generated by other sources different from the devices noise (flicker and thermal noise), a test board using battery (shown in figure 7.17) was designed. The objective here is the replacement of the Agilent E3631A Triple output DC source and check again the jitter performance.

The battery provides a DC output voltage of 4.2 V and thus, a simply circuit composed by an op-amp configured as unity gain buffer and a resistor divider was used in order to generate the required supply and bulk bias voltages. Some low noise from the op.-amp. (IC LM324)

and the discrete resistors are still expected. The output signals of this board is then connected to our board with the integrated oscillators (figure 6.2).

Figure 7.17 - Test board with battery for the jitter measurement



Source: the author

The jitter performance of sample #2 was re-measured and the jitter performance of both cases were about the same: 7.4 ps and 7.0 ps, using the Agilent power supply and the board test, respectively. For this single sample, there is only a 5% of noise reduction on the measured .

7.1.8 Comments on the Period Jitter calculation

A limitation of our case-study is the data sampling rate of the oscilloscope. It records a data point each 6.25 ps that is in the order of the measured jitter (~ 7.6 ps). As a consequence, there is a measurement error included in our data that cannot be neglected in our analysis.

The jitter calculation starts plotting all points recorded in the time windows of 50 µs. The plotted curve includes an interpolation of the sampled data. After that, a second curve representing a voltage reference was plotted over the first one, as shown in the example of figure 7.18, whose reference was set to zero. After that, the period was calculated by the time difference between points A and B. This calculation was done successively for all points and the standard distribution (jitter) was found.

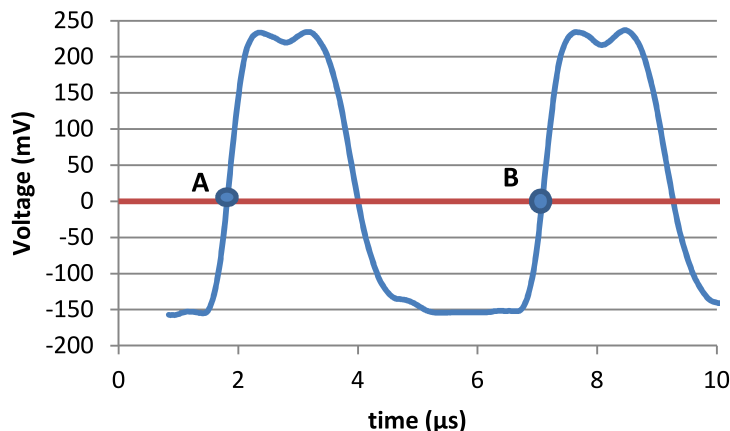
Considering that the rise and fall time of a CMOS inverter can be modeled as a RC system whose voltage and time have a exponential dependency, the interpolation curve tends to be not very different from the real data.

Since the oscilloscope samples data each 6.25 ps, the worst case discrepancy between the real data and the interpolated points (A and B in figure 7.18) is 3.125 ps (center of two consecutive measured points).

If one considers that the error (Δt) between the interpolated points and the real ones follows an Gaussian distribution, its effect should be mitigated for a large set of data (more than 5000 points). It means that Δt can be positive, negative or even equal to zero for the set of data. In addition, if one consider that the interpolate data has some fixed difference between the interpolated data, its effect tends to be mitigated because we are calculating the difference between two consecutive points. However, other errors that are not compensated in our analysis may also exist.

Consequently, although an estimation of the jitter was found, it would be desirable to measured it with a instrument with a higher sampling rate in order to have consistent set of data that supports our conclusions.

Figure 7.18 - Output voltage and reference curve



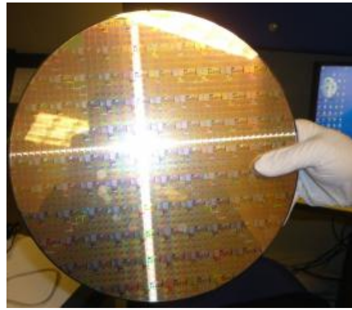
Source: the author

7.2 Oscillators implemented in 45 nm CMOS process

7.2.1 Measurement Setup

The LC-tank and the ring oscillators presented in sections 5.3 and 5.4 were fabricated and planned to be measured directly on wafer shown in figure 7.19.

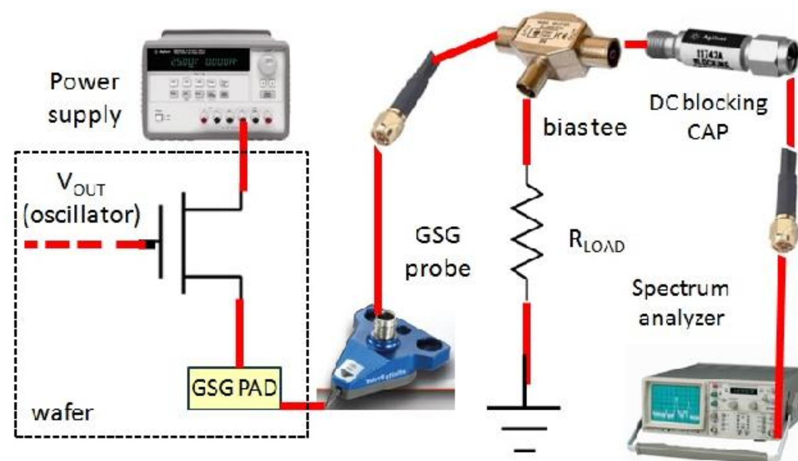
Figure 7.19 - Wafer with the integrated oscillators (45 nm process)



Source: the author

The block diagram of the measurement setup is shown in figure 7.20 and it includes: a resistor load and a bias tee used to bias the output source follower, a spectrum Analyzer (Advantest R3273 of Rohde-Schwarz), power supply, DC and GSG probes.

Figure 7.20 - Block diagram of the measurement setup



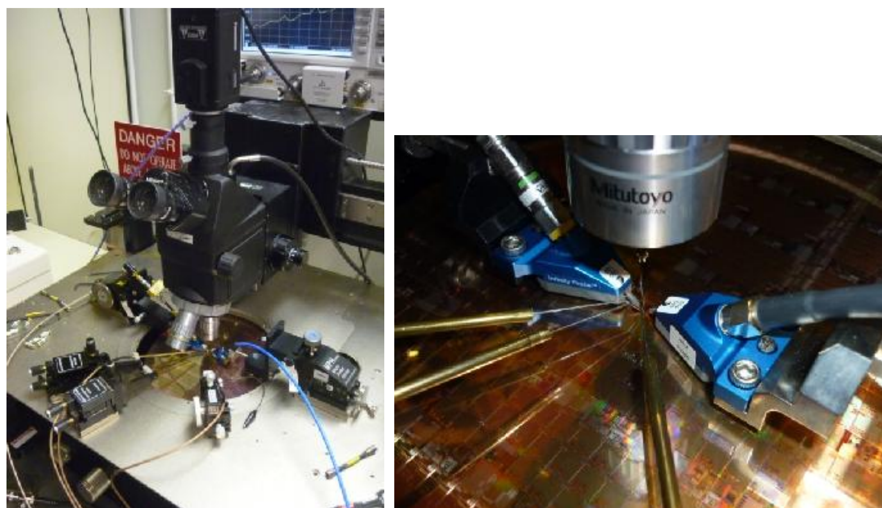
Source: the author

Figures 7.21 and 7.22 show photos of the measurement setup. The goal of this fast bring-up was the verification of circuit functionally and the measurement of power spectrum of the designed oscillators. The setup was not optimized for low-noise measurement.

For the LC-tank oscillators, three DC probes were used. The first one was used to provide the power supply voltage of 1.1 V. The second one was used provide the bias voltage for the current source of the oscillator (see the terminal PAD in figure 5.11). A current of about 5.5 mA is used to bias the oscillator. The third DC probe was used to bias the bulk (p-well and n-well for n-channel and p-channel, respectively) of the g_m-pair transistors. Moreover, two GSG RF probes were used in order to measure the output voltage in a single-ended way.

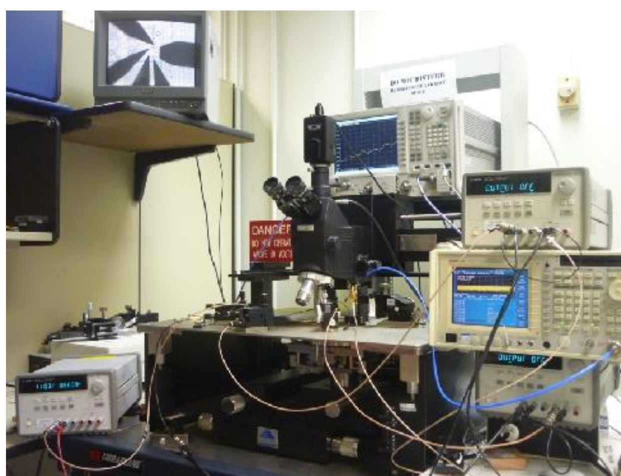
For the ring-oscillator, four DC probes were used. The first and the second ones were used to provide the power supply (0.8 V < vdd < 1.4 V) to the ring and to the output buffer (1. 8 V). The third and forth DC probes were used to bias the bulk of the n-channel and p-channel devices). Finally, a GSG probe was used to measure the output voltage

Figure 7.21- Measurement setup: probe station, DC and GSG probes



Source: the author

Figure 7.22 - Complete setup with power supply and spectrum analyzer



Source: the author

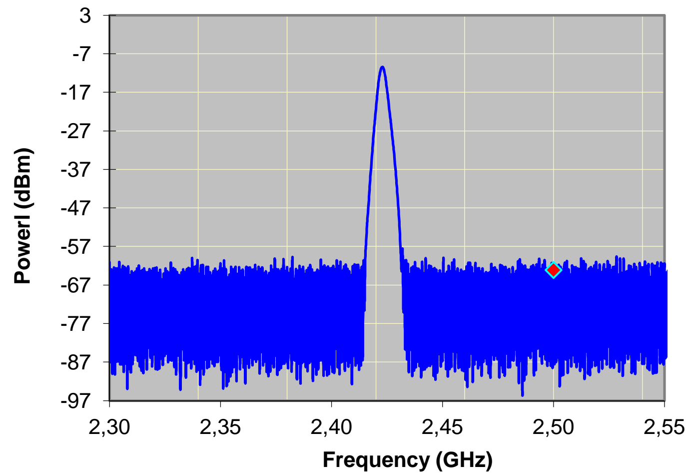
7.2.2 LC-tank oscillators

Figures 7.23 and 7.24 show the measured power spectrum of oscillator OSC_{N3} (Section 5.5.3) with the spectrum analyzer configured with a span of 250 MHz and 10 MHz,

respectively. The g_m-pair of the OSC_{N3} was implemented using digital (core) transistors. Parameters RBW and VBW were set to 100 kHz.

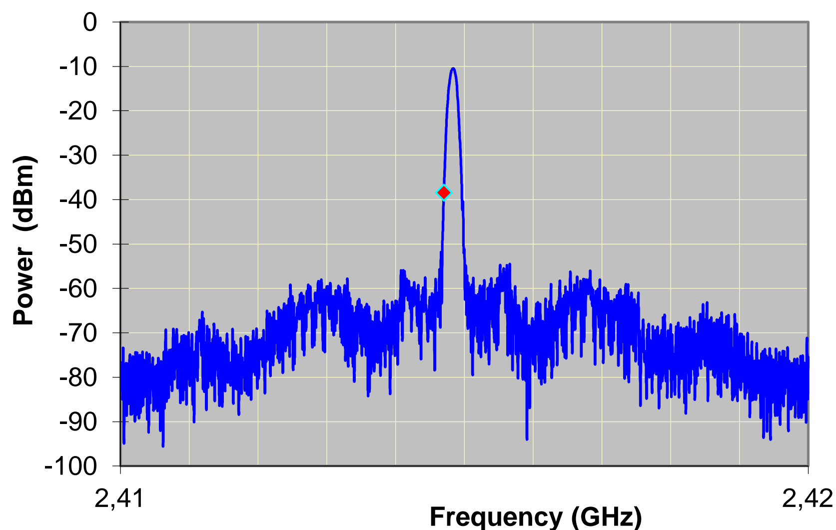
As can be seen in Figure 7.24, the measured oscillation frequency is 2.419 GHz, what agrees to the simulation result (~ 2.5 GHz at nominal process and condition).

Figure 7.23 - Power Spectrum of OSC_{N3} (span = 250 MHz)



Source: the author

Figure 7.24 - Power Spectrum of OSC_{N3} (span = 10 MHz)

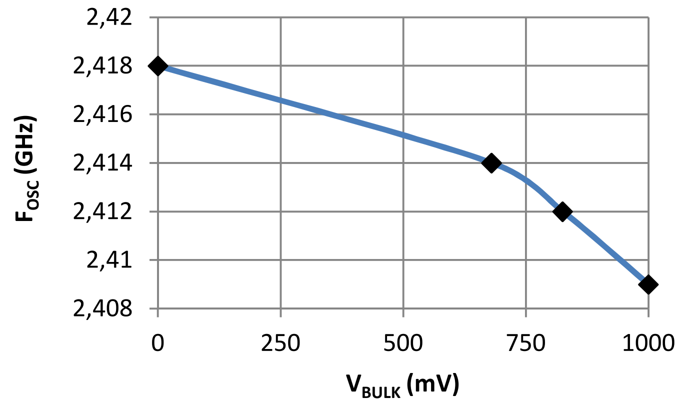


Source: the author

Figure 7.25 shows the oscillation frequency as a function of bulk bias for OSC_{N3}. For V_{BULK} = 0, the source-bulk voltage of the g_m-pair (composed by n-channel transistor) and the

source-bulk PN junction is reverse biased. For V_{BULK} = 825 mV, the source-bulk voltage is negative and the PN junction is forward biased (V_{TH} reduction).

Figure 7.25 - Measured f_{OSC} as a function of bulk bias for OSC_{N3}



source: the author

As can be seen, the impact of bulk bias on the f_{OSC} is small. There as a reduction of about 9 MHz (Δf_{OSC} ~ 0.4 %) for 1 V of variation in the bulk bias. It is totally in agreement with the simulation results (table 5.7). This small reduction of F_{OSC} when applying forward bulk bias is caused by the reduction of the transistor depletion width and an increase in the depletion charge capacitance.

Oscillator OSC_{N1} was implemented using analog-friendly devices in the g_m-pair. The measured oscillation frequency is 2.480 GHz (V_{BULK} = 0) what is near to the simulation results (~ 2.5 GHz). Moreover, F_{OSC} = , 2.479 GHz, 2.477 GHz and 2.474 GHz for a bulk bias of 680 mV, 825 mV and 1000 mV, respectively. The oscillation frequency variation was only 6 MHz for 1 V of bulk bias variation .

Figure 7.26 - Measured oscillation frequency for OSC_{N1}

source: the author

Figure 7.26 shows a photo of the spectrum analyzer when V_{BULK} = 1000 mV is applied. For this bias condition, note that the marker is showing f_{OSC} = 2.474 GHz.

Finally, using the power spectrum data shown in figure 7.24 and equation 3.4 (Chapter 4), it would be possible to calculate the phase noise of OS_{CN3}. However, if our data is used, a phase noise much worse than the simulation results is found. One of the reasons this performance is because our setup not optimized to low noise measurements. Some recommendations that would improve our measurement are:

(i) Increase the buffer power consumption (decrease R_{LOAD}),

(ii) Use a chamber in order to protect the wafer from the incidence of light (and the generation of minority carriers),

(iii) Decrease to the lowest possible value the RBW:VBW (*e.g.* ~ 1 kHz)

(iv) Supply the circuit through batteries.

7.2.3 Ring-Oscillator

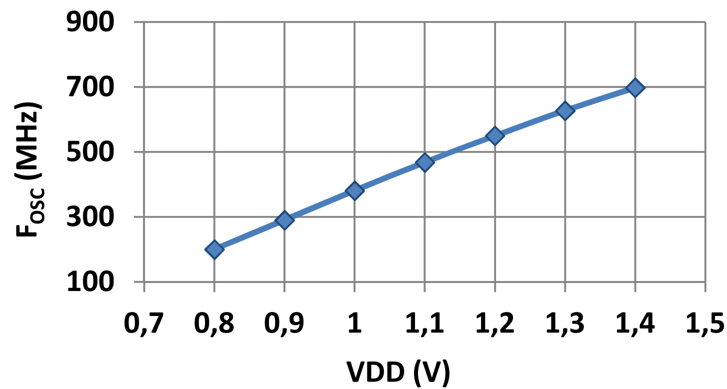
The measured oscillation frequency of the ring-oscillator biased with a supply voltage of 1.1 V is 468 MHz. The simulated f_{OSC} for this bias condition and nominal process is ~ 666 MHz (section 5.3). Therefore, the resistance and capacitance parasites seem to be worse than those given by the simulator extraction. The transistor threshold voltage and carrier mobility also may be larger and lower, respectively.

Figure 7.27 shows the measured f_{OSC} as a function of supply. A total measured variation of about 826 MHz/V was observed. This value is smaller than the simulation results (~ 1.2 GHz/V). Figure 7.28 shows a photo of the spectrum analyzer showing the measured f_{OSC} for VDD = 1.3 V.

Comparing figures 7.26 and 7.28, it is possible to see that power spectrum of the ring-oscillator is much more noisy than that of the LC-tank, what it is in agreement with our expectation.

Figure 7.29 shows f_{OSC} as a function of bulk bias for the ring-oscillator. In this measurement, the bulk bias is varied simultaneously for the n-channel and p-channel devices. The bulk-bias for n-channel (p-channel) increases (decreases) while the VDD is kept constant at 1.3 V.

Figure 7.27 - Measured f_{OSC} as a function of supply for the ring-oscillator

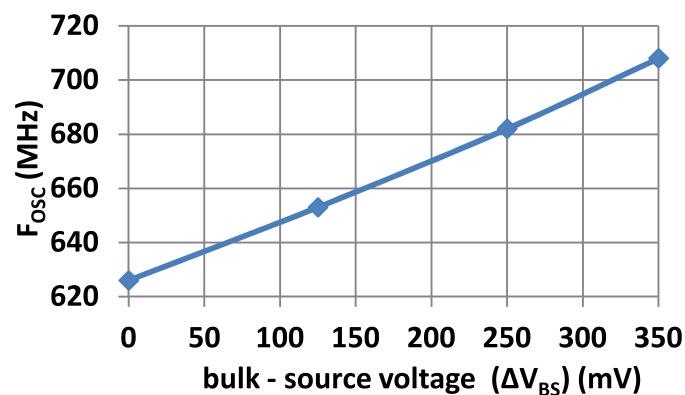


source: the author

Figure 7.28 - Measured f_{OSC} for $VDD_{RING} = 1.3$ V for the ring-oscillator

source: the author

Figure 7.29 - Measured f_{OSC} as a function of V_{BS} for the ring oscillator



Source: the author

The three bias conditions employed in figure 7.29 are: (i) $V_{BS} = 0$ (no bulk bias), (ii) $V_{BULK} = 125$ mV (n-channel) and $V_{NWELL} = 975$ mV (p-channel), (iii) $V_{BULK} = 250$ mV and

V_{NWELL} = 850 mV, and (iiii) V_{BULK} = 350 mV and V_{NWELL} = 750 mV. A total variation in f_{OSC} of ~ 82 MHz was obtained.

7.3 Conclusions

Considering the ring-oscillator implemented in 130 nm CMOS process, there was a good agreement between silicon and simulation results regarding the oscillation frequency and its dependency on supply voltage and bulk bias voltages. This agreement was verified in 8 measured samples and the average f_{OSC} is 103.4 MHz when the ring-oscillator is supplied with 700 mV.

The average oscillation frequency variation caused by supply voltage and bulk bias variation are 495 kHz/mV and 81 kHz/mV, respectively. The bulk bias can be used as frequency tune voltage when fine tuning is needed. It allows a 6 times more precise control of the oscillation frequency than the supply voltage. On the other hand, the supply voltage can be used to achieve a wide tuning range.

The Period jitter measured in 4 samples is less than 10 ps as we expected. The average measured jitter is 7.6 ps and the average worst case variation between the maximum and minimum oscillation frequency is about 1 MHz in a time windows up to 400 μs.

The measured jitter is about twice the simulated value (3.7 ps) and one of the reasons is probably the additional noise sources (not only flicker and thermal device noise) presented in our case-study. One of these additional sources of jitter is the small fluctuation of the supply lines.

Nevertheless, based on the histogram and the normal probability plot, we can see that the majority data of measured oscillation period follows a normal distribution. There were only few points at the ends of the curve that departs from the normality. It seems that the most part of the measured jitter is generated by random noise sources (*i.e.* thermal noise, shot noise and flicker noise) that follow a Gaussian distribution, and thus, it can be defined by the mean and sigma of that Gaussian distribution.

It seems that determinist jitter is not the dominant source of jitter in our case-study. The determinist jitter caused by, for instance, cross-talk and impedance mismatch effects and so on, are not random and do not follow any predictable distribution.

The Period jitter dependency on the bulk bias voltage was also investigated. A reduction of jitter caused by the bulk forward bias of n-channel devices was observed and it was predicted in our simulations. Moreover, the bulk forward bias of p-channel devices results in an initial small increment of the jitter followed by a slight reduction - also seen in the simulations. It provides us a reasonable qualitative estimation regarding the behavior of the jitter as a function of bulk bias.

Although a qualitative agreement of silicon and simulation regarding the impact of bulk bias on the jitter was found, it was not possible to develop a consistent and qualitative conclusion regarding this dependency. The first reason is because the jitter was measured in only four samples and its dependency on bulk bias was verified in a single sample. The second one is the limited sampling rate of the measurement equipment used in this work. The measured jitter is in the same order of the oscilloscope data rate acquisition.

The third reason is those few points out of the normality observed in our analysis. As discussed earlier, it means an additional and undesired noise source presented in our case-study. In order to improve our measurement, and then achieve a consistent set of data regarding the impact of bulk bias on jitter, the following recommendations are given:

(i) Design a single test board with the battery as close as possible to the integrated circuit. Place the discrete decoupling caps in the supply line under (bottom layer) the integrated circuit in order to decrease its RC constant and then minimizing the supply voltage fluctuation. Improve the ground plane, and eventually provide a shield isolation for the entire test board (a metal box connected to ground).

(ii) Separate the ground pins of the output buffer and the ring oscillator in order to avoid any voltage drop and noise coupling between these lines. Although our circuit have different supply voltage pins for the ring and output buffer, the ground pin was shared. It was observed a small (not null) impact of the buffer supply voltage on the oscillation frequency - what it is not desired. It happens because the ground lines is shared and not configured in a star connection. It is desirable to totally eliminate this effect. If the output buffer were redesigned, it could also help the reduction of this dependency.

(iii) In order to help the isolation of the jitter caused by device noise and supply voltage fluctuations, a second version of the ring-oscillator can be designed. A current source and a capacitor can be placed between the supply line and ring-oscillator (source terminals of p-channel transistors). In this case, the sensitivity of the oscillation frequency on the supply

voltage will be drastically reduced. The current source can be designed with wide and long channel transistors in order to decrease its flicker noise contribution to the output jitter.

Regarding the LC-tank oscillator implemented using 45 nm process, there was also a good agreement between silicon and simulations regarding the oscillation frequency and its dependency on the bulk bias voltages.

The measured oscillation frequency for the oscillator with the g_m-pair implemented using n-channel digital transistors is 2.419 GHz. The variation of f_{OSC} considering 1 V of variation on the bulk bias voltage is only $\sim 0.4\ \%$. This is useful case-study in our investigation of the impact of bulk bias on jitter because the oscillation frequency is not significant impacted when bulk bias is applied.

8 CONCLUSIONS

This work focus on two challenges faced by analog integrated circuits designers when using modern CMOS process: Total ionizing Dose and flicker noise of circuits under cyclo-stationary operation. The first two chapters discuss the main important concepts regarding these two topics.

Chapter 2 reviews the state of art literature regarding TID. The physical process, the impact of TID on the performance of general integrated circuits, the impact of scaling on the radiation effects, radiation hardening techniques, and the impact of TID on integrated voltage references were presented and discussed.

Chapter 3 reviews the state of art regarding flicker noise of integrated circuits under cyclo-stationary operation. The physical process, the effect of forward bulk bias during the off-state operation, the simulation tools used to estimate the impact of flicker noise in analog circuits were discussed. Moreover, basic concepts of jitter and phase noise were also presented.

Regarding the TID effects, it was found that the impact of radiation was similar or more severe than the fabrication process effects for most of the case-study circuits. Only for traditional P_{TAT} current reference (I_{PTAT}) and the simple V_{TH0}-Based reference (V_{REF_3}), the TID effects were lower than the fabrication process.

For the bandgap reference (V_{REF_1}), TID effects result in a variation of the output voltage of 5.5 %, while the total variation caused by the fabrication process was 4.8%. If we consider these two error sources are uncorrelated, the total error of V_{REF_1} considering fabrication process and TID effects is 7.3 %. For this circuit, the PNP BJT device was probably the main responsible for the voltage reference variation during irradiation process.

For the V_{TH0}-based V_{REF_4} circuit the TID effects were about 3 times worse than the impact of fabrication process. While the total variation caused by the mismatch effects were about 4.7%, TID effects results in an output variation of 15%.

The Bandgap-based V_{REF_7} and V_{REF_8} circuits implemented using thick-oxide transistors were also very degraded by the TID effects (about 12 % of variation). We expected this behavior because these circuits were implemented using thick-oxide transistors (more susceptible to TID than thin-oxide transistors). For these topologies, the self-cascode transistors using the minimum channel length were probably the mean responsible for the output variation.

In summary, a complete discussion regarding the impact of fabrication process and impact of TID were provided for 10 cases-study. The IC design, simulation methodology and the integrated circuit characterization were presented. All the results obtained in this work are useful in the prediction of the TID effects in the majority voltage references circuits available in state-of-art literature. Moreover, some recommendations regarding how mitigating the impact of TID effects on the performance of these circuits were also provided.

Regarding the flicker noise of circuits under cyclo-stationary operation, the oscillation frequency and its dependency on the bulk bias voltage were investigated. There was a good agreement between the simulation and silicon for the LC-tank implemented using 45 nm process and the ring-oscillator implemented using 130 nm process.

Considering the LC-tank, the measured oscillation frequency is 2.419 GHz for the oscillator using g_m-pair implemented by means of n-channel digital transistors. The variation of f_{OSC} considering 1 V of variation on the bulk bias voltage is only ~ 0.4 %. This small variation of f_{OSC} when applying forward bulk bias is caused by the reduction of the transistor depletion width and an increase in the depletion charge capacitance. This small variation of f_{OSC} when applying bulk bias makes this circuit an useful case-study in the investigation of the impact of bulk bias on jitter performance. Since jitter is a function of the oscillation frequency, it makes easier the jitter investigation because the oscillation frequency is not significantly changed for the different bias conditions.

Considering the ring-oscillator, the average oscillation frequency for 8 samples is 103.4 MHz when the circuit is supplied with 700 mV. The average oscillation frequency variation caused by supply voltage and bulk bias variation are 495 kHz/mV and 81 kHz/mV, respectively. The bulk bias can be used as frequency tune voltage when fine tuning is needed.

The Period jitter measured in 4 samples is less than 10 ps, as expected. The average measured jitter is 7.6 ps and the average worst case variation between the maximum and minimum oscillation frequency is about 1 MHz in a time windows up to 400 µs. The measured jitter is about twice the simulated value (3.7 ps) and one of the reasons of this discrepancy is probably the additional noise sources (not only flicker and thermal device noise) presented in our case-study.

The jitter as a function of bulk bias was investigated for the ring-oscillator and the obtained result agrees qualitatively with the simulation results. It was not possible to develop a consistent conclusion regarding the relation between jitter and bulk bias due to limited

number of characterized samples, the additional noise presented in our data and the limited accuracy of the measurement equipment (jitter is in the order of oscilloscope sampling rate). However, recommendations of how improving our measurement setup and case-study were provided.

A complete investigation of jitter was presented. The design of the integrated oscillators, simulation methodology and silicon characterization were presented. This work is an important step in the development of new flicker noise models - project been carried out in our university.

Finally, we summarizes the main contributions of this thesis:

(1) Design of integrated voltage reference circuits using 130 nm CMOS process aiming the characterization of TID effects,

(2) Estimation of the impact of TID on the performance of the design voltage reference circuits (Both, 2013).

(3) Silicon characterization of TID and fabrication process effects on the designed circuits.

(4) Design of integrated oscillator circuits with ring and LC-tank topologies using 45 nm and 130 nm CMOs processes aiming the characterization of flicker noise under cyclo-stationary operation.

(5) Investigation of the impact of bulk bias on the simulated phase noise and jitter performance for the designed oscillators.

(6) Silicon characterization of Period jitter for the ring-oscillator designed in 130 nm CMOS process.

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ANEX A: DESIGN METHODOLOGY USING INVERSION COEFFICIENT

Other activity developed in this thesis was the employment of a design methodology using the Inversion Coefficient proposed by (BINKLEY, 2008) for the sizing process of low voltage and low power voltage references. Design methodologies are useful because it makes possible the reduction of the cycle time of the analog design process and enable the designer to explore different design options quickly while evaluating their tradeoffs (STEFANOVI, 2008) and (SILVEIRA, 1996).

An analog design methodology that provides good insight leading towards optimized design is the selection of the inversion coefficient (IC) of MOS transistors (BINKLEY, 2008). The inversion coefficient is a numerical measure of the channel inversion, which depends on the applied bias voltage at the MOS terminals. In other words, the IC is a normalized number that is proportional to the quantity of free carriers in the channel region. The selection of the IC enables design within weak, moderate or strong inversion operation. Transistors operating in weak and moderate inversion are important for low voltage and low power applications due to their low drain source saturation voltage (V_{DSAT}) and high transconductance efficiency (g_m/I_D). Using simple equations motivated by the EKV MOS model (ENZ, 1995), the method proposed by (BINKLEY, 2008) guides the designer in the manual selection of bias currents and transistor sizes, resulting in an optimized design.

This section shows a transistor-level design methodology for voltage references that uses the selection of the inversion coefficient. For this objective, we chose circuit V_{REF_4} as a case-study and we present the equating of the key transistors of this circuit. The proposed method, used as initial design guidance, reduces the design time and minimizes the number of required simulations (COLOMBO, 2010) and (COLOMBO, 2011).

As mentioned early, IC provides a numerical representation of the MOS inversion level. Weak inversion corresponds to $IC < 0.1$, while moderate inversion corresponds to $0.1 < IC < 10$. For $IC > 10$, MOS transistors are operating in strong inversion (BINKLEY, 2008). In weak inversion, the transport of carriers in the channel is dominated by diffusion; while in strong inversion, the prevailing transport mechanism is drift (TSIVIDIS, 2010).

Equations (A.1) – (A.5) that describes IC as a function of drain-source current (I_{DS}), transistor aspect ratio ($S = W/L$) and the specific current I_0 (a technology and transistor-type dependent current) (BINKLEY, 2008). Note that parameters N_{SUB}, , μ_0, C_{OX} can be extracted from the BSIM model provided by the foundry. Parameter n_0 is the substrate factor

which represents a loss of coupling efficiency between the gate and channel caused by the substrate or body, which acts as a back gate.

$$IC = I_{DS}/I_0 \cdot S \quad (A.1)$$

$$I_0 = 2 \cdot n_0 \cdot \mu_0 \cdot C_{OX} \cdot U_T^2 \quad (A.2)$$

$$n_0 = 1 + \gamma/\left(2 \cdot \sqrt{\Psi_0 + (V_{GS} - V_{TH})/n + V_{SB}}\right) \quad (A.3)$$

$$\psi_0 \approx 2 \cdot \phi_F + 4 \cdot U_T \quad (A.4)$$

$$\emptyset_F = U_T \cdot \ln(N_{SUB}/n_i) \quad (A.5)$$

IC, S and n_0 are dimensionless quantities. C_{OX} is the gate oxide capacitance (fF/µm^2),   is the body-effect factor (V$^{1/2}$), $_0$ is psi parameter (V), N_{SUB} is the substrate doping concentration (cm^{-3}), I_0 is the technology current (A), μ_0 is the low-field mobility (cm^2/V.s), U_T is thermal voltage (mV), V_{SB} is the source bulk voltage (V), $_F$ is the Fermi Potential (V), and n_i is the silicon intrinsic carrier concentration (cm^{-3}) (~1.5*10^{10} @ 300k). Table A.1 shows the process parameters for the 130 nm CMOS process used in this thesis.

Table A.1: Process parameters for the used 130 nm CMOS process

	NMOS	PMOS	Unit
I_0	633	154	nA
n_0	1.07	1.22	-
t_{OX}	3.12	3.35	nm
u_0	440	94	cm^2/V.s
C_{OX}	11.1	10.0	fF/µm^2
V_{TH0}	0.113	-0.236	V

Source: the author

The substrate factor "n" in weak inversion is normally expressed by the weak inversion or subthreshold swing, S, and it is given by equation (A.6) (BINKLEY, 2008). S represents the increase in the gate-source voltage for a factor-of-10 increase in drain current. The weak inversion swing is roughly 80 mV/dec at room temperature (300 K) (RAZAVI, 2001). Note that equation (A.2) shows the substrate factor with sub index "0" that means at moderate

inversion condition. Substrate factor has a small dependency of the inversion level (BINKLEY, 2008), but it can be roughly considered constant in our hand calculations.

$$S = \ln(10) \cdot n \cdot U_T \approx 2.3 \cdot n \cdot U_T \quad \text{(A.6)}$$

The objective of equations proposed in (BINKLEY, 2008) is the possibility to sizing of all transistors of the circuit by means a proper choice of the inversion level. The design procedure starts by choosing the inversion coefficient for the transistors. Therefore, by means of equations (A.7) and (A.8), it is possible to calculate the transistor width and the transistor area for a given I_{DS}, IC and L. All following equations are only valid for saturation mode.

$$W = (L/IC) \cdot (I_{DS}/I_0) \quad \text{(A.7)}$$

$$W \cdot L = (L^2/IC) \cdot (I_{DS}/I_0) \quad \text{(A.8)}$$

Equation (A.9) gives the transconductance efficiency (g_m/I_{DS}) measured in 1/V or µS/µA. The transconductance efficiency is maximum in weak inversion, decreases modestly in moderate inversion and continues dropping in strong inversion (BINKLEY, 2008). Note that if we assumes IC very small (*e.g.* IC = 0.1 - deep weak inversion), g_m/I_{DS} is approximately $1/(n \cdot U_T)$. As a result, by means of g_m/I_{DS} in deep weak inversion, it is possible to have an estimation of "n".

$$g_m/I_{DS} = 1/\left[n \cdot U_T \cdot \left(\sqrt{IC + 0.5 \cdot \sqrt{IC} + 1}\right)\right] \quad \text{(A.9)}$$

Equation (A.10) gives the value of effective gate source voltage, $V_{EFF} = V_{GS} - V_{TH}$ as a function of IC. Equation (A.10) approaches (A.11) for weak inversion.

$$V_{EFF} = 2 \cdot n \cdot U_T \cdot \ln\left(e^{\sqrt{IC}} - 1\right) \quad \text{(A.10)}$$

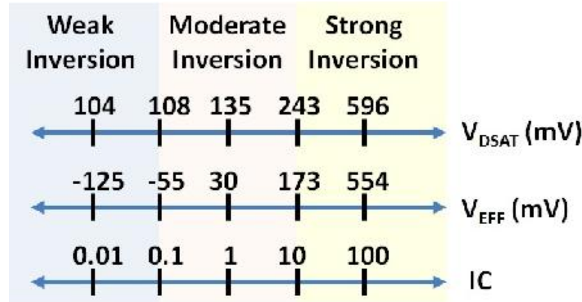
$$V_{EFF} = n \cdot U_T \cdot \ln(IC) \quad \text{(A.11)}$$

Equation (A.12) gives the drain source saturation voltage V_{DSAT}. Note that (A.12) approaches $4 \cdot U_T$ (*e.g.* 100 mV @ 300 K) in weak inversion and $2 \cdot U_T \cdot \sqrt{IC} = V_{EFF}/n$ in strong inversion. Equation (A.12) is very useful for the design of low-voltage circuits since it gives the boundary between the triode and saturation region in terms of the inversion level. This equation can be used to estimate the minimum supply required by voltage references to work properly.

$$V_{DSAT} = 2 \cdot U_T \cdot \sqrt{IC + 0.25} + 3U_T \quad \text{(A.12)}$$

Figure A.1 shows the calculated values of V_{EFF} and V_{DSAT} using equations (A.10) and (A.12), respectively. For IC = 1, NMOS transistors are working in the middle of moderate inversion, V_{DSAT} is 135 mV and V_{GS}-V_{TH} is 30 mV.

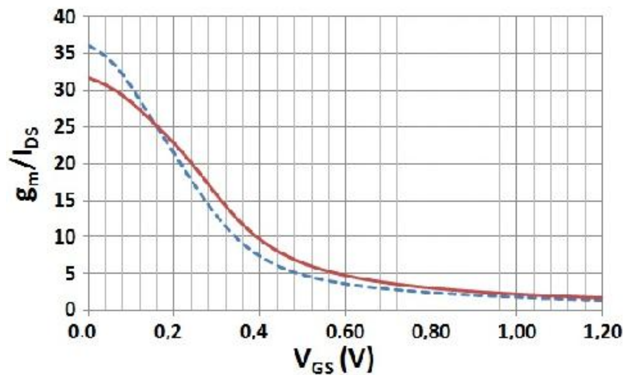
Figure A.1 - V_{DSAT} and V_{EFF} as a function of IC



Source: the author

Figure A.2 shows the simulated g_m/I_{DS} for a 10 μm/10 μm NMOS (dotted line) and PMOS (line) in the 130 nm CMO process. For V_{GS} = 0, g_m/I_{DS} is equal to 36 and 31.7 for the NMOS and PMOS devices, respectively.

Figure A.2 - Simulated g_m/I_{DS} for NMOS (dotted line) and PMOS (line)



Source: the author

In order to start the design procedure for our study-case V_{REF_4}, designers traditionally would use equation (4.6) for devices in weak inversion and equation (4.42) for devices in strong inversion. Parameter models the channel length modulation phenomenon. In order to have very low voltage operation, all devices of V_{REF_4} should operate in weak or moderate inversion. Devices in strong inversion requires high values of V_{DSAT}.

$$I_D = (1/2) \cdot \mu_0 \cdot C_{OX} \cdot S \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \tag{A.13}$$

The use of equation (4.35) in order to calculate the transistor width allows a more conscious choice of the level of MOS inversion than the traditional approach: equations (4.6) and (A.13).

The design procedure starts with the design of PTAT I_{BIAS} generator circuit composed by devices P_{1-3}, P_{8-10} and N_{1-4}. More specifically, we start choosing proper values of IC for devices N_4 and N_3. The difference between the gate-source voltage of N_4 and N_3 defines the temperature coefficient of I_{BIAS}.

In order to have a linear PTAT I_{BIAS}, N_4 and N_3 should operate in weak inversion and their IC should be less than 0.1. Moreover, taking into account that these devices must have a good layout matching, it was assumed $IC_{N3}/IC_{N4} = 5$ for equal currents ($I_{DS_N3} = I_{DS_N4}$). Equations (A.14) and (A.15) shows ΔV_{GS} and I_{BIAS} as a function of inversion coefficient, if one neglects the body effects of N_3.

$$\Delta V_{GS} = n \cdot U_T \cdot \ln(IC_{N3}/IC_{N4}) \quad (A.14)$$

$$I_{BIAS} = \Delta V_{GS}/R_1 \quad (A.15)$$

Equation (A.14) was developed using equation (A.11) since both devices are in weak inversion operation. By means of (A.15), resistor R_1 and I_{BIAS} can be calculated based on the power-consumption requirement.

The dimensions of P_1, P_2 and P_3 were considered to be equal in order to provide good layout matching. These devices can operate in the highest level of IC that is allowed by the low-supply voltage requirement. The variability of I_{DS} in strong inversion is lower than in weak inversion, and therefore, current mirrors should be designed, if possible, in strong inversion operation. Reduced transistor variability is desirable because the accuracy of V_{REF_4} depends on a good matching of key transistors.

Equations (A.16) and (A.17) shows the minimum supply voltage dependency for the I_{BIAS} circuit generator. The minimum supply voltage of the bias circuit for V_{REF_4} is the largest value of $VDD_{MIN,1}$ and VDD_{MIN_2}.

$$VDD_{MIN,1} = \Delta V_{GS(N3-N4)} + V_{DSAT_N4} + V_{SG_P9} + V_{SG_P2} \quad (A.16)$$

$$VDD_{MIN,2} = V_{GS_N3} + V_{GS_N1} + V_{DSAT_P8} + V_{DSAT_P1} \quad (A.17)$$

That is, by means of $VDD_{MIN,1}$ and VDD_{MIN_2}, and equations (A.10) and (A.12), that describes V_{DSAT} and V_{EFF}, it is possible to find the maximum IC for devices P_1, P_2 and P_3 for the required minimum supply voltage operation (*i.e.* we defined 800 mV at typical process).

The low values of V_{DSAT} for transistor operating in the middle of moderate inversion (e.g. $V_{DSAT} < 150$ mV) are suitable for our supply voltage specification. IC around ~ 0.5 were chose for the current mirror transistors. Moreover, in order to decrease the effects of channel length modulation, transistor length should be large and it was chose to be 5 µm in this design.

Moreover, it is well known that the effects of mismatch and flicker noise on transistor performance are roughly given by (A.18) – (A.21) (KINGET, 2005) and (RAZAVI, 2001):

$$\sigma(\Delta V_{TH}) = A_{VTH}/\sqrt{W \cdot L} \quad \text{(A.18)}$$

$$\sigma(\Delta\mu \cdot C_{OX} \cdot W/L)/(\mu \cdot C_{OX} \cdot W/L) = \sigma(\Delta\beta)/\beta = A_K/\sqrt{W \cdot L} \quad \text{(A.19)}$$

$$\sigma(\Delta I_{DS}/I_{DS})^2 \cong (\sigma(\Delta\beta)/\beta)^2 + (g_m/I_{DS})^2 \cdot \sigma^2(\Delta V_{TH}) \quad \text{(A.20)}$$

$$V_n^2 = K_F/(C_{OX} \cdot W \cdot L \cdot f) \quad \text{(A.21)}$$

Parameters (V_{TH}), $\sigma(\Delta\mu \cdot C_{OX} \cdot W/L)$ and V_n^2 model, respectively, the variance of the mismatch on threshold voltage , the variance of the mismatch on current gain; and the flicker noise voltage in a bandwidth of 1 Hz. In literature, the current gain is often called . Variables AV_{TH}, A_K and K_F are process-dependent constants; and f is the frequency. Parameter (I_{DS}/I_{DS}) represents the mismatch variance in the drain-source current, which includes V_{TH} and . As can see in (A.20), the higher g_m/I_{DS}, higher the contribution of V_{TH} on the I_{DS} mismatch. In weak inversion, the transconductance efficiency is maximum, as can be seen in figure A.2 and thus, higher V_{TH} mismatch is expected.

As a consequence of the above discussion, as the flicker noise and mismatch are approximately inversely proportional to the square root of transistor area, it was assumed that the channel lengths of P_1–P_3 are higher than 35 times the minimum value permitted by the technology.

For the 130 nm process used, A_{VTH} is around 13.5 and 8.1 mV*µm, for NMOS and PMOS devices, respectively. Considering a channel length of 5 µm and a minimum gate area of nearly 60 µm^2, the maximum expected variance of V_{TH} of PMOS devices in our circuit is roughly 1 mV.

After sizing the key transistors of the PTAT current generator, the second step is the sizing of the CTAT current generator composed by $P_{4\text{-}5}$, $P_{11\text{-}12}$ and $N_{5\text{-}6}$. Due to the feedback loop presented in this circuit, I_{R2} is defined by (A.22), where the bias current of N_6 is a copy of I_{R1}

through P_3. Using (A.11), it is possible to rewrite (A.22) as a function of IC, as shown by (A.23).

$$I_{R2} = V_{GS_N6}/R_2 \tag{A.22}$$

$$I_{R2} = [n \cdot U_T \cdot \ln(IC_{N6}) + V_{TH}]/R_2 \tag{A.23}$$

In order to reduce the power consumption and the required value of R_2 (for a given current), N_6 must operate in weak inversion, and thus consequently present a low V_{GS}. We have considered $R_1 = R_2 = R_3$ in order to achieve a good layout matching.

All the recommendations regarding the current mirror discussed for the PTAT current generator is also employed for the CTAT current generator. Regarding the minimum inversion coefficient for the transistor of the current mirror, equation (A.24) that describes the minimum supply voltage for the ICTAT current generator, should be taken into account.

$$VDD_{MIN,3} = V_{SG_P4} + V_{SG_P11} + V_{DSAT_N5} \tag{A.24}$$

The third step is the sizing process for the current adder composed by devices $P_{6\text{-}7}$, $P_{13\text{-}14}$ and R_3. This sub-circuit is responsible to add the PTAT and CTAT currents in a balanced way and thus, it converts the total current to output voltage. The output voltage is described by (A.25) and (A.26):

$$V_{REF_4} = (I_{P6} + I_{P7}) \cdot R_3 \tag{A.25}$$

$$V_{REF_4} = R_3 \cdot \ (S_{P6}/S_{P4}) \cdot \left(V_{GS_N6}/R_2\right) + (S_{P7}/S_{P2}) \cdot (\Delta V_{GS}/R_1)] \tag{A.26}$$

As can be seen in (A.26), the temperature compensation of V_{REF_4} is provided by a proper sizing of the transistors. Note that R_3 does not affect the temperature compensation, and for this reason, V_{REF_4} can be adjusted to the desired level simply by adjusting R_3.

(S_{P6}/S_{P4}) is set to be 1, with the aim of keeping low power consumption. Therefore, (A.26) can be rewritten as (A.27). Note that V_{REF_4} is a direct function of IC because V_{GS_N6} and ΔV_{GS} are defined respectively by equations (A.14) and (A.11).

$$V_{REF_4} = V_{GS_N6} + (S_{P7}/S_{P2}) \cdot \Delta V_{GS} \tag{A.27}$$

To estimate the required value of (S_{P7}/S_{P2}) for temperature compensation, one can take the derivative with respect to temperature in (A.27). Posing $(dV_{REF_4}/dt) = 0$, one can show that (S_{P7}/S_{P2}) can be found through (A.28).

$$(S_{P7}/S_{P2}) = -TC_{VGS_N6}/TC_{\Delta VGS} \quad (A.28)$$

The temperature coefficient $TC_{_VGS_N6}$ can be roughly estimated using equations (4.4) and (4.5) presented in the begging of chapter 4. The temp. coefficient $TC_{\Delta VGS}$ can be calculated by taking the derivative of (A.15) and checking the temperature coefficient of resistors $R_{1,2,3}$ implemented with high-resistance P-Poly material. A simple temperature sweep simulation can be used to have an estimation of $TC_{\Delta VGS}$ and TC_{VGS_N6}. In summary, the current mirror composed by P_6 and P_7 is sized to allow proper temperature compensation. P_6 and P_7 transistors should also operate in moderate inversion.

Finally, after the manual estimation of the transistor dimensions using the above methodology, some simulation iterations were carry out using Spectre in order to find the appropriate values of transistor size. At this point, an additional simulation step that can be realized is the sensibility analysis. The sensibility analysis is the calculation of the dependency of the output voltage on the device parameters (*e.g.* W, V_{TH}, u_0). It helps the designer to find out the most critical devices and their impact on the V_{REF}. This type of analysis can be useful to provide recommendations regarding which transistors should be optimized and designed with more area in order to reduce fabrication process variability. Or, for instance, to find out which devices or parts of the circuit is more susceptible to the impact of TID.

Table A.2 shows the results of sensibility analysis of V_{REF_4} at 22.5 °C (figure 4.10 shows the devices names). The sensibility parameter is given by the ratio of the output variable to the change in an input design parameter. As one can see, the PTAT current generator is the most sensitive part of the circuit and the diode-connected transistor, P_2, of the current mirror is the critical device. This happen because V_{REF_4} is a direct function of I_{BIAS} multiplied by high gain, S_7/S_2, needed to achieve the temperature compensation. N_3 and N_4 are also critical devices because they define the value of I_{BIAS} and its TC.

This section shows a detailed step-by-step design procedure used for V_{REF_4}. However, the equations and the idea presented can be employed in the design of any voltage reference circuit. A numerical example of the above step-by-step design procedure can be found in our paper (COLOMBO, 2011).

Table A.2: Sensibility analysis for V_{REF_4} at 22.5 °C

Sensibility	**Parameter**	**Device**	**Sensibility**	**Parameter**	**Device**
$+7.4*10^4$	L	P_2	$+1.9*10^4$	L	N_3
$-7.0*10^4$	W	P_2	$-1.5*10^4$	L	N_4
$-6.3*10^4$	W	N_3	$+9.8*10^3$	W	P_6
$+5.3*10^4$	W	N_4	$-9.7*10^3$	W	P_5
$-3.6*10^4$	L	P_7	$-5.9*10^3$	L	P_3
$+3.5*10^4$	W	P_7	$+5.6*10^3$	W	P_3
$-3.3*10^4$	L	P_1	$+4.2*10^3$	L	N_6
$+3.1*10^4$	W	P_1	$+1.9*10^3$	W	N_2
$-2.2*10^4$	L	P_6	$-1.8*10^3$	W	N_1
$+2.2*10^4$	L	P_5	$-1.0*10^3$	W	N_6

Source: the author